A ONE CHIP HARDENED SOLUTION FOR HIGH SPEED SPACEWIRE SYSTEM IMPLEMENTATIONS

Session: Components

Long Paper

Joseph R. Marshall and Richard W. Berger

BAE Systems, 9300 Wellington Road, Manassas, Virginia 20110 USA

Glenn P. Rakow

NASA-GSFC, Code 561, Greenbelt, Maryland 20771 USA

E-mail: Joe.Marshall@baesystems.com, Richard.W.Berger@baesystems.com, Glenn.P.Rakow@nasa.gov

ABSTRACT

An Application Specific Integrated Circuit (ASIC) that implements the SpaceWire protocol has been developed in a radiation hardened 0.25 micron CMOS technology. This effort began in March 2003 as a joint development between the NASA Goddard Space Flight Center (GSFC) and BAE Systems. The BAE Systems SpaceWire ASIC is comprised entirely of reusable core elements, many of which are already flight-proven. It incorporates a router with 4 SpaceWire ports and two local ports, dual PCI bus interfaces, a microcontroller, 32KB of internal memory, and a memory controller for additional external memory use. The SpaceWire cores are also reused in other ASICs under development. The SpaceWire ASIC is planned for use on the Geostationary Operational Environmental Satellites (GOES)-R, the Lunar Reconnaissance Orbiter (LRO) and other missions. Engineering and flight parts have been delivered to programs and users.

This paper reviews the SpaceWire protocol and those elements of it that have been built into the current and next SpaceWire reusable cores and features within the core that go beyond the current standard and can be enabled or disabled by the user. The adaptation of SpaceWire to BAE Systems' On Chip Bus (OCB) for compatibility with the other reusable cores will be reviewed and highlighted. Optional configurations within user systems and test boards will be shown. The physical implementation of the design will be described and test results from the hardware will be discussed. Application of this ASIC and other ASICs containing the SpaceWire cores and embedded microcontroller to Plug and Play and reconfigurable implementations will be described. Finally, the BAE Systems roadmap for SpaceWire developments will be updated, including some products already in design as well as longer term plans.

1. SPACEWIRE PROTOCOL AND USAGE

The SpaceWire protocol was defined in the European Cooperation for Space Standardization (ECSS) group as ECSS-E-50-12A. It grew out of the IEEE 1355 standard and earlier efforts to develop high performance point to point standard interfaces between computer nodes. With the advent of Low Voltage Differential Signaling (LVDS) devices being used in space, it has become possible to marry these physical elements with straightforward high performance logic and create space qualifiable devices that deliver the power and performance required.

The current SpaceWire standard defines the interface at the signal, physical, character, exchange, packet and network levels. Further standardization of higher and parallel sections

such as those needed for plug and play are in development. At the signaling level, data stream encoding is used to embed clocks and data across two signals in each direction. Each of these are physically transmitted using LVDS circuitry. Thus a total of eight logic wires and a ground are in each standardized cable, with 9 pin micro-D connectors on each end. At the character level, there are two types, control and data, each with embedded parity for fault detection. Control characters are used for flow control, packet completion and special combinations with data characters for the link. Data characters carry the message and time codes. Null characters are sent when no other character is available in order to maintain a link. Flow control, which manages the sending of characters when there is space at the receiver and detection of parity and disconnect errors, is handled at the exchange level. The packet level uses a destination header on the front and an end of packet marker on the back to encapsulate packets. At the network level, there are two addressing modes defined – path addressing and logical addressing. Path addressing concatenates the path as a series of addresses, each one stripped off as the packet traverses a SpaceWire network. Logical addressing maintains a lookup table and a global addressing scheme across a SpaceWire network.

SpaceWire links provides a scalable full duplex communications that may be expanded through the use of routers to most any size network. Three typical uses of the SpaceWire in a spacecraft are shown in Figure 1. A Control Tree has one CPU (or two with redundancy) performing the normal C&DH functions and controlling and sending and receiving data from several instruments and other subsystems. The 4 port router block shown provides direct connections between the CPU and three additional instruments. If more instruments or subsystems were present, the router could be expanded to more ports, a second router added and daisy-chained or routers could be added to some instruments. We will discuss router configurations further later in this paper.

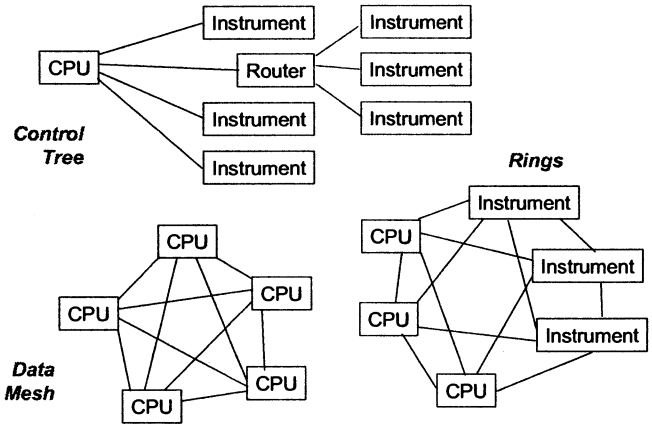


Figure 1: Typical SpaceWire Topographies

Data meshes are used for pure communications between a set of peers. If a CPU has four SpaceWire ports, it can take part in a five CPU mesh and have direct connections with four others. If more CPUs / peers are in the system, routers could be used to expand the connectivity either within the CPUs or as separate switches. In the Ring topology, one or more CPUs have connectivity with several instruments or other subsystems and they are connected by rings. In this picture, six nodes are connected by an outer ring and three nodes each are connected to each other by sub-rings. These could also be done as a second outer ring. This structure is easily expanded simply by adding nodes and the fault tolerance remains the same.

The SpaceWire interface is constantly being compared to other interfaces for potential space usage. Table 1 shows a comparison between SpaceWire (*based on BAE's implementations) and three other interfaces it may be used to replace. With its higher potential data rate per network, SpaceWire offers the most scalability and flexibility in building high performance networks.

Standard	SpaceWire	MIL-STD-1553B	1394a	cPCI
Attribute				
Width	Serial	Serial	Serial	32/64
Topology	Point to Point	Bus	Point to Point	Bus
Maximum Frequency	10-264 MHz*	1 MHz	100-400 MHz	33-66 MHz
Maximum Data Rate/Node	212 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Data Rate/Network	27136 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Nodes	256 (Unlimited)*	32	63	8 to 4
Isolation between Nodes	LVDS	Transformer	Galvanic	Resistor
Node Redundancy	Full Port	PHY Only	PHY Only	Device

Table 1: Standards Comparisons

2. SpaceWire Core Design and ASIC Integration

In March 2003, a joint development effort began between BAE Systems and NASA Goddard Flight Center (GSFC) to join the GSFC SpaceWire IP with the BAE Systems core-based ASIC technologies[1]. The GSFC design was first realized as an FPGA design and implemented in the NASA Swift mission and then upgraded for the James Webb Space Telescope mission. This design was captured in VHDL and converted to a core for BAE Systems R25 CMOS Technology. The core contains four SpaceWire ports and two external ports and a six port routing switch. LVDS physical drivers and receivers are built into this core and mapped onto BAE Systems LVDS I/O circuits in the R25 technology. These LVDS circuits are capable of 600 MHz operation, however the combined SpaceWire circuit and link budget supports full protocol speeds to 264 MHz. 32-bit wide, 64 deep FIFOs are utilized for each transmit and receive function.

Figure 2 below shows the internal blocks of SpaceWire ASIC.

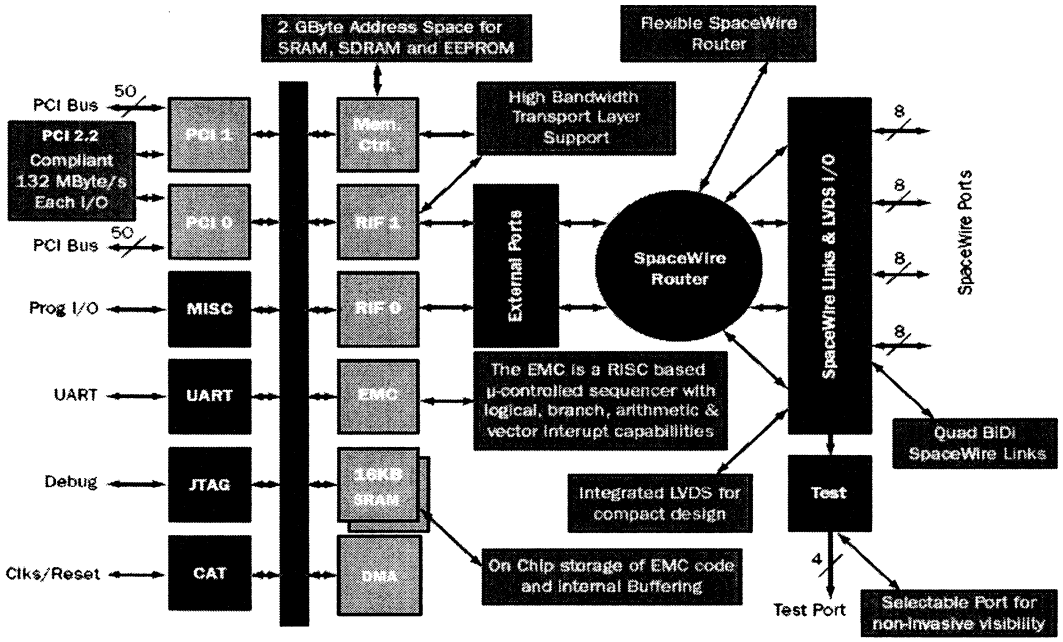


Figure 2: SpaceWire ASIC Block Diagram

The elements in blue on the right make up the SpaceWire core provided by GSFC. The external ports in the SpaceWire core provide the connection into the rest of the SpaceWire ASIC. These are connected by two Router Interfaces (RIF) into the cross-bar switch connection fabric within

the ASIC. This connection medium is termed the On Chip Bus (OCB) and is shown as the blue bar between all the square cores in the figure. Each RIF contains DMA controllers in each direction and may connect to any other core on the OCB. The other cores shown are all reused from other BAE Systems programs and include the Peripheral Component Interface (PCI), Miscellaneous core containing programmable I/O discretes (MISC), Universal Asynchronous Receiver Transmitter (UART) I/F for debug and low speed data transfers, Joint Test Action Group (JTAG) Interface, Direct Memory Access (DMA) usable by any other intelligent core for independent transfers, a Memory Controller that may access external SRAM, SDRAM or EEPROM (Mem Ctrl.), an Embedded Microcontroller (EMC), two 16 KB SRAM cores for buffering data from any core or interface on the OCB or storing programs for the EMC and the Clock and Timer (CAT) core. Only the CAT and MISC core were changed for the SpaceWire ASIC design, maximizing the reuse and minimizing the design risk.

The OCB is made up of 32 bit and 64 bit connections. All of the lighter (tan) blocks shown in the figure above are 64-bit and have connectivity to all other blocks. The darker (blue) blocks are 32 bit, low performance and connect through a single 64 to 32 bit bridge to the rest of the OCB 64 bit fabric.

3. SpaceWire ASIC Implementation

The SpaceWire ASIC is implemented in BAE Systems R25 Technology[1]. It is packaged in a 624 pin 32.5mm Ceramic Column Grid Array (CCGA) package. It operates with a core voltage of 2.5V and an I/O voltage of 3.3V. The design uses 423 of the 512 available signal pins. The ASIC utilizes five sets of clocks that may be similarly derived or unique – one drives the ASIC system clock, one drives the internal logic of the ASIC, one is used for the PLLs that set the speed for the SpaceWire ports and two are used for the PCI cores. The PLL may be user selectable to 1x, 1.5x, 2x, 2.5x, 3x, or 3.5x by configuring the clock and timing core. This is typically done with EMC code. The clocks so generated may then be divided by each port for individual port transmission speeds and provide a significant flexibility in configuring and using each port to best match its data bandwidth needs.

Any use of the SpaceWire ASIC includes analyzing the paths through the ASIC. Because of the cross-bar nature of the OCB, multiple transfers may be going simultaneously as long as they do not collide at a destination block. Thus, data may be moving through two SpaceWire ports into/out of external memory and onto/off of a PCI Bus at the same time that the EMC is executing a program and working out of internal memory, the DMA controller is moving data from JTAG onto the other PCI interface, and data is moving through the router between the remaining two SpaceWire ports. Such a maximum configuration is shown in Figure 3. A more typical operation would have some conflicts and the key analysis is latency and waiting for an interface or memory to become unblocked. External memory is especially useful for buffering data and then processing or moving it out on an interface once it has become available.

The EMC[2] is a special block and one that provides a significant processing capability for the SpaceWire ASIC. The third generation of this BAE Systems-designed core is used in the SpaceWire ASIC. It is able to execute instructions at the internal ASIC speed and includes a small instruction cache for tight loop high performance. The EMC is able to access any core on the OCB and thus can talk on any interface. Its instructions are typically stored in a non-volatile memory such as EEPROM or BAE Systems' new chalcogenide-based C-RAM and then copied into the internal SRAM on the ASIC for execution. An assembler, linker, C Compiler and simulator are all available for EMC code development.

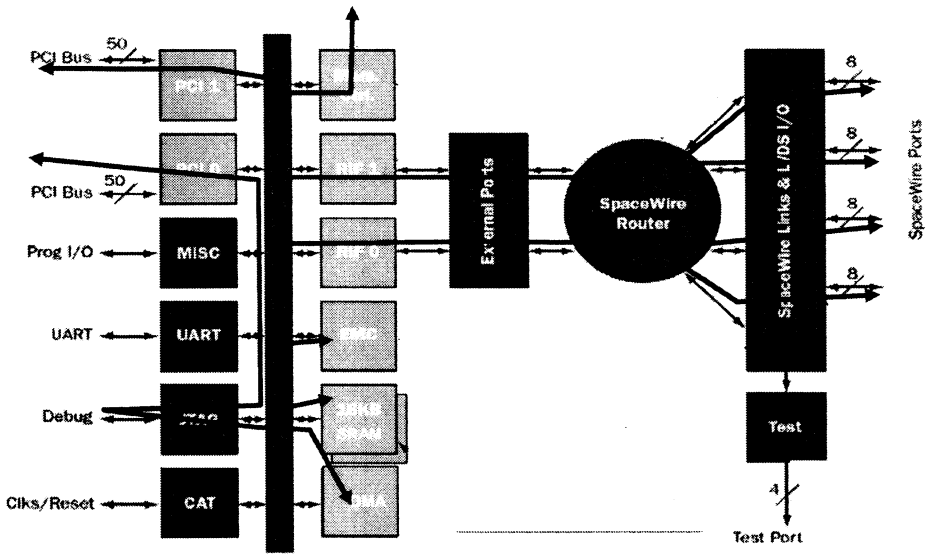


Figure 3: Simultaneous Paths Through the SpaceWire ASIC

The EMC uses a straightforward instruction set and has an execution structure shown below which is simple and elegant compared to other more complex microcontroller cores. Using a 66 MHz clock, it can execute at around 10 Dhrystone MIPS. This provides a significant adjunct processing capability and has been used for startup and configuration as well as post processing of packets sent to the SpaceWire ASIC. The EMC block diagram is shown in Figure 4.

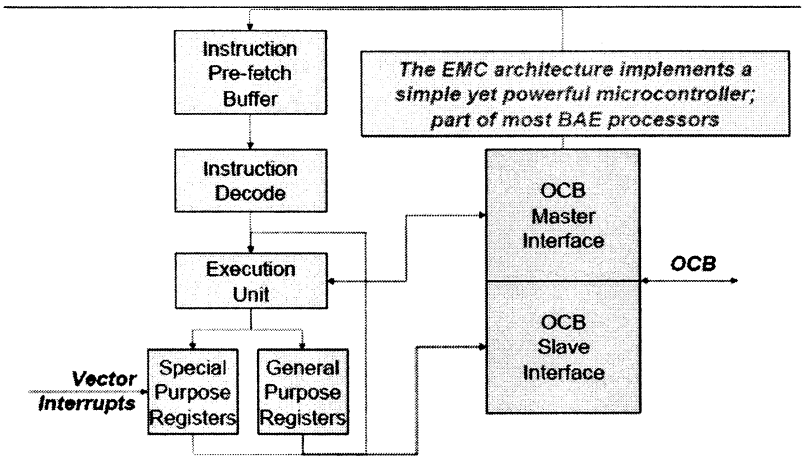


Figure 4: Embedded Microcontroller Core Block Diagram

The SpaceWire ASIC is built out of R25 Technology and is thus power efficient for this technology. It is radiation hardened to 200 Krads(Si) total ionizing dose, has an single event upset rate of less than 1E-9 errors/bit-day, and is latch-up immune. The SpaceWire ASIC has been measured to draw between 1 and 2.5 Watts in use to date at speeds up to 132 MHz. It is expected that if all four ports are being used as wells as most interfaces at full speeds, the typical power would peak around 4 watts.

4. SpaceWire ASIC Usage and Configurations

The SpaceWire ASIC has been used on two different boards for the NASA Lunar Reconnaissance Orbiter mission due to be launched in 2008. Both are single board computers

and include BAE Systems RAD750 processor, memory, other interfaces and functions. Four ports are brought out from each and used for connectivity in the system. One is built in a standard 6U-220 CompactPCI form factor and the other to a more custom slice form factor. The LRO single board computer is described in much more detail in a separate paper[3]. Both types of flight boards have been space qualified and delivered for integration.

The SpaceWire ASIC has also been delivered to other companies of use on the Geostationary Operational Environmental Satellite (GOES-R) and is available for use in other spaceborne applications as a standard product. In another application, the SpaceWire ASIC has been used as a standalone control chip for the Universal FPGA Support Device (UFSD) Test Board[4], a 6U-220 CompactPCI reconfigurable computing board utilizing Xilinx RAM-based FPGAs for space. One of the PCI Busses is brought to the backplane for connection to other CompactPCI boards while the second PCI bus is connected to one or more FPGAs on the board. The EMC in the SpaceWire ASIC is the master microcontroller on the board and is used to setup and configure the board. A second EMC is contained in the FPGA Resource Enabling Device (FRED) ASIC that manages the array of FPGA devices, the FPGA Resource Enabling Device. Both utilize BAE Systems new C-RAM non-volatile memory on the board to save program and configuration information. The SpaceWire ASIC provides two levels of system interfaces for the board – CompactPCI and four SpaceWire ports.

BAE Systems is developing a customer evaluation board based on these various board designs. A block diagram is shown below in Figure 5. At its center is the SpaceWire ASIC with onboard EEPROM to store configuration information and code for the ASIC's EMC and SRAM for buffering messages as well as scratchpad memory. Only one PCI interface will be utilized and this will form an external CompactPCI interface for the card. The card will run from 5V and 3.3V supplies on the backplane and develop the 2.5V on the card. It will have options to use an onboard oscillator for its clock sources or an external clock source from the backplane. Finally, the JTAG, UART, various discretes and a SpaceWire sniffing port will be available on a test connector.

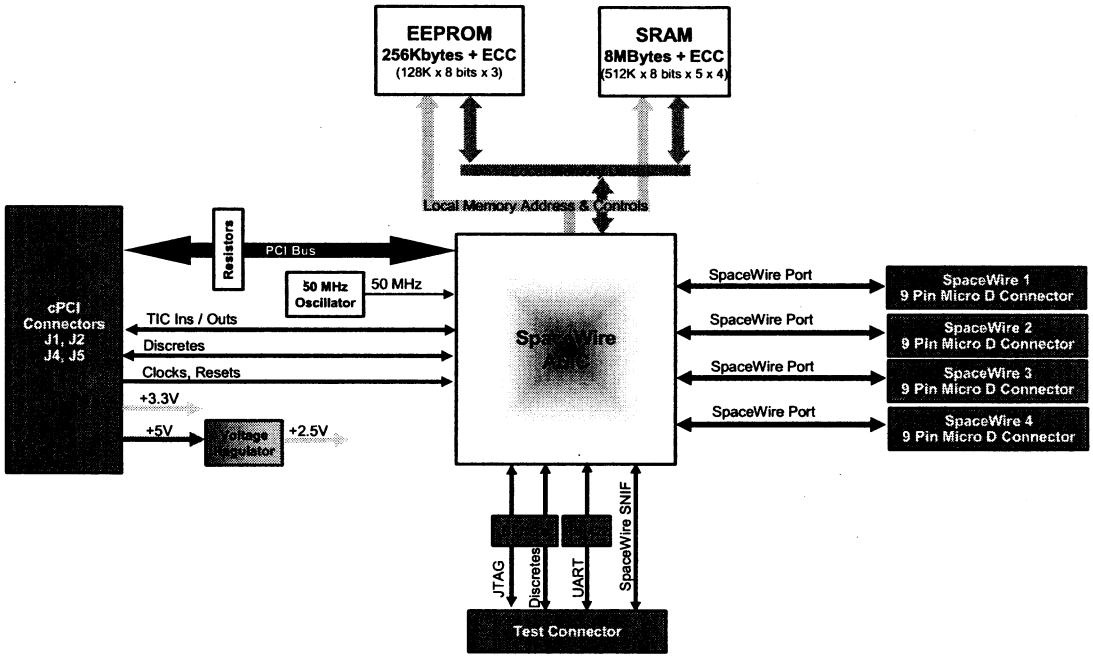


Figure 5: Four Port CompactPCI 6U SpaceWire Evaluation Board Block Diagram

The board will be implemented on a 6U-160 Compact PCI form factor. Each of the SpaceWire connectors will use the standard 9 pin micro-D connectors. A mock-up of this board is shown in Figure 6 below. Since there is so much extra space on the board, it will be very easy to layout and produce. For an actual space product, it is expected that more optional memory or other functions will take advantage and fill the board.

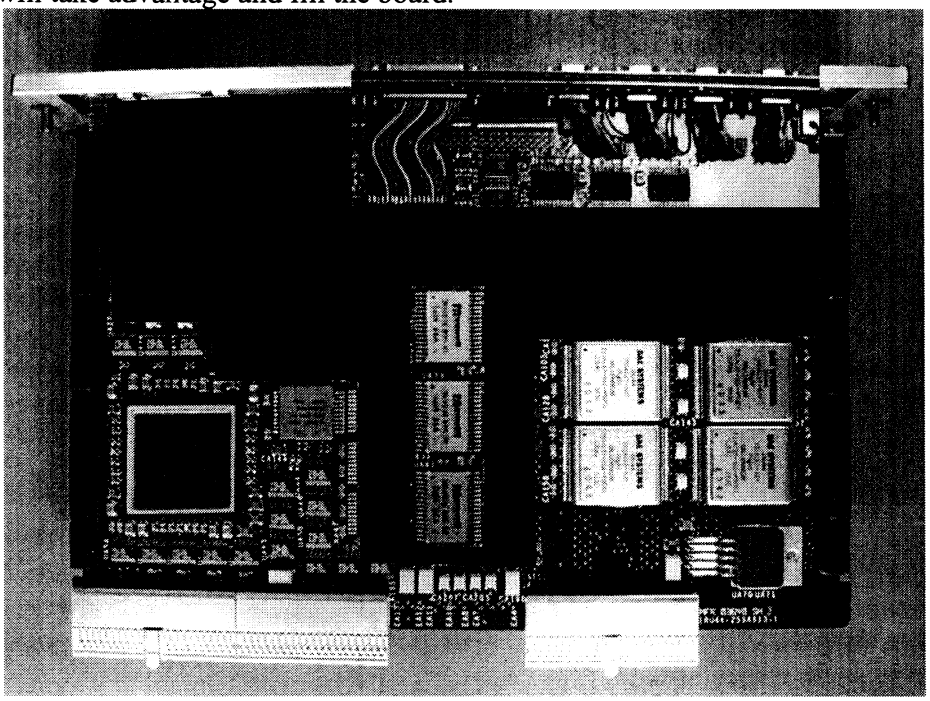


Figure 6: SpaceWire Evaluation Board Mock-up

The SpaceWire ASIC has been successfully integrated into the boards described above. Due to the high amount of reuse from both GSFC and BAE Systems, very few design problems were expected or encountered and all errata have workarounds. Potential users may design in this stable device or board into their products. The SpaceWire core elements are part of two new ASICs under development at BAE Systems, the RAD6000MC[4][5] and next generation Power PCI bridge ASIC. Both of these will provide four SpaceWire ports and appropriate internal routers to other assets within the device.

As the topologies shown earlier illustrate, there is a need for larger numbers of ports in more complex systems that require any to any switching. The dual PCI busses allow up to 8 SpaceWire ASICs to be placed on a single assembly and provide up to 32 ports with the PCI Busses used for passing data between ports not on the same device. However, these PCI busses may become bottlenecks in a maximum performance case and add latency to the routing function since each is a shared bus. For maximum performance, designs may use some of the SpaceWire ports for connections between external ports and group SpaceWire ASICs onto groups of PCI Busses. An example of such an implementation is shown below in Figure 7 as a 10 port SpaceWire Router using four SpaceWire ASICs.

There are actually three PCI busses shown. One PCI Bus is used only to connect the router to the external world through SpaceWire ASIC 1, probably through a connector. A common PCI bus is routed between all four SpaceWire ASICs and a third PCI Bus is routed between SpaceWire ASICs 2, 3 and 4. SpaceWire ASIC 1 utilizes three of its ports to connect directly to SpaceWire ASICs 2, 3 and 4, providing an alternate routing path between ports not requiring translation to PCI and back. This approach would provide at least 100% more routing performance when compared to a three ASIC solution providing 12 ports. Additionally, BAE

Systems also expects to expand its ASIC solution to between 8 and 24 ports directly with appropriate internal routers as customer needs dictate.

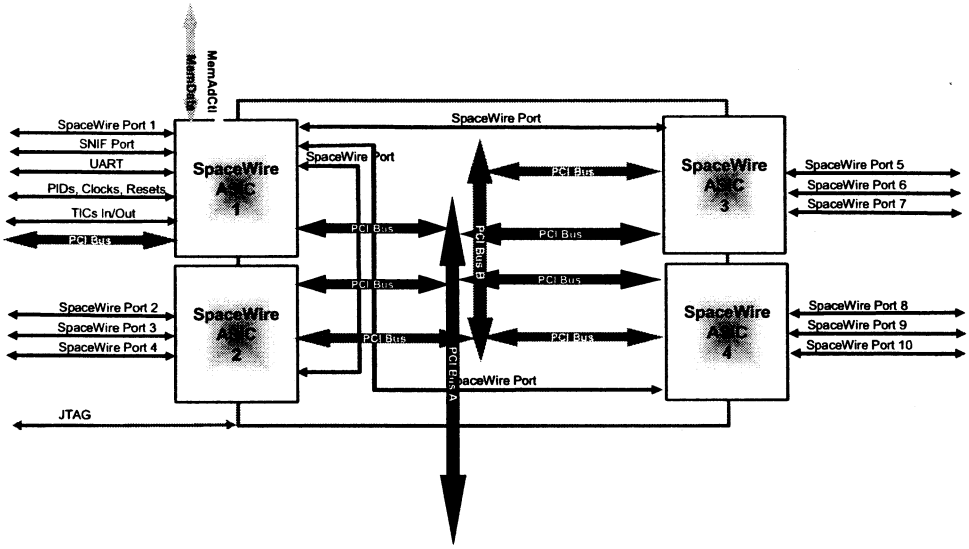


Figure 7: Ten Port Highest Performance SpaceWire Router

To support the SpaceWire ASIC, BAE Systems has developed application programming interfaces (API) for VxWorks. These may be ported to other operating systems. We have also created startup code (SUROM) that configures the SpaceWire ASIC and simple communication code for using the EMC after startup as data is flowing through the ASIC - both may be used as a basis for future applications.

SpaceWire has been identified as one of the key interfaces for the Space Avionics Plug and Play (SPA) standards for responsive space and standardization activities are underway to add appropriate layers and capabilities to the standard to support self discovery, configuration and utilization in such systems. It is very important that existing devices such as the SpaceWire ASIC are able to participate in such standards and BAE Systems and GSFC are part of these standardization efforts. The UFSD Test Board mentioned earlier is being utilized as a potential test vehicle for testing these standards as they become defined.

5. SPACEWIRE ROADMAP

Throughout this paper we have discussed various BAE Systems products for SpaceWire focused around the SpaceWire ASIC. A product roadmap is shown below in Figure 8. At the top is the evaluation board. This is followed by the two LRO SpaceWire RAD750 boards. Next, we show how high speed multiple gigabit per second SERDES cores may be utilized for a higher speed version of SpaceWire followed by the RAD6000MC microcontroller. A potential 24 port ASIC and the next generation Power PCI Bridge round out new offerings while the actual current SpaceWire ASIC is shown on the bottom line. As this shows, BAE Systems has both current products and plans for future improvements to make the use of SpaceWire more cost effective and higher performance.

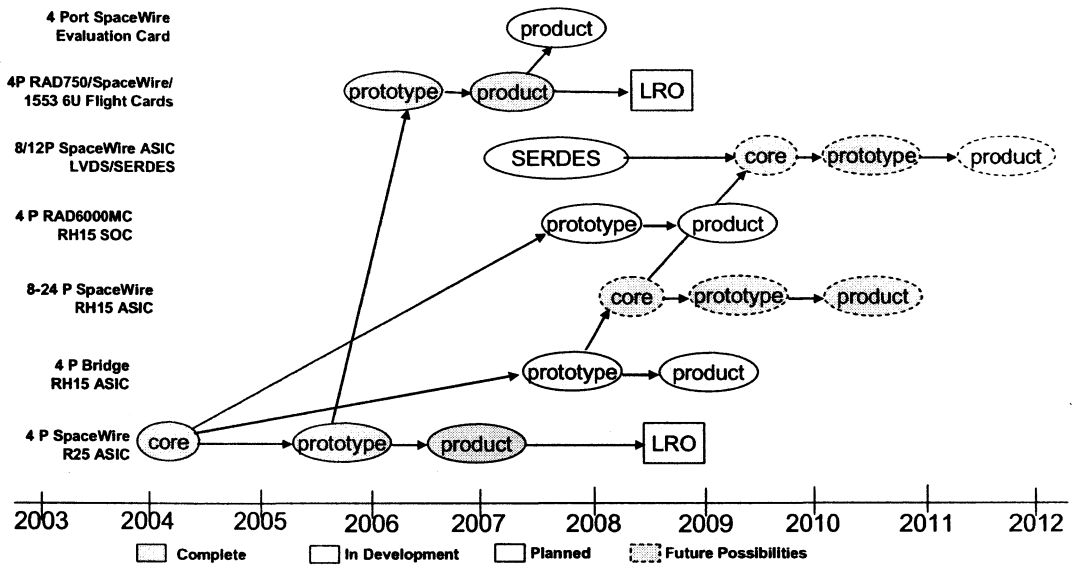


Figure 8: SpaceWire Product Roadmap

6. SUMMARY

BAE Systems along with GSFC has developed a high performance SpaceWire ASIC and successfully applied and qualified it initially to GOES-R and LRO missions and made it part of its future high performance micro-controllers, processors and reconfigurable systems. This device supports multiple topologies and form factors and is cost and power effective for high performance and scalable applications. BAE Systems is developing an evaluation board that will make it easier for its customers to utilize this state of the art Spacecraft product. It is positioned for use in upcoming plug and play and other space applications and is fully supported by support and development software and tools.

7. REFERENCES

[1] Berger, Richard W. et. al., "A Radiation Hardened SpaceWire ASIC and Roadmap", *2006 Military Applications of Programmable Logic Devices (MAPLD) Conference Proceedings*, Washington, DC, September, 2006.

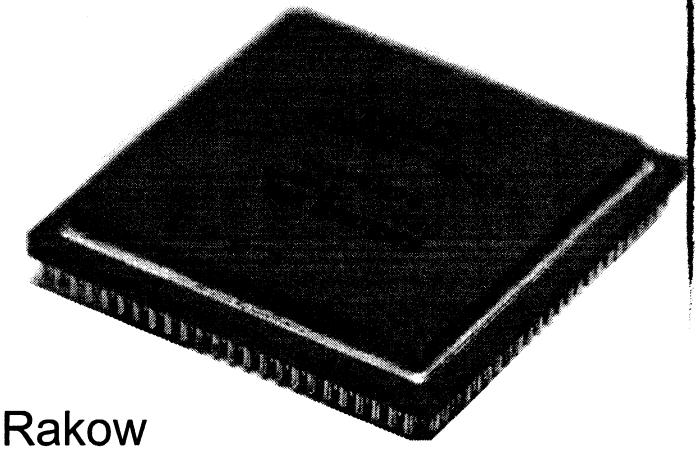
[2] Marshall, Joseph R. & Robertson, Jeffrey, "An Embedded Microcontroller for Spacecraft Applications", *IEEE Aerospace Conference 2006 Proceedings*, Big Sky, Montana, March 2006.

[3] Berger, Richard W. et. al., "RAD750 SpaceWire-Enabled Flight Computer for Lunar Reconnaissance Orbiter", *2007 International SpaceWire Conference*, Dundee, Scotland, September 2007.

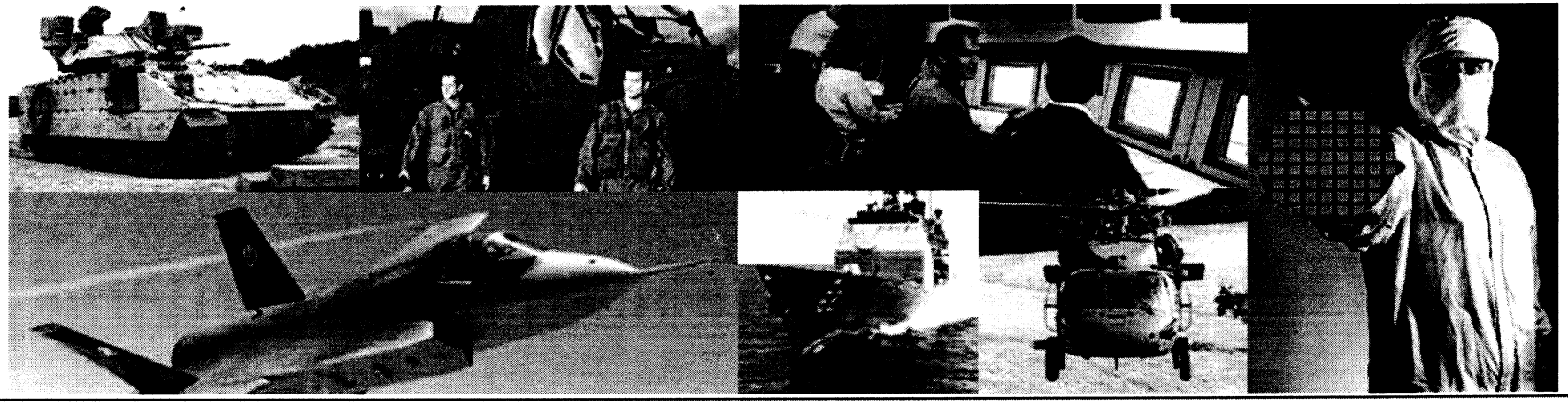
[4] Marshall, Joseph R. et. al., "Reconfigurable and Processing Building Blocks in Responsive Space", *2007 Infotech@Aerospace Conference Proceedings*, Rohnert Park, California, May 2007.

[5] Berger, Richard W. et. al., "A System-On-Chip Radiation Hardened Microcontroller ASIC With Embedded SpaceWire Router", *2007 International SpaceWire Conference*, Dundee, Scotland, September 2007.

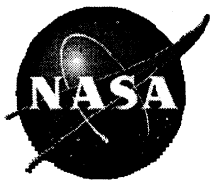
A ONE CHIP HARDENED SOLUTION FOR HIGH SPEED SPACEWIRE SYSTEM IMPLEMENTATIONS



Joseph R. Marshall, Richard W. Berger, Glenn P. Rakow
19 September 2007 – SpaceWire Conference



© 2007 BAE Systems - All rights reserved

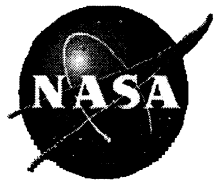


BAE SYSTEMS

Contents

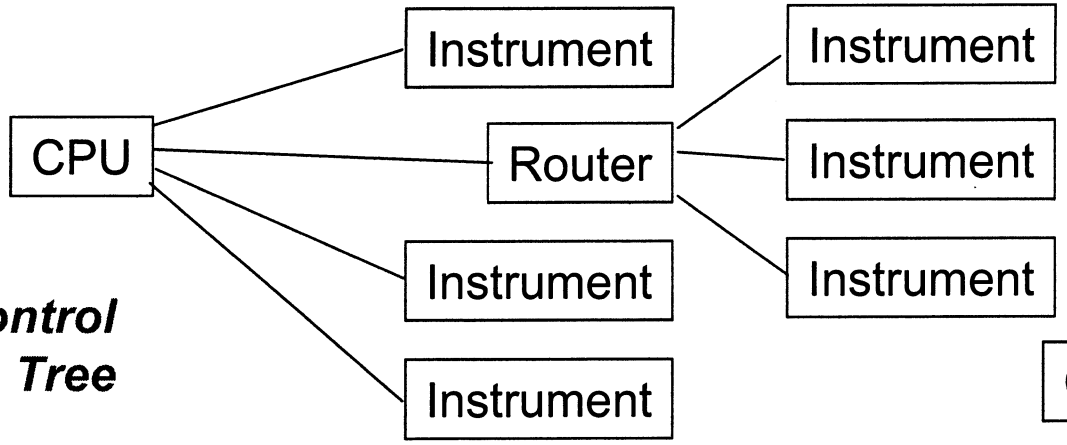
- SpaceWire Standards & Topology
- SpaceWire ASIC Program History
- SpaceWire ASIC Features and Block Diagrams
- SpaceWire ASIC Internal Functions Descriptions and Diagrams
- Embedded Microcontroller Description and Block Diagram
- SpaceWire Boards
- SpaceWire Routers & MCMs
- Support Software and Test Equipment
- SpaceWire Product Roadmap

© 2007 BAE Systems - All rights reserved

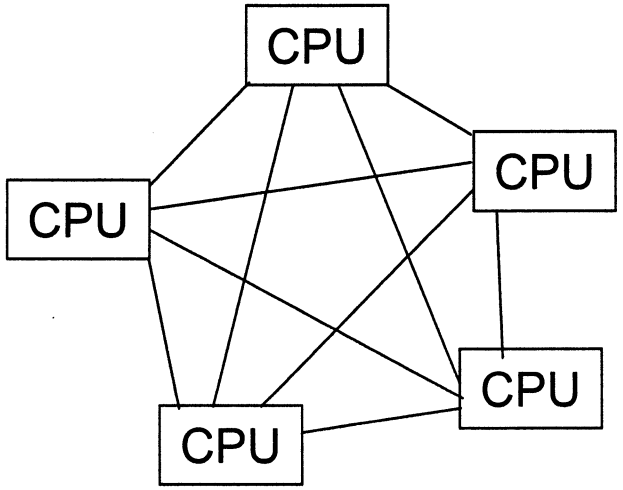


BAE SYSTEMS

Examples of SpaceWire Topologies

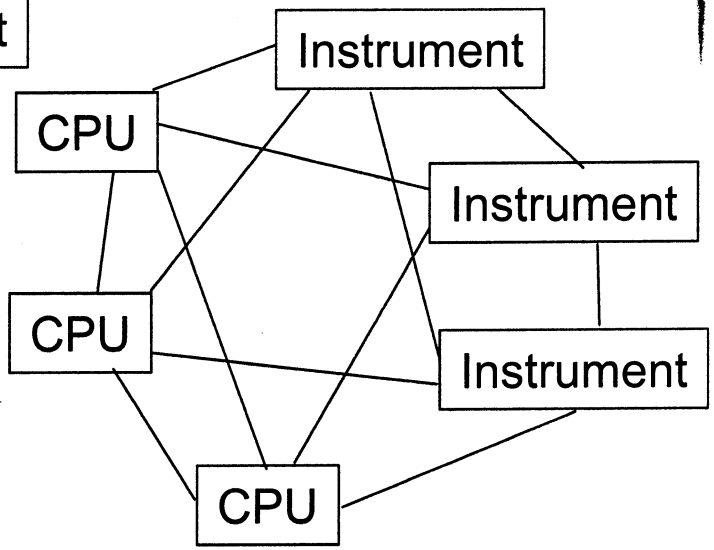


Control Tree



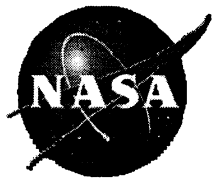
Data Mesh

Rings



The four port router built into the BAE SpaceWire ASIC makes many useful spacecraft topologies possible

© 2007 BAE Systems - All rights reserved



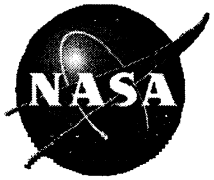
BAE SYSTEMS

Standards Comparison

Standard	SpaceWire	MIL-STD-1553B	1394a	cPCI
Attribute				
Width	Serial	Serial	Serial	32/64
Topology	Point to Point	Bus	Point to Point	Bus
Maximum Frequency	10-264 MHz*	1 MHz	100-400 MHz	33-66 MHz
Maximum Data Rate/Node	212 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Data Rate/Network	27136 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Nodes	256 (Unlimited)*	32	63	8 to 4
Isolation between Nodes	LVDS	Transformer	Galvanic	Resistor
Node Redundancy	Full Port	PHY Only	PHY Only	Device

**Based on BAE Systems Implementations*

© 2007 BAE Systems - All rights reserved

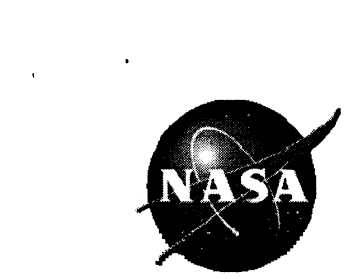


BAE SYSTEMS

BAE Systems SpaceWire ASIC Program

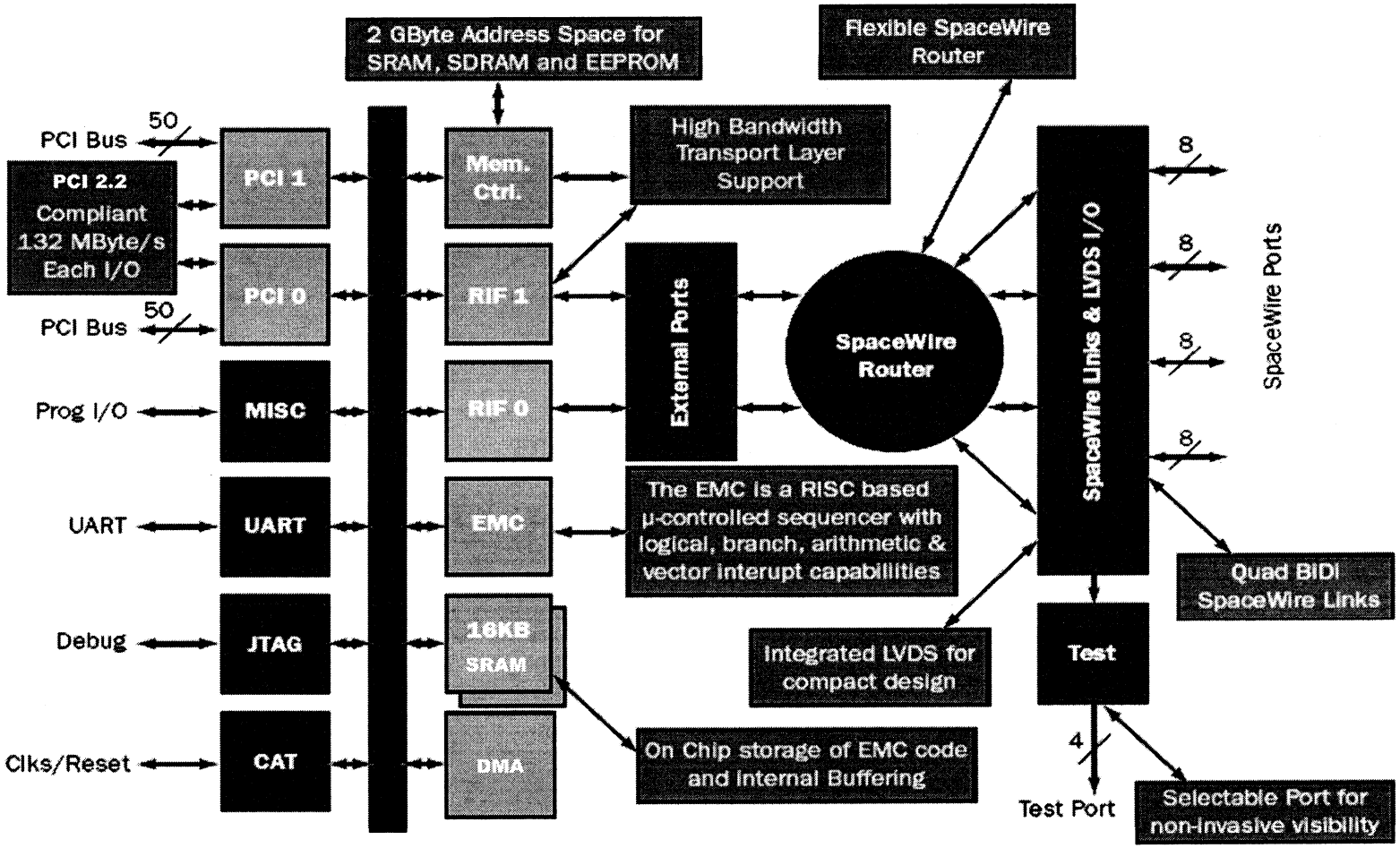
- Program initiated in March 2003
- BAE Systems and Goddard Space Flight Center (GSFC) joint development effort
  - Modeled in VHDL
  - 250nm CMOS technology ASIC
    - 2.5V core supply
    - 6 layers of metal
    - Flip-chip mount to package
  - Based entirely on synthesizable cores
    - Reused BAE Systems cores and On Chip Bus connection medium
    - Reused GSFC SpaceWire router core with extensions for transport layer support and dual external interfaces
    - New interface between router and On Chip Bus
- Design was funded by Glenn Research Center
- Design Changes, manufacturing and test was funded by GOES-R mission
  - First hardware in 4Q 2005
  - Qualification testing is in progress
  - Flight modules available in 4Q 2006

© 2007 BAE Systems - All rights reserved

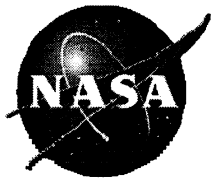


BAE SYSTEMS

4 Port SpaceWire ASIC Block Diagram



© 2007 BAE Systems - All rights reserved

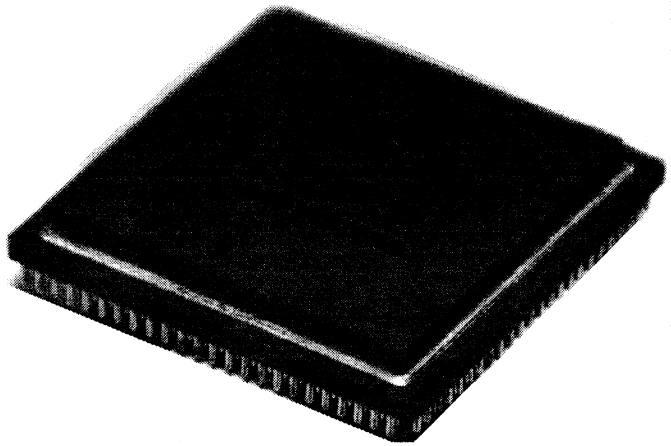


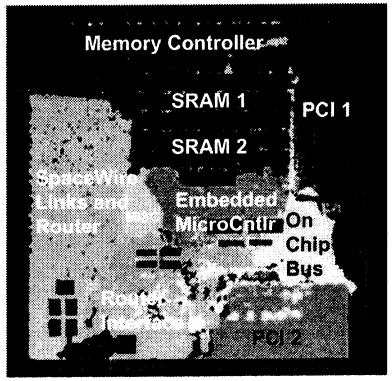
BAE SYSTEMS

4 Port SpaceWire ASIC

- **SpaceWire Interface**
  - 6 port switch
    - 4 SpaceWire serial ports (addresses 1-4)
    - 2 local parallel ports interface to the On Chip Bus via a Router Interface (RIF) core (addresses 5-6) providing higher throughput and minimizing risk of bottlenecks
    - Configuration port is address 0
  - SpaceWire ports include internal LVDS drivers / receivers with support for cold sparing
  - 264 MHz maximum data rate on SpaceWire link interfaces
- **Dual PCI ports (version 2.2)**
  - Up to 66 MHz operation
  - 32-bit address / data bus
  - Parity and cold spare
- **Memory interface w/error correction**
  - Supports EEPROM, SDRAM, SRAM
  - Single bit / nibble error correction
- **Embedded Microcontroller**
  - Internal 32 KB SRAM and DMA Controller
- **Test interfaces**
  - 16550 UART
  - JTAG
  - SpaceWire test data (SNIF) access port
- **Packaging *(TRL-9)***
  - 32mm 624 pin ceramic CGA
  - 423 of 504 signal pins used
- **Low power**
  - 3.3V I/O & 2.5V core supplies
  - 1-4 W depending on speed and usage

- **Radiation hardened R25 library and technology *(TRL-9)***
  - 200 Krad(Si) Total Dose
  - <1E-9 upsets/bit-day SEU
  - Latch-up immune
  - SEU-hardened RAMs, flip-flops, clocks

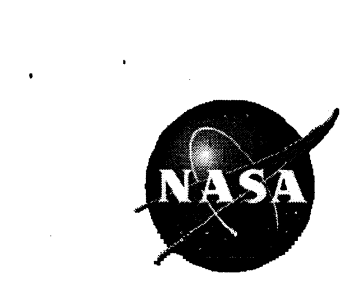




12.7mm x 12.7mm die

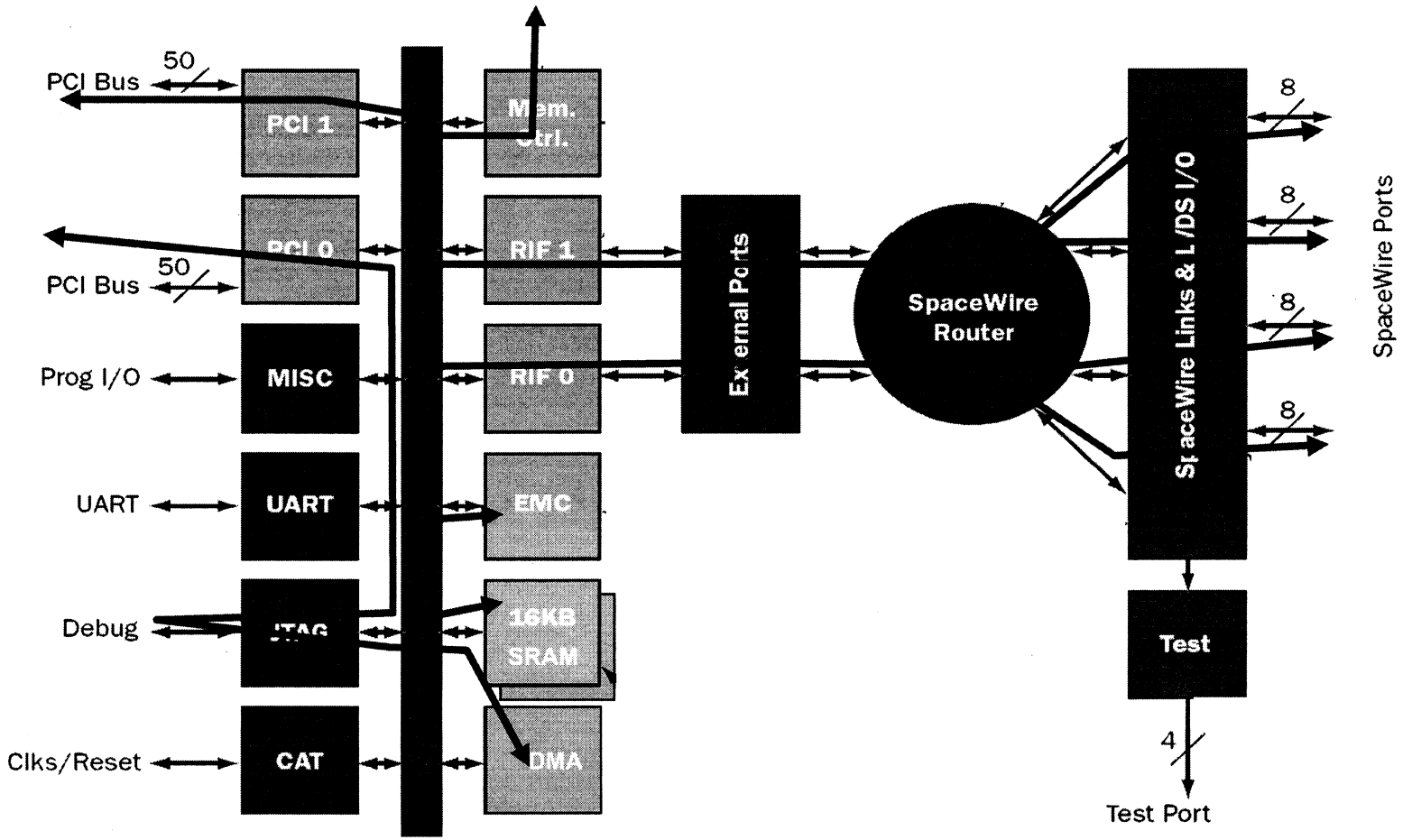
Flight parts and boards are being delivered to multiple space missions

© 2007 BAE Systems - All rights reserved



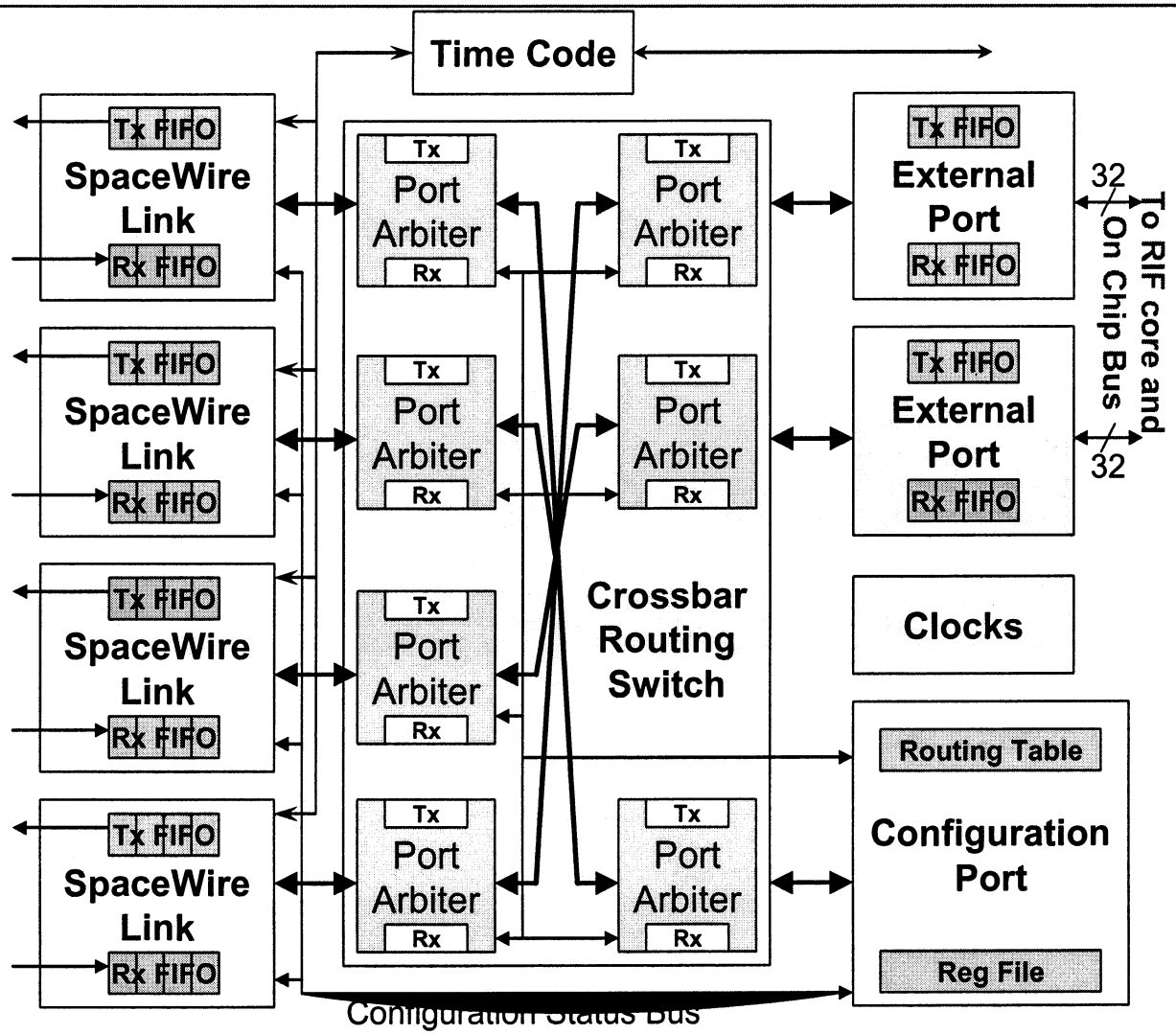
BAE SYSTEMS

Simultaneous Paths through SpaceWire ASIC



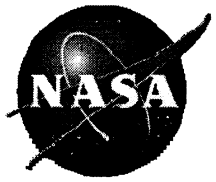
© 2007 BAE Systems - All rights reserved

SpaceWire Router Implementation



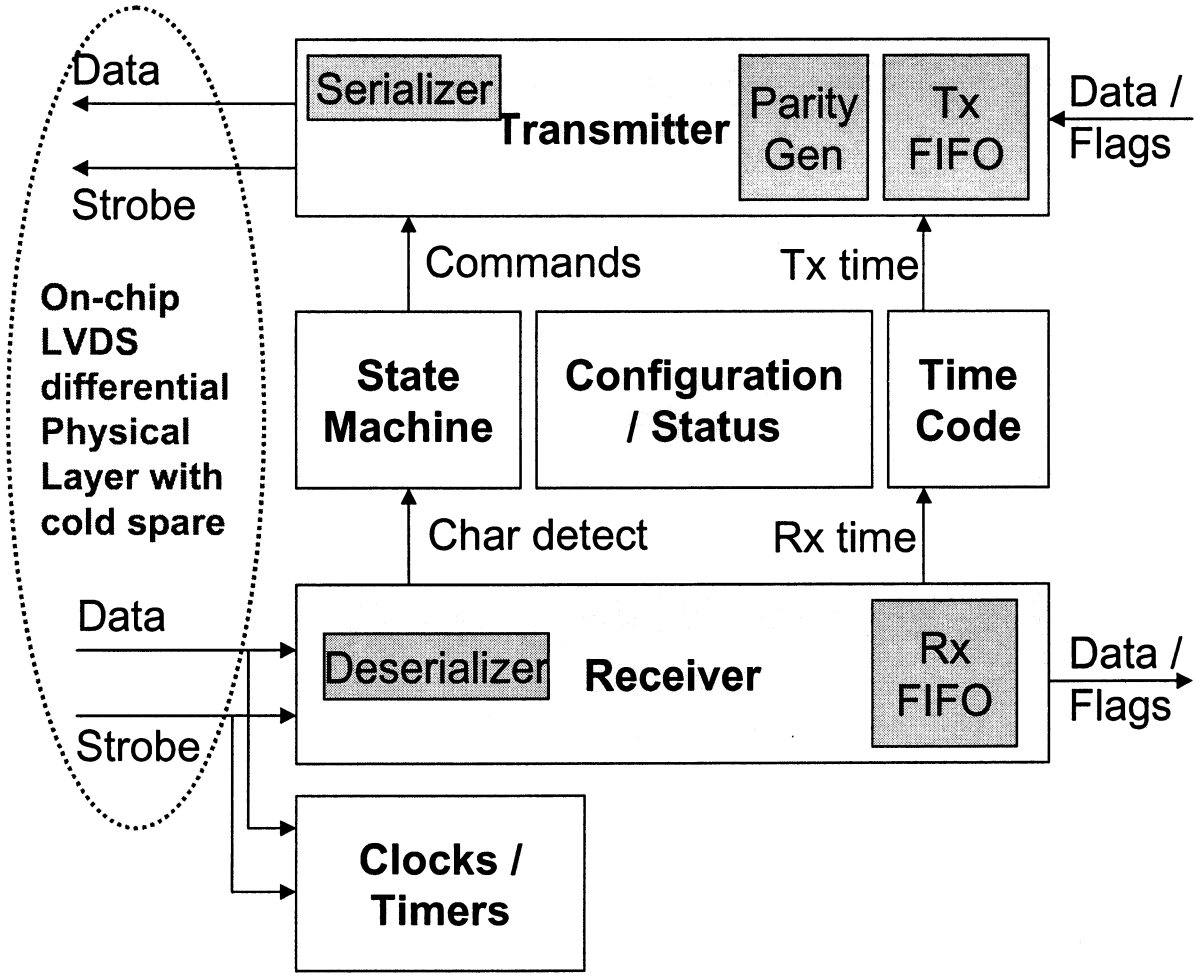
- The router is a non-blocking crossbar switch
  - **Employs non-prioritized, round robin arbitration for output port access upon contention**
  - **Router can limit maximum packet size**
- The router switch implements a port arbiter on each port, each of which has a Tx arbiter and Rx requester
- Bypass mode with local header that defines arrival port and presence of logical address

© 2007 BAE Systems - All rights reserved



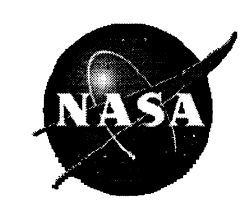
BAE SYSTEMS

SpaceWire Link Port Implementation



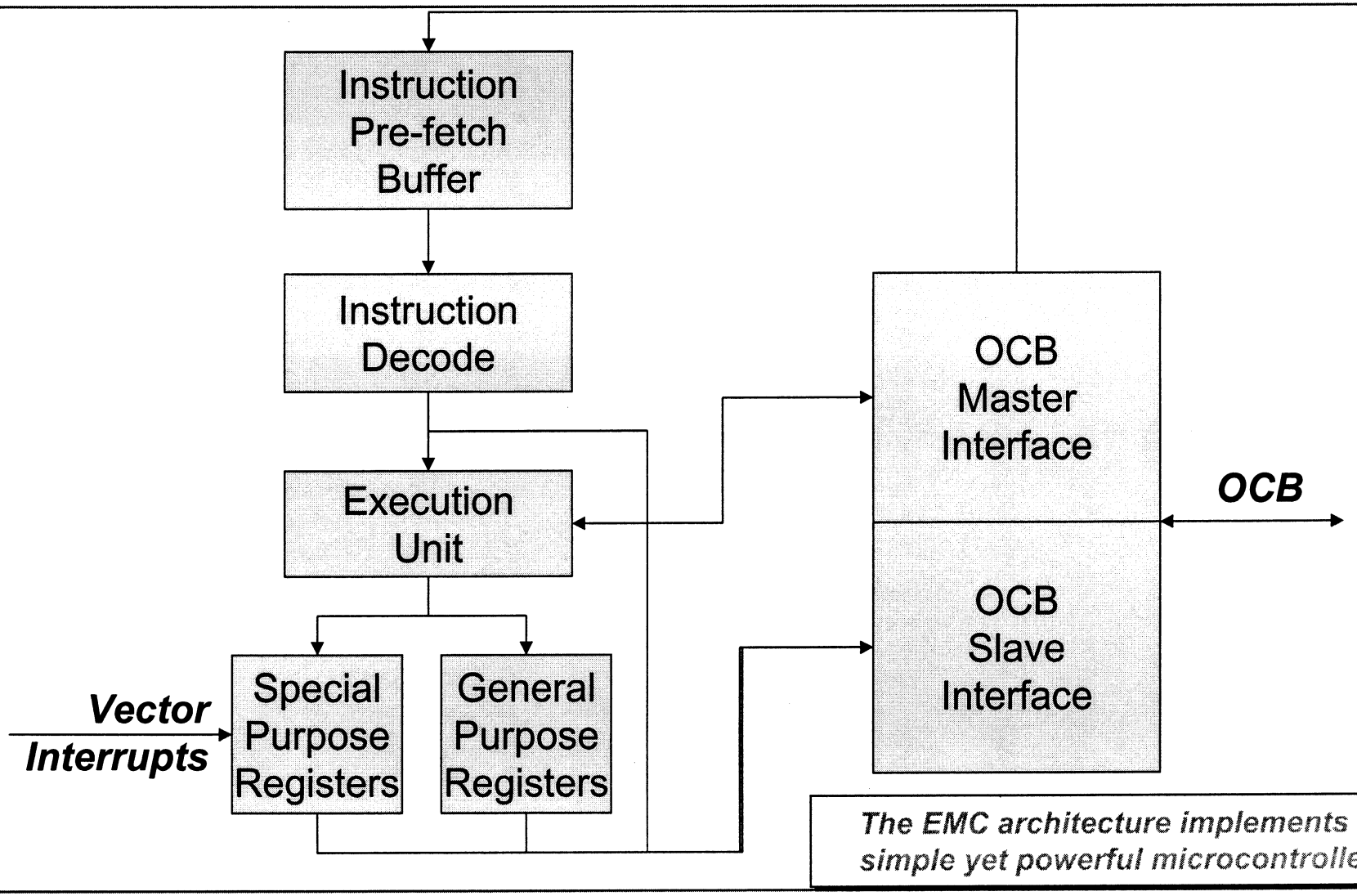
- **Variable SpaceWire data transfer rate**
  - **Controlled by 6-bit rate field**
  - **Generated from Tx clock**
  - **Power-up initializes to 10MHz**
- **The receive clock is recovered by XORing data and strobe signals**
- **The clock block generates the 4x link interface clock via Phase Locked Loop (PLL)**
- **Tx and Rx FIFOs are 64 words deep by 32 bits wide**
- **LVDS drivers and receivers are instantiated on the chip and support cold sparing**

© 2007 BAE Systems - All rights reserved

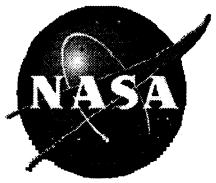


BAE SYSTEMS

EMC Core Block Diagram



© 2007 BAE Systems - All rights reserved



BAE SYSTEMS

Embedded Micro-Controller (EMC)

- Handles Reset of RAD750
- Handles Critical Errors to Keep CPU Out of Checkstop
- Part of Bridge ASIC for RAD750 (Power PCI)
- Also Part of SpaceWire Bridge
- Expanded General Purpose Registers and Instruction Set
- Full Access to Bridge Resources
- Instruction Cache
- One Enhancement Cycle Complete (Enhanced Power PCI)

The EMC takes full advantage of the rich functions of its bridge and the high performance connections to each

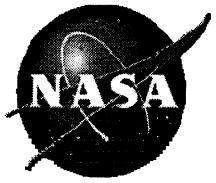
© 2007 BAE Systems - All rights reserved

BAE SYSTEMS

SpaceWire Boards

- LRO SBC Board – 6U 220 RAD750 Single Board Computer
  - 4 SpaceWire Ports + Memory + 1553
- LRO Application Board – Custom Slice RAD750 Single Board Computer
  - 4 SpaceWire Ports + Memory + 1553
- UFSD Test Board – Reconfigurable Processing Board
  - 4 SpaceWire Ports + C-RAM Memory + Xilinx FPGA + FRED + Rocket I/O
- Customer Evaluation Board – 6U 160 SpaceWire CompactPCI Board
  - 4 SpaceWire Ports + Memory

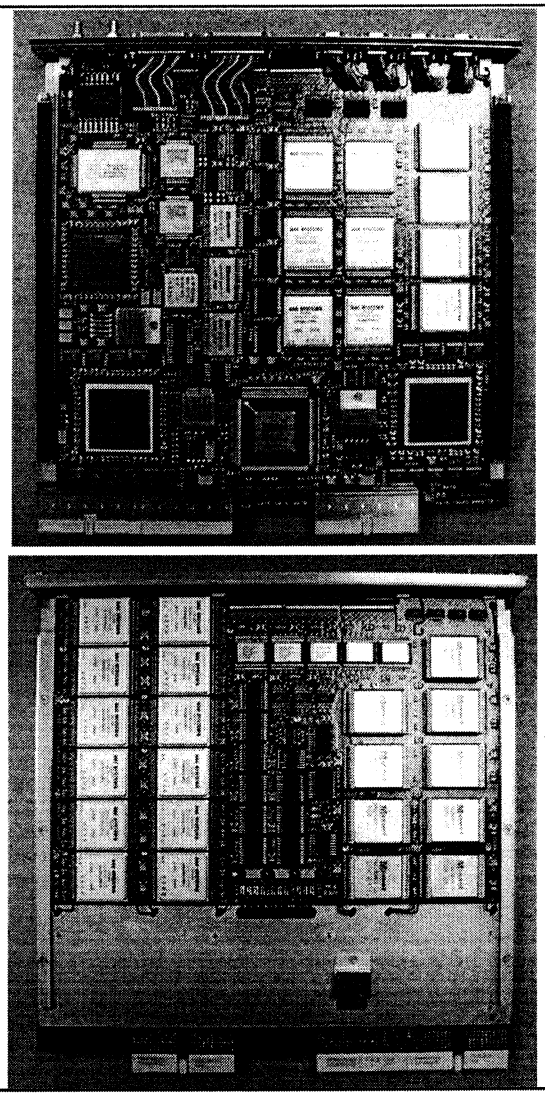
© 2007 BAE Systems - All rights reserved



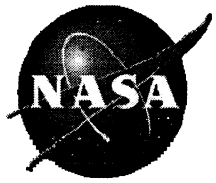
BAE SYSTEMS

4 Port 6U-220 RAD750/SpaceWire/1553 SBC

- **External Interfaces**
  - Backplane Interfaces;
    - 33MHz PCI Bus in CompactPCI compatible format
      - Operates as Central Resource
      - Supports up to five other PCI Bus Masters or Slaves.
    - Provides up to 27 single ended discrete input,
      - discrete output or interrupt input signals
  - Four SpaceWire Interfaces, each capable of operation at up to 264 MHz.
  - MIL-STD-1553B Bus A & Bus B interfaces; Operates as either BC or RT
  - Provides four RS-422 discrete inputs and four RS-422 discrete outputs.
    - Also provides an RS-422 watchdog timer expired output.
  - Test interface containing JTAGs and UART for ground level debug
- **Capabilities**
  - RAD750 PowerPC 750 running internally at 132 MHz and externally at 66 MHz
  - En-Power PCI & SpaceWire contain Embedded Microcontrollers running at 66MHz
  - Six 32-bit programmable up/down timers; Four of these can be externally operated.
  - Multiple DMA Controllers – contained within the En-Power PCI, SpaceWire and SPIF
  - Local Memory EEPROM can be powered off while the LRO En-SBC remains active.
- **Capacities**
  - Local Memory SRAM = 36 Mbytes plus SECDED error correction code (ECC)
  - Local Memory EEPROM = 4 Mbytes plus SECDED ECC
  - SpaceWire SRAM = 8 Mbytes plus SECDED ECC
  - SUROM = 64Kbytes (PROM) or 256Kbytes (EEPROM) plus SECDED ECC
  - 1553 SRAM = 64Kbytes
- **Characteristics**
  - Operates from +3.3V and +5.0V supplied at backplane;
    - Requires proper voltage sequencing.
  - Operating Temperatures: -20°C to +50°C
  - Power consumption (est.): Maximum of 21.4 Watts for LRO usage.
  - Card envelope: Height=40.64mm, Width=231mm, Length=220mm.
  - Weight (est.): 3.790 lbs (1.723 kg)

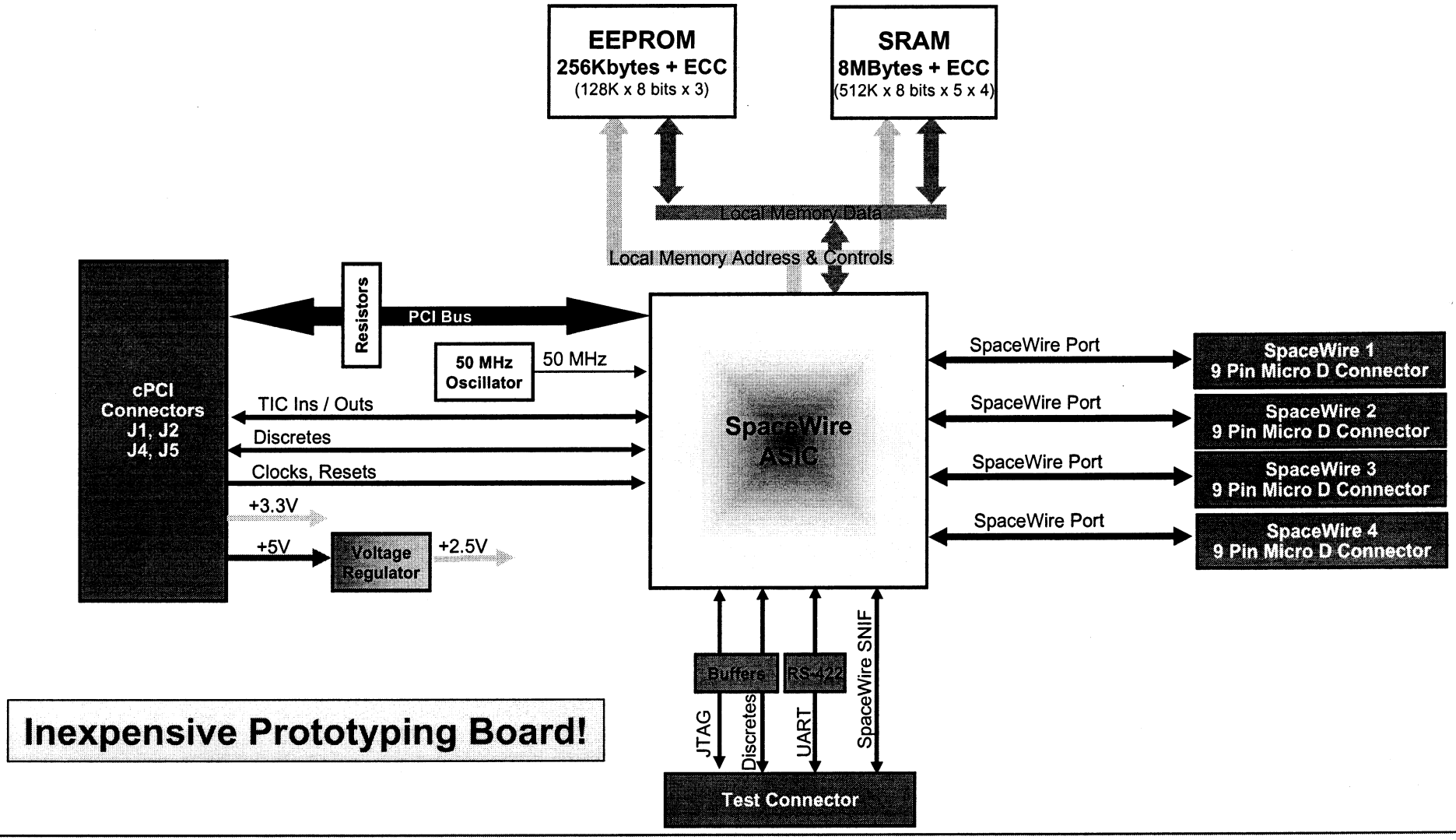


© 2007 BAE Systems - All rights reserved



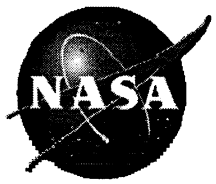
BAE SYSTEMS

4 Port SpaceWire 6U cPCI Evaluation Board



Inexpensive Prototyping Board!

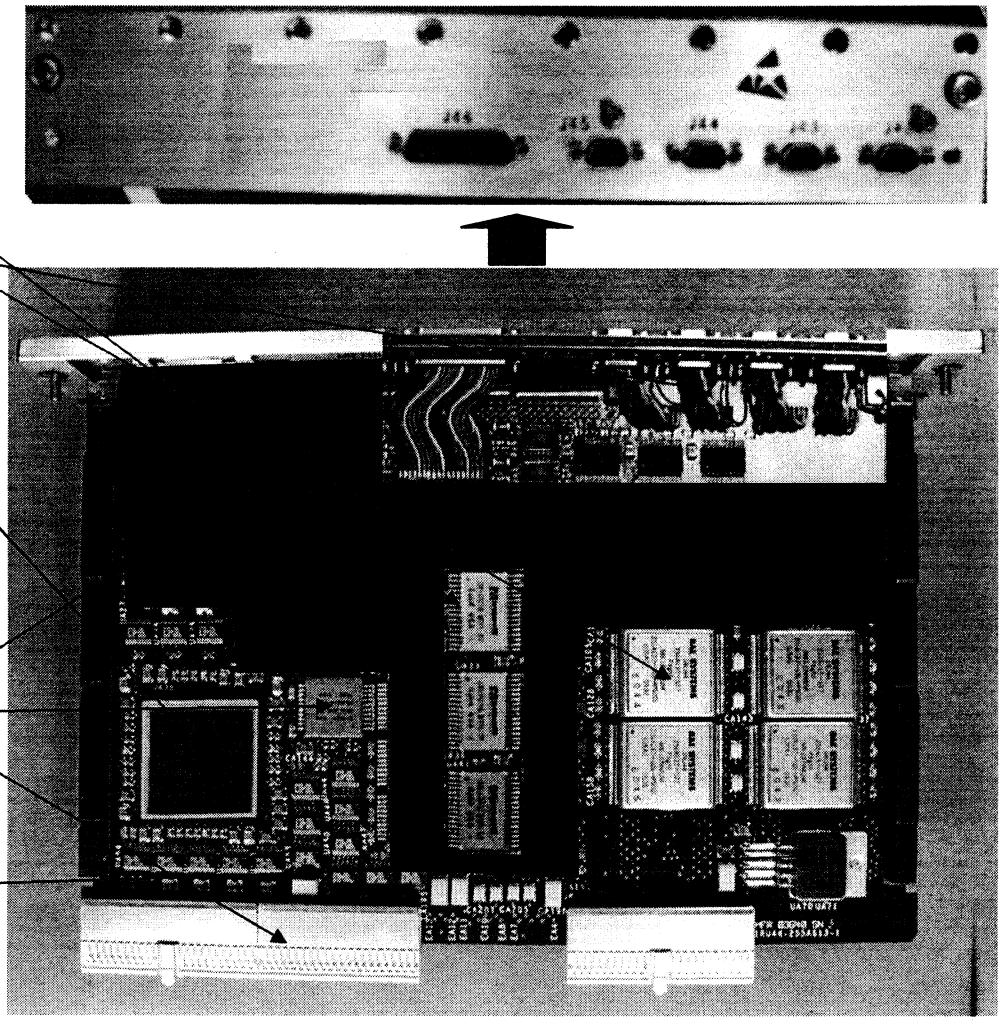
© 2007 BAE Systems - All rights reserved



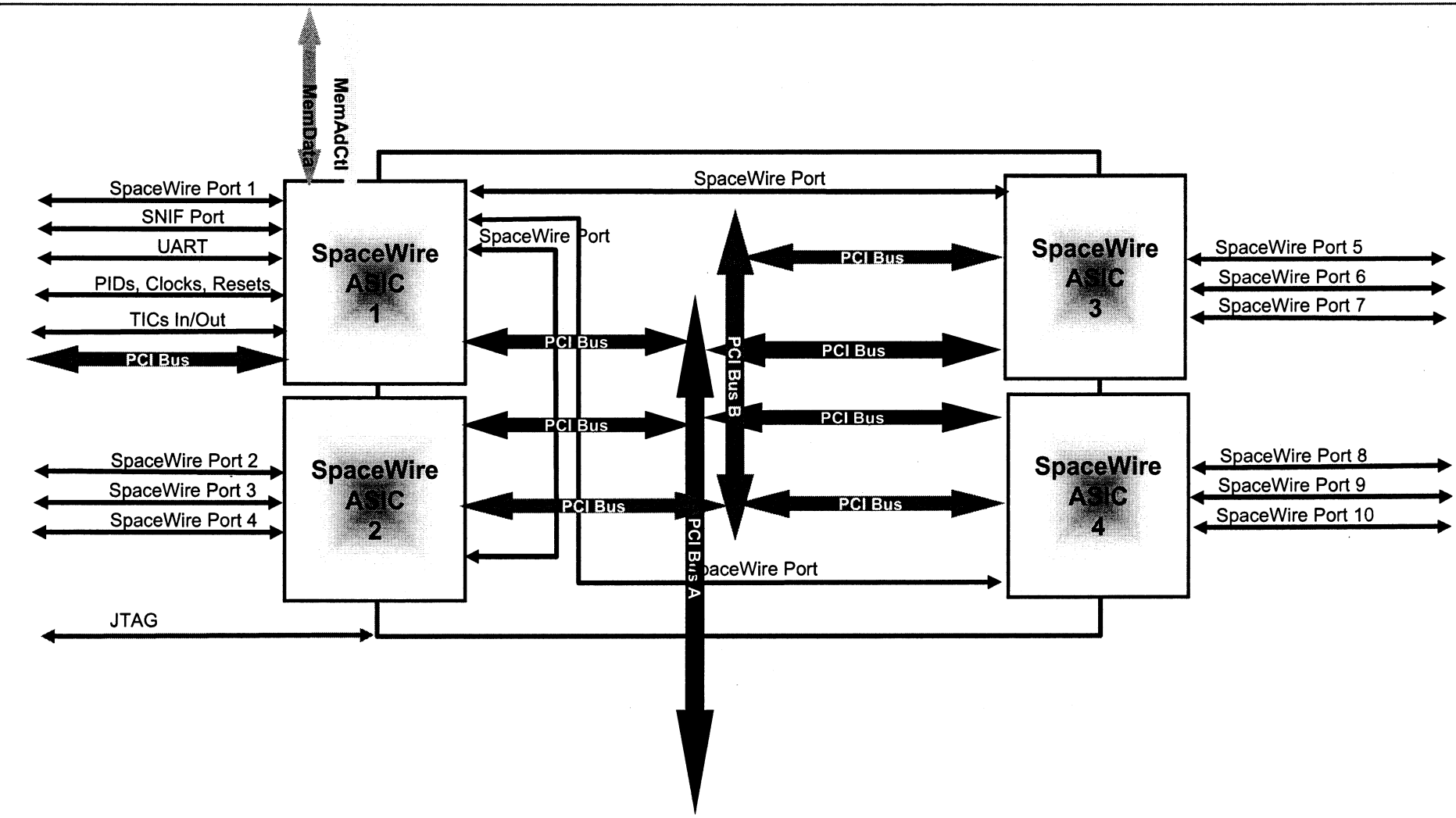
BAE SYSTEMS

4 Port SpaceWire 6U cPCI Evaluation Board

- 256 KB COTS EEPROM
- 8 MB BAE Lab SRAM
- 4 Port SpaceWire ASIC
  - 4 SpaceWire Ports
  - 6 Port Internal Router
  - DMA Controller, 16 MB SRAM
  - Embedded Microcontroller
  - UART
  - JTAG Input, Discretes and Timers
- 6U-160 CompactPCI
  - 32 bit 33 MHz PCI
  - Discretes
- 50 MHz Oscillator
- External Oscillator Input
- 5V and 3.3V Operation
  - 2.5V Regulator on Board
- Test Connector
  - UART, JTAG, Discretes, SNIF Port

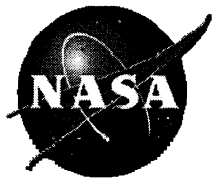


© 2007 BAE Systems - All rights reserved



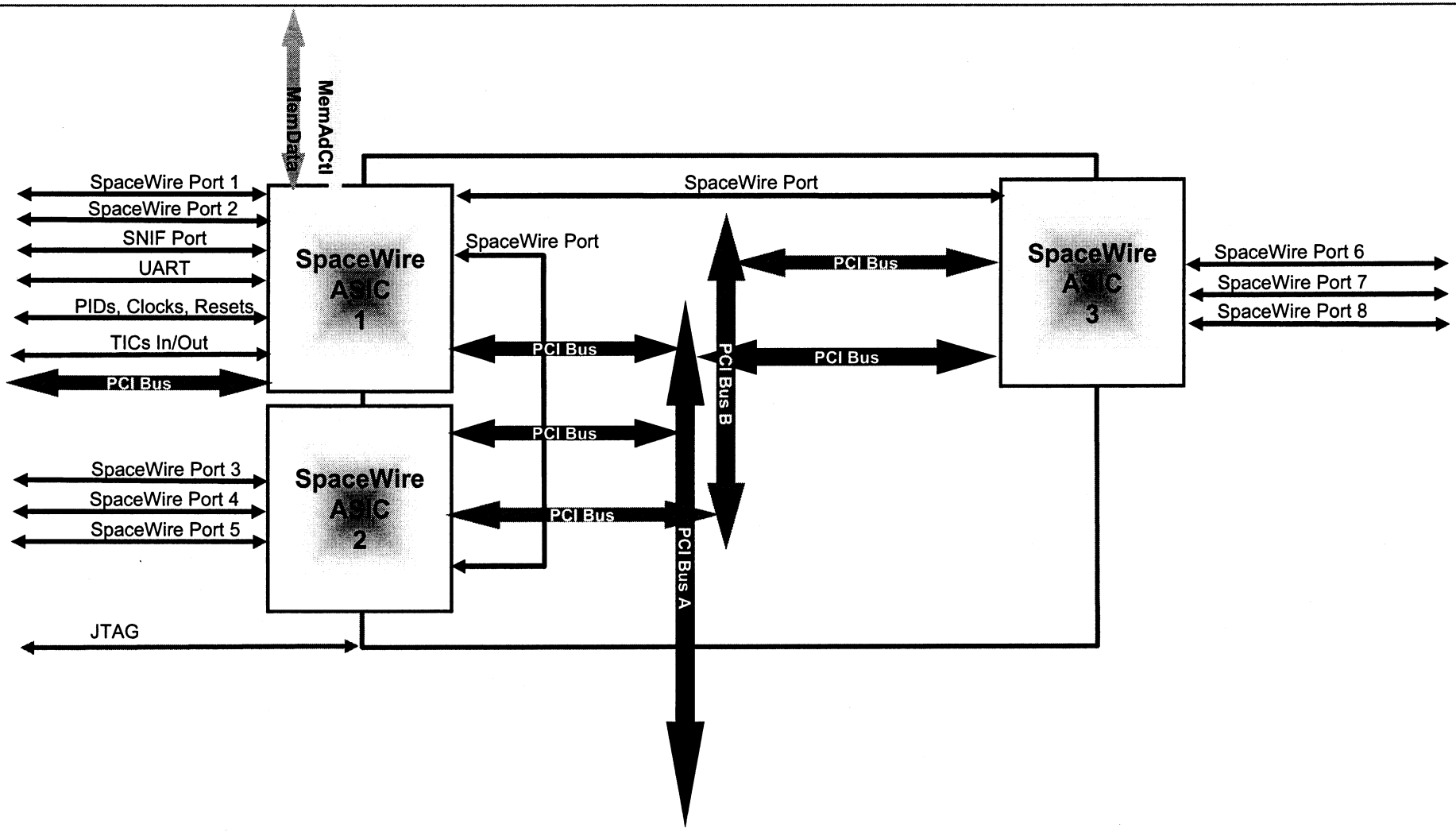
10 Port SpaceWire Hi Perf Router

© 2007 BAE Systems - All rights reserved

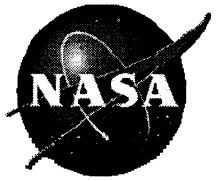


BAE SYSTEMS

8 Port SpaceWire Hi Perf Router



© 2007 BAE Systems - All rights reserved



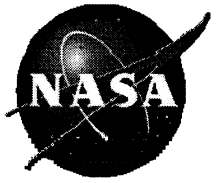
BAE SYSTEMS

Software – EMC Tool Chain Overview

- The EMC Tool Set allows the development of ANSI-C code targeted for the EMC. It consists of the following tools:
  - Lcc compiler targeted for the EMC (consists of a pre-processor and compiler)
  - EMC assembler built on top of the GNU assembler PPC "GASM"
  - The GNU linker to link EMC C and assembler code.
  - EMC Map to extract binary and debug information from output of GNU linker.
  - EMC Debugger for source level debugging of C & assembler code:
    - On target ASIC via JTAG
    - With EMC Simulator (simulation of EMC instruction set and memories)
- Toolset has been in use since 10/2005
- Previous Assembler-only toolset used since 1/2000 for RAD750 SUROMs

These tools enable applications to be built and simulated in high level language environments

© 2007 BAE Systems - All rights reserved



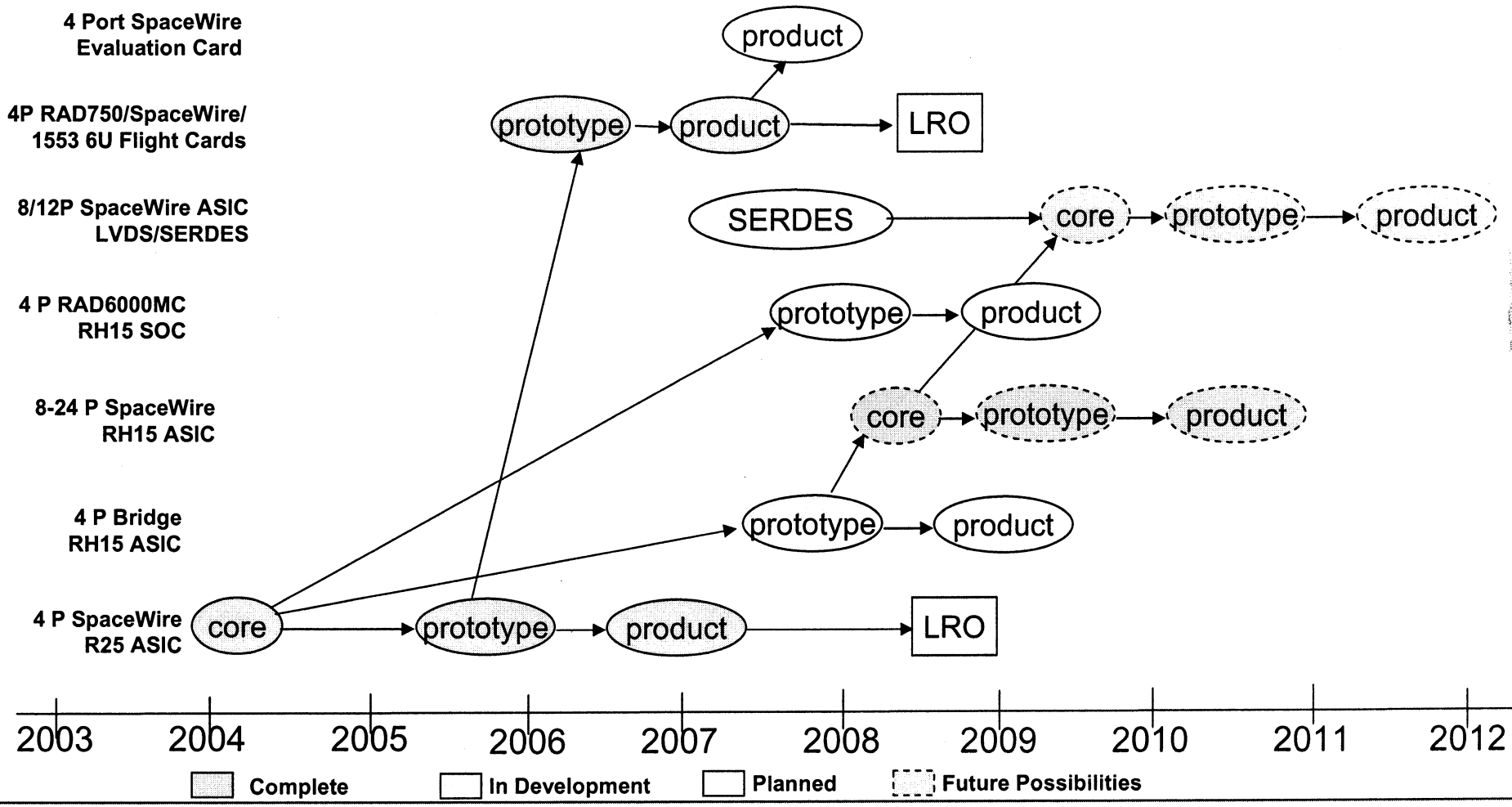
BAE SYSTEMS

Software Support for SpaceWire ASIC

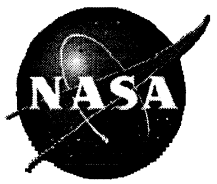
- Supporting software development
  - On-chip Embedded Microcontroller (EMC) controls transport layer
  - BAE Systems developed a C compiler for the EMC
  - GSFC is developing code for the EMC
- SpaceWire ASIC device driver written in C
  - RAD750 processor supports all functions via the PCI bus
  - Driver glues together software modules for Programmable Interrupt Discretes (PID), interrupt routing, PCI and address translation, DMA controller, the Router Interfaces (RIF), and SpaceWire router configuration
- Network routing layer on top of device driver
  - Provides queues in the system for incoming packets
  - Used by the LRO C&DH unit
- SpaceWire driver also written on on-chip EMC in C code
  - The EMC generates control block “descriptors” to partition large files into more easily transmittable pieces
  - Requires approximately 40% of EMC throughput capacity

© 2007 BAE Systems - All rights reserved

SpaceWire External Product Roadmap



© 2007 BAE Systems - All rights reserved



BAE SYSTEMS

Summary

- Existing SpaceWire Chip built from GSFC and BAE IP
- 4 Ports plus 7 port internal router
- Radiation Hardened and Flight Qualified – will fly in 2008
- Three Board Designs to Date with Evaluation Board by YE2007
- Various Performance Routers may be Implemented
- Full Roadmap for current and future products.

© 2007 BAE Systems - All rights reserved