Considerations for IC and Component Selection for Space Systems*

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**focus is on active components and not passive*

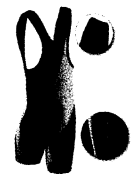
Outline

- **Semiconductors: The Evolution of ICs**
  - Availability and Technology
- **IC Selection Requirements - three fields of thought**
  - Technical – "The Good"
  - Programmatic – "The Bad"
  - Risk/Reliability – "The Ugly"
- **Reliability and Radiation**
- **Radiation Perspective - Four methods of selecting ICs for space systems**
  - Guaranteed hardness
  - Historical ground-based radiation data
  - Historical flight usage
  - Unknown assurance
- **Understanding Risk**
  - Risk trade space
    - Example: ASICs and FPGA – sample selection criteria
- **Conclusions**

To be presented by Kenneth LaBel at NASA Quality Leadership Forum (QLF), March 5-6, 2008, Cape Canaveral, FL.

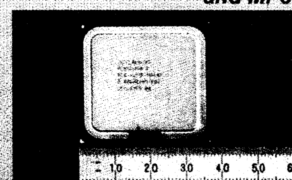
The Growth in IC Availability

- The semiconductor industry has seen an explosion in the types and complexity of devices that are available over the last several decades
  - The commercial market drives features
    - High density (memories)
    - High performance (processors)
    - Upgrade capability and time-to-market (FPGAs)
    - Wireless (RF and mixed signal)
    - Long battery life (Low-power CMOS)



Integrated Cycling Bib and MP3

Zilog Z80 Processor
circa 1978
8-bit processor



Intel 65nm Dual Core Pentium D Processor
circa 2007
Dual 64-bit processors

The Changes in Device Technology

- Besides increased availability, many changes have taken place in
  - Base technology,
  - Device features, and,
  - Packaging
- The table below highlights a few selected changes

Feature	circa 1990	circa 2007
Base technology	bulk CMOS/NMOS	CMOS with strained Si or SOI
Feature size	> 2.0 um	65 nm
Memory size - volatile (device)	256 kb	1 Gb
Processor speed	64 MHz	> 3 GHz
FPGA Gates	2k	> 1M
Package	DIP or LCC - 40 pins	FCBGA - 1500 balls
Advanced system on a chip (SOC) features	Cache memory	>Gbps Serial Link, Serdes, embedded processors, embedded memory

The Challenge for Selecting ICs for Space

- **Considerations since the "old days"**
  - **High reliability (and radiation tolerant) devices**
    - **Now a *very* small market percentage**
  - **Commercial "upscreening"**
    - **Increasing in importance**
    - **Measures reliability, does not enhance**
  - **System level performance and risk**
    - **Hardened "systems" not devices**

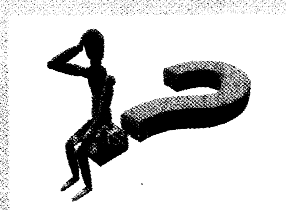
ADCs? *SerDes?* *SDRAM?* *Processor?* *ASICs?* *DSPs* *FPGAs?* *Flash?*

System Designer

Trying to meet high-resolution instrument requirements AND long-life

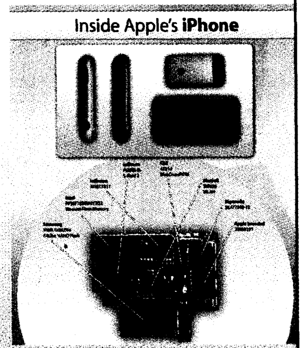
IC Selection Requirements

- **To begin the discussion, we shall review IC selection from three distinct and often contrary perspectives**
  - **Performance,**
  - **Programmatic, and,**
  - **Reliability.**
- **Each of these will be considered in turn, however, one must ponder all aspects as part of the *process***



Performance Requirements

- **Rationale**
  - Trying to meet science, surveillance, or other performance requirements
- **Personnel involved**
  - Electrical designer, systems engineer, other engineers
- **Usual method of requirements**
  - Flowdown from science or similar requirements to implementation
    - I.e., ADC resolution or speed, data storage size, etc…
- **Buzzwords**
  - MIPS/watt, Gbytes/cm^3, resolution, MHz/GHz, reprogrammable
- **Limiting technical factors beyond electrical**
  - Size, weight, and power (SWaP)



Performance
Inside a Apple iPhone™ player

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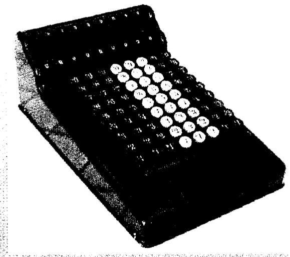
Programmatic Requirements and Considerations

- **Rationale**
  - Trying to keep a program on schedule and within budget
- **Personnel involved**
  - Project manager, resource analyst, system scheduler
- **Usual method of requirements**
  - Flowdown from parent organization or mission goals for budget/schedule
    - I.e., Launch date
- **Buzzwords**
  - Cost cap, GANTT/PERT chart, risk matrix, contingency
- **Limiting factors**
  - Parent organization makes final decision



Programmatics
A numbers game

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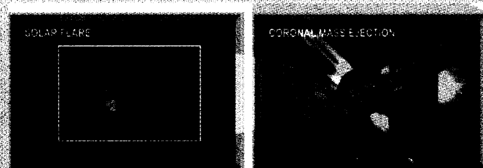
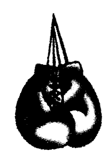
Risk Requirements

- Rationale
  - Trying to ensure mission parameters such as reliability, availability, operate-through, and lifetime are met
- Personnel involved
  - Radiation engineer, reliability engineer, parts engineer
- Usual method of requirements
  - Flowdown from mission requirements for parameter space
    - I.e., SEU rate for system derived from system availability specification
- Buzzwords
  - Lifetime, total dose, single events, device screening, "waivers"
- Limiting factors
  - Management normally makes "acceptable" risk decision

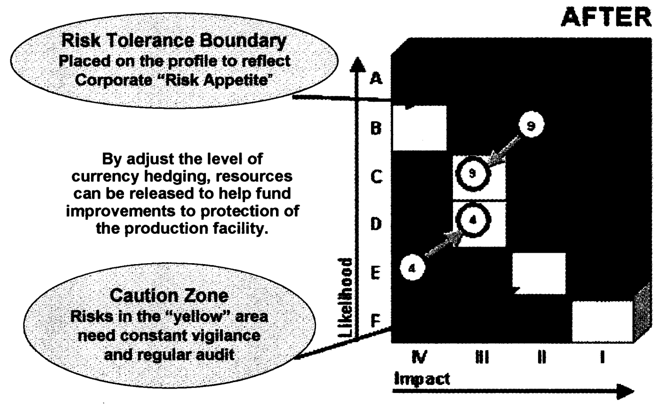


An Example "Ad hoc" Battle



- Mission requirement: High resolution image
  - Flowdown requirement: 14-bit 100 Msps ADC
    - Usually more detailed requirements are used such as ENOB or INL or DNL as well
  - Designer
    - Searches for available radiation hardened ADCs that meet the above requirements
    - Searches for commercial alternatives that could be upscreened
  - Manager
    - Trades the cost of buying Mil-Aero part requiring less aftermarket testing than a purely commercial IC
    - Worries over delivery and test schedule of the candidate devices
  - Radiation/Parts Engineer
    - Evaluates existing device data to determine reliability performance and additional test cost and schedule
- The best device? Depends on mission priorities

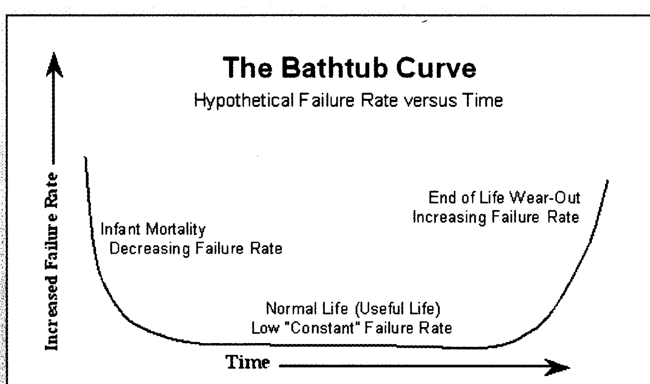
Traditional Risk Matrix



Likelihood Scale: A: Very High B: High C: Occasional D: Low E: Very Low F: Almost Impossible
Impact Scale: I: Catastrophic II: Critical III: Significant IV: Marginal

Reliability "versus" Radiation: Basic Electronics Reliability

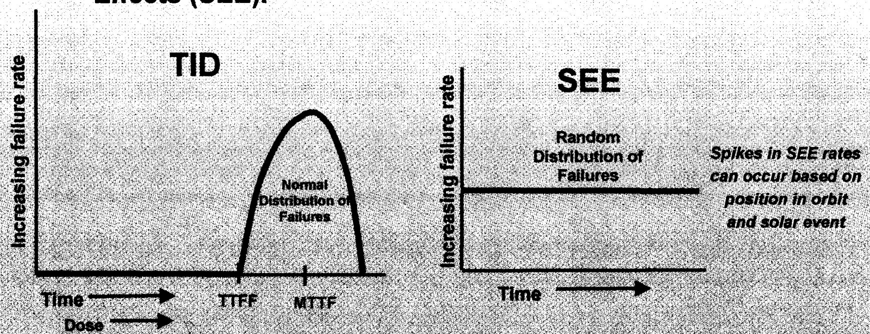
- **Reliability of electronics is viewed traditionally using a "bathtub" curve view of mean time to failure (MTTF)**
  - **This looks at both intrinsic (wearout) and extrinsic (infant mortality) failure modes**



Source: http://www.weibull.com/hotwire/issue21/hottopics21.htm

Radiation Effects and Reliability

- Radiation reliability is viewed differently than a normal reliability (bathtub) consideration
  - It is a mix of a MTTF (or Time to First Failure - TTFF) condition known as Total Ionizing Dose (TID) or Displacement Damage (DD) and a Mean Time Between Failures (MTBF) condition known as Single Event Effects (SEE).



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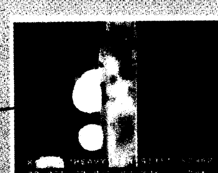
Radiation and Traditional IC Reliability: Are the two related?

- The short answer is yes
  - Radiation MTTF conditions can accelerate reliability wearout mechanisms either by eroding electrical signal margins or material damage
  - Radiation MTBF conditions also can impact long-term reliability
    - A single energetic particle, for example, can cause device failure instantaneously (such as with a gate rupture) or at a later time due to material damage.
- The methods of coupling the radiation-induced impacts into reliability calculations are limited
  - NEPP Program has a new effort to explore this coupling on state-of-the-art commercial Flash memories that are highly sought by flight programs

Latent damage from a single particle



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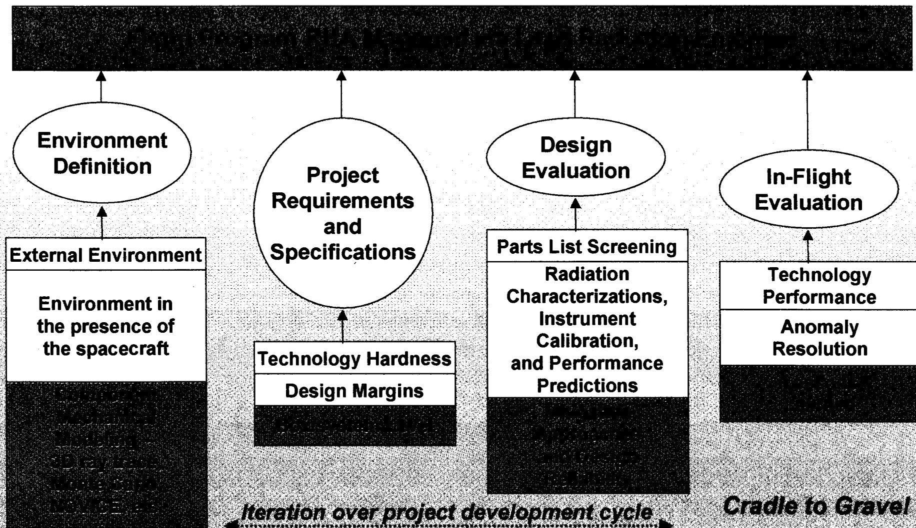
Flight Program:
Typical Radiation Hardness Assurance (RHA) Flow



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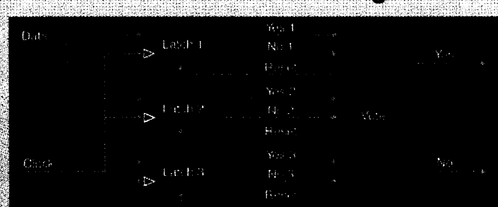
Radiation Perspective on IC Selection

- From the radiation perspective, ICs can be viewed as one of four categories.
  - Guaranteed hardness
    - Radiation-hardened by process (RHBP)
    - Radiation-hardened by design (RHBD)
  - Historical ground-based radiation data
    - Lot acceptance criteria
  - Historical flight usage
    - Statistical significance
  - Unknown assurance
    - New device or one with no data or guarantee



RHBD Voting Approach

http://www.aero.org/publications/crosslink/summer2003/08.html

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"Guaranteed" Radiation Tolerance

- A limited number of semiconductor manufacturers, either with fabs or fabless, will guarantee radiation performance of devices
  - Examples:
    - ATMEL, Honeywell, BAE Systems, Aeroflex
  - Radiation qualification usually is performed on either
    - Qualification test vehicle,
    - Device type or family member, or
    - Lot qualification
  - Some vendors sell "guaranteed" radiation tolerant devices by "cherry-picking" commercial devices coupled with mitigation approaches external to the die
- The devices themselves can be hardened via
  - Process or material (RHBP or RHBM),
  - Design (RHBD), or
  - Serendipity (RHBS)

Most radiation tolerant foundries use a mix of hardening approaches →

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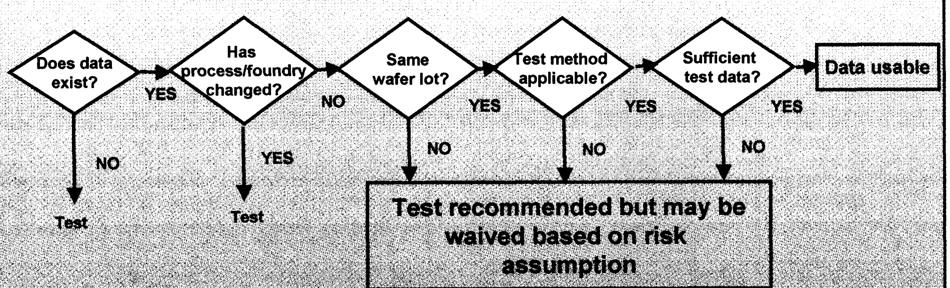
Archival Radiation Performance – Ground-based Data

- Reviewing existing ground radiation test data on a IC and it's application has been discussed previously
  - For example. Christian Poivey at NSREC Short Course in 2002
  - Using a "similar" device with data is risky, but sometimes considered (though not recommended)
- In general, the flow is shown below



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Archival Radiation Performance – Flight Heritage

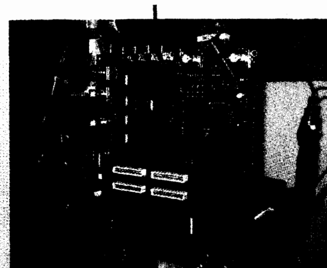
- Can we make use of parts with flight heritage and no ground data for new mission?
- Similar flow to using archival ground data exist, but consider as well
  - Statistical significance of the flight data
    - Environment severity?
    - Number of samples?
    - Length of mission?
  - Has storage of devices affected radiation tolerance or reliability?
  - And so forth
- This approach is rarely recommended by the radiation experts

Some heritage designs last better than others

IC's with no Guarantee or Heritage

- Radiation testing is required in the vast majority of cases
  - Testing complexities and challenges are discussed elsewhere (e.g., Swift during this short course, LaBel during the conference)
  - The true challenge is to gather sufficient data in a cost and schedule effective manner.
    - A backup plan should be made in case device fails to pass radiation criteria.
- Reliability testing has similar concerns

FPGA-based motherboard

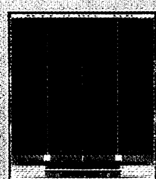


SDRAM mounted on a daughtercard

"Abandon all hope, ye' who enter here"

Is Testing Always Required?

- **Exceptions for testing may include**
  - **Operational**
    - **Ex., The device is only powered on once per orbit and the sensitive time window for a single event effect is minimal**
  - **Acceptable data loss**
    - **Ex., System level error rate may be set such that data is gathered 95% of the time. This is data availability. Given physical device volume and assuming every ion causes an upset, this worst-case rate may be tractable.**
  - **Negligible effect**
    - **Ex., A 2 week mission on a shuttle may have a very low TID requirement. TID testing could be waived.**



A FLASH memory may be acceptable without testing if a low TID requirement exists or not powered on for the large majority of time.

Understanding Risk

- **Risk for a mission falls in to the same topic areas as parts selection**
  - **Technical, programmatic, and reliability**
- **Technical risks**
  - **Relate to the circuit designs not being able to meet mission criteria such as jitter related to a long dwell time of a telescope on an object**
- **Programmatic risks**
  - **Relate to a mission missing a launch window or exceeding a budgetary cost cap which can lead to mission cancellation**
- **Reliability risks**
  - **Relate to mission meeting its lifetime and performance goals without premature failures or unexpected anomalies**
- ***Each mission must determine its priorities among the three risk types***



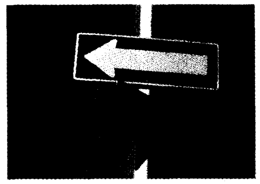
The Risk Trade Space –
Considerations for Device Selection (Incomplete)

- Cost and Schedule
  - Procurement
  - NRE
  - Maintenance
  - Qualification and test
- Performance
  - Bandwidth/density
  - SWaP
  - System function and criticality
  - Other mission constraints (ex., reconfigurability)
- System Complexity
  - Secondary ICs (and all their associated challenges)
  - Software, etc...
- Design Environment and Tools
  - Existing infrastructure and heritage
  - Simulation tools
- System operating factors
  - Operate-through for single events
  - Survival-through for portions of the natural environment
  - Data operation (example, 95% data coverage)
- Radiation and Reliability
  - SEE rates
  - Lifetime (TID, thermal, reliability,...)
  - "Upscreening"
- System Validation and Verification

Systems Engineering and Risk

- The determination of acceptability for device usage is a complex trade space
  - There is often more than one answer that's acceptable
- A more omnidirectional approach is taken to evaluate the various risks
  - Each of the three factors may be assigned weighted priorities
    - The systems engineer is often the "person in the middle" evaluating the technical/reliability risks and working with management to determine acceptable risk levels

Example: Considerations for Selecting a "Custom" Device



- **Three basic device type options**
  - Custom ASIC (CA)
    - Also called standard cell or just ASIC
    - Essentially a fully-custom design IC
  - Structured ASIC (SA)
    - Newer device that is a semi-custom design using built-in functional blocks that are interconnected for a user's design by the device manufacturer
  - Field Programmable Gate Array (FPGA)
    - One-time or reprogrammable interconnecting of logic performed by the user or can be done in-circuit (reprogrammable options)
- **These class of devices now have so much functionality that they can be classified as system on a chip (SOC)**
- **We will use the three discussed selection criteria for this example.**

Sample System Implementation for the Three Styles of FPGAs

Increasing System Complexity

One-time Programmable (OTP) — FPGA

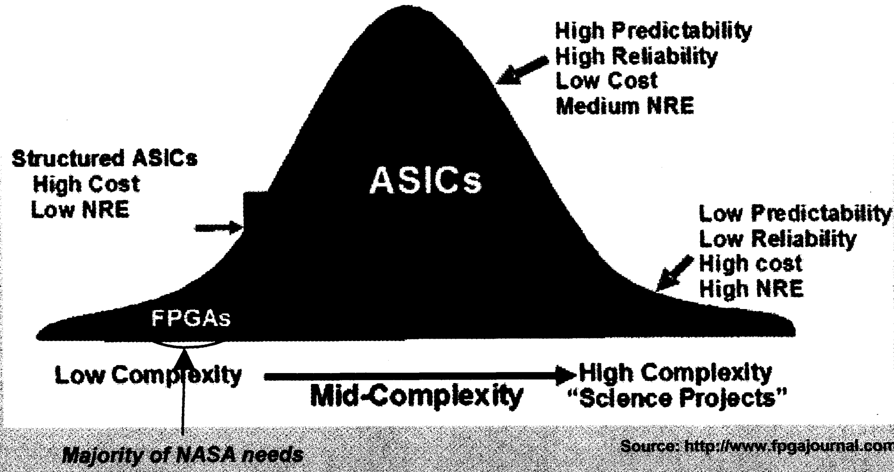
Non-volatile Reprogrammable (Flash) — Circuits to interface between FPGA and ground for new configuration uploads — FPGA

SRAM-based — Circuits to interface between FPGA and ground for new configuration uploads — Watchdog/controller — FPGA — Non-volatile memory (NVM) – holds configuration of FPGA

Radiation tolerant/hardened options available in all types; Some are "harder" than others

The Trade Space Curve for Performance

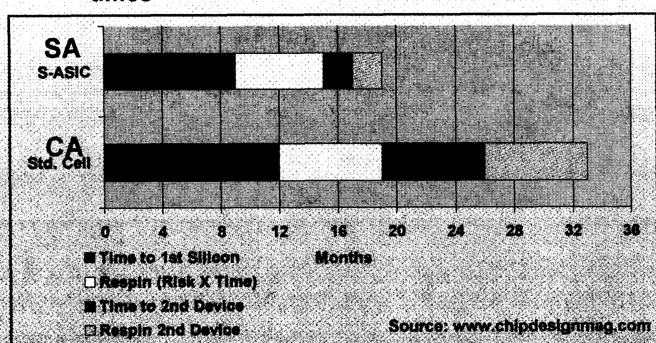
- **Application-specific trade-offs are often made based on the design complexity of the application requirements.**
  - ***Note: FPGAs and SAs are moving to the right as semiconductor processes scale to smaller transistor feature***



Source: http://www.fpgajournal.com

Programmatics: Development Schedule

- **Example of a time to market (TTM) for commercial options**
  - **Assumptions**
    - **90nm technology, < 1Mgate device**
  - **SA is ~1/2 TTM of a CA**
  - **FPGAs are likely < ½ of the SA TTM**
  - **Note: This does not consider reliability or radiation qualification times**

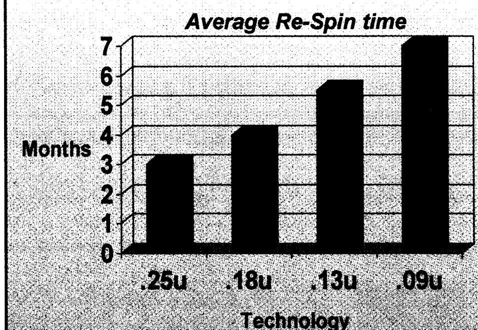


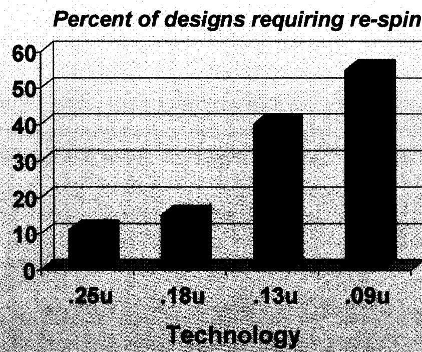
Source: www.chipdesignmag.com

Comparing SA vs. CA for TTM

Programmatics:
What if the first design is incorrect?

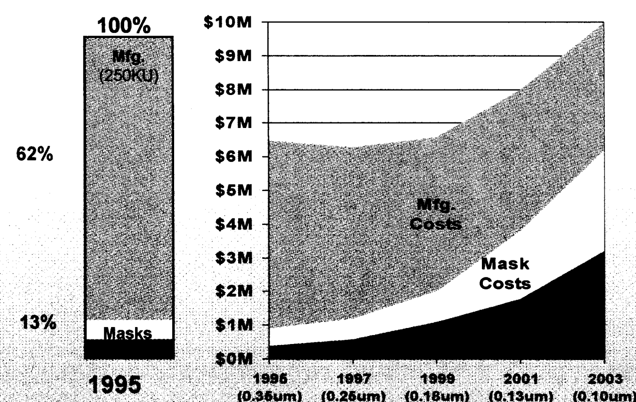
- As digital devices pack more bits into the same physical space (i.e., technology feature size is shrinking), more designs require a “second pass” or re-spin.
- Even worse, the time it takes for this re-spin has increased





Source: www.chipdesignmag.com

Programmatics: Development Cost



Assumptions: 6M-70M transistors, 3 mask spins, 250K Units, transistor costs and productivity projected from the ITRS

Graphic from MIPS Technologies "The Coming Reality for SOC Designers" by John Bourgoin

- Overall product development costs are increasing: design, mask, and manufacturing
  - However, the percentage of product cost for both design and masks (>$1M for 90nm!) are also increasing
    - Implies cost effectiveness of minimizing masks and design re-spin costs (advantage FPGAs and SAs)

Selection Criteria: Radiation and Reliability

- **While there is no "generic" answer for radiation tolerance and reliability levels in the trade, there are numerous considerations such as**
  - What is known of the process radiation tolerance?
    - Was process/device radiation qualification sufficient for planned design or application?
      - Library? Cells? Speed? Etc...
    - Is the process reliable and achieving good yield?
      - High-volume commercial fab vs. low-volume niche fab?
    - Are there lot-specific or application-specific concerns?
  - Is there a specific performance requirement such as reconfigurability or ultra-low power that forces a non-radiation tolerant device selection?
    - How does a fault-tolerant system architecture enter the equation?
  - How testable is the design/device?
- **As has become more evident, trade spaces are much more complex than "just" an IC**

Current Radiation Hardening Considerations

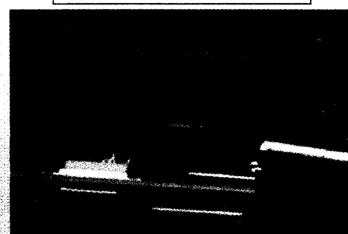
Category	Generic CMOS Technology	CA	SA	FPGA
RH Availability	Poor	Niche vendors for RH; Commercial would rely on RHBS and RHBD	Niche vendors – none currently available, but several vendors are developing	Limited, but new developments underway
TID	RHBS; improving with scaling	RHBS, RHBD, RHBP	RHBS, RHBP, partial RHBD	RHBS
SEE	RHBS – not; increasing sensitivity; SOI?	RHBS, RHBD, RHBP (substrate)	RHBS, RHBD partial, RHBP (substrate)	RHBS
Notes	IP: Limited RH IP available; Commercial IP? Commercial manufacturers working soft error rate (SER) issues	RH levels can be "tuned" via RHBD or RHBP; Difficult for radiation testing	Circuit tiles can incorporate mitigation options	External and internal SEE mitigation (TMR, scrubbing, reconfiguration, etc) for logic and configuration

Related SOC Radiation and Reliability Considerations

New Silicon
- -90nm CMOS
- -new materials

New Connectors
- -higher-speed, lower noise
- -serial/parallel

New Board Material
- -thermal coefficients
- -material interfaces



New Architectures
- -new interconnects
- -new power distribution
- -new frequencies

New Workmanship
- -inspection, lead free
- -stacking, double-sided
- -signal integrity

New Design Flows/Tools
- -programming algorithms, application
- -design rules, tools, simulation, layout
- -hard/soft IP instantiation

New Package
- -Inspection
- -Lead free

BEWARE! Support circuitry (power, memory, IO, etc) can often be limiting factor for system reliability and radiation performance

Summary of Generalized Features – ASICs versus FPGAs

Category	SRAM - FPGA	OTP FPGA	SA	CA
NRE	Low	Low	Med	High
Production Cost	High	High	Med	High
Risk	Low	Low	Med	High
Development Span (TTM)	Low	Low	Med	High
Electrical Performance	Low	Low	Med	High
Density/Capacity	Low	Low	Med	High
Power Consumption	High	Med	Med	Low
Flexibility	High	Med	Med	Low
Radiation Performance	Low	Med	High	High

Conclusions

- In this talk, we have presented considerations for selection of ICs for space systems
  - Technical, programmatic, and risk-oriented
    - As noted, every mission may view the relative priorities between the considerations differently
- We have also noted a specific type of example, that of custom to semi-custom devices
- As seen below, every decision type may have a process.
  - It's all in developing an appropriate one for your application.

Five stages of Consumer Behavior

http://www-rohan.sdsu.edu/~renglish/370/notes/chapt05/