NASA Electronic Parts and Packaging (NEPP) Program

http://nepp.nasa.gov

Kenneth A. LaBel
and Michael J. Sampson
Co-Managers NEPP Program

NEPP Mission

- The NEPP mission is to provide guidance to NASA for the selection and application of microelectronics technologies, to improve understanding of the risks related to the use of these technologies in the space environment and to ensure that appropriate research is performed to meet NASA mission assurance needs.

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
NEPP Overview

- NEPP supports all of NASA for >15 years
  - 7 NASA Centers and JPL actively participate
- The NEPP Program focuses on the reliability aspects of electronic devices
  - Integrated circuits such as a processor in a computer or optical components such as might be used in a communication link.
- There are three principal aspects of this reliability:
  - Lifetime, inherent failure and design issues related to the electronic parts technology and packaging,
  - Effects of space radiation and the space environment on these technologies, and
  - Creation and maintenance of the assurance support infrastructure required for mission success.

NEPP interests span electronic parts technologies

- Emerging semiconductors and packages
- Commonly-used "mission building blocks"
- New state-of-the-art commercial products

NEPP is multi-disciplinary

- Including radiation, materials, test, experimentation, process and specification experts across NASA and its partners

NEPP has close, cooperative and long-standing relationships with government and non-government entities worldwide

NEPP provides unique capabilities within NASA

- Evaluate technologies in advance of mission needs
- Provide assistance with risk management of technology insertion

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
Sample challenges for radiation testing of “simple” memories

<table>
<thead>
<tr>
<th>Category</th>
<th>1997</th>
<th>2007</th>
<th>Implication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>SRAM</td>
<td>SDRAM DDR2</td>
<td>More complex architecture</td>
</tr>
<tr>
<td>Feature Size</td>
<td>&gt;=1.0 um</td>
<td>&lt;=90 nm</td>
<td>Miniscule target</td>
</tr>
<tr>
<td>Density</td>
<td>4 Mb</td>
<td>1 Gb</td>
<td>Large tester data storage; Difficult data analysis</td>
</tr>
<tr>
<td>Speed</td>
<td>&lt;50 MHz</td>
<td>&gt;1 GHz</td>
<td>Drives challenges for at-speed test and data collection; transient propagation; thermal/mechanical challenges</td>
</tr>
<tr>
<td>Package</td>
<td>DIP or LCC</td>
<td>TSOP or FBGA</td>
<td>Difficult access for heavy ion and high-temperature testing</td>
</tr>
<tr>
<td>Notes</td>
<td>Mostly ceramic, simple operating modes</td>
<td>Plastic, flip-chip, many operating modes</td>
<td>Complex signatures for error and data analysis; “Unknown” features</td>
</tr>
</tbody>
</table>

NEPP Has a Wide Range of FY08 Efforts

- A few samples follow highlighting work on state-of-the-art technologies
  - Keys to missions in early to mid design phases
- NEPP’s sister program, NEPAG, focuses on challenges more relevant to the missions that are “bending metal”
CMOS Scaling – New Challenges

Modeling, simulation, device physics understanding of failure modes, data gathering and analysis, and reliability prediction
- Foundation for technology insertion of the next generation of scaled microelectronics.

CMOS Scaling Reliability
NEPP POC: Mark White, JPL

Sample NEPP Technology Areas

Leveraging Rad-Hard by Design (RHBD) Efforts
Evaluating state-of-the-art memory
Advanced Electronics Packaging

SDRAM
Flash

Sample CMOS Scaling 90nm Transistor Test

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
Sample Efforts on Advanced Electronic Technologies

NEPP POC for embedded actives: Linda Del Castillo, JPL

NEPP POC for extreme temperature: Richard Patterson, GRC

Improving understanding of risk and test methods
Can we test anything completely?

“Complete” Single Event Effect (SEE) Radiation Test Matrix
for a commercial SDRAM (does not include temperature variations)

<table>
<thead>
<tr>
<th></th>
<th>Number of Samples</th>
<th>Modes of Operation</th>
<th>Test Patterns</th>
<th>Frequencies of Operation</th>
<th>Power Supply Voltages</th>
<th>Ions</th>
<th>Hours per Ion per Test Matrix Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>68</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 3              |                   |                    |               |                          |                        |      | 66096                             |
| 3              |                   |                    |               |                          |                        |      | 2754                              |
| 3              |                   |                    |               |                          |                        |      | 7.54                               |

Implications:
- Test planning and performance is now application-specific focused
- Existing datasets must be viewed in the same light (application)

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
NEPP and FPGAs -
A Sampling of Challenges

Can we “qualify” the system without breaking the bank?

New Silicon
-90nm CMOS
-new materials

New Board Material
-thermal coefficients
-material interfaces

New Connectors
-higher-speed, lower noise
-serial/parallel

New Workmanship
-inspection, lead free
-stacking, double-sided
-signal integrity

New Architectures
-new interconnects
-new power distribution
-new frequencies

New Design Flows/Tools
-programming algorithms, application
-design rules, tools, simulation, layout
-hard/soft IP instantiation

New Package
-inspection
-Lead free

FPGA Insertion Processes: Viewed as a System

FPGA Insertion Process

Foundry
-Technology
-Yield
-Quality Program

Vendor
-Design
-Test
-Quality Program

User
-Application
-Design Process
-Screening

Successful insertion requires significant contributions from all three areas.

NEPP POC:
Doug Sheldon, JPL

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
FPGAs: Radiation Testing, Test Method Development, Data Interpretation and User Insertion

NEPP POCs: Melanie Berg, MEI/GSFC
Greg Allen, JPL

FPGAs: Packaging and Support Devices

Radiation and Reliability of FLASH NVMs
NEPP POCs: Doug Sheldon, JPL (reliability)
Tim Oldham, PerotSystems/GSFC (radiation)

Device Packaging
NEPP POCs: Reza Ghaffarian, JPL
Jill Mohammed, GSFC

Radiation Effects on Low-Voltage Regulators
NEPP POC: Ken LaBel, GSFC (acting)

Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).
NEPP Mission

The NEPP mission is to provide guidance to NASA for the selection and application of microelectronics technologies, to improve understanding of the risks related to the use of these technologies in the space environment and to ensure that appropriate research is performed to meet NASA mission assurance needs.

NEPP Overview

- NEPP supports all of NASA for >15 years
  - Seven NASA Centers and JPL actively participate
- The NEPP Program focuses on the reliability aspects of electronic devices
  - Integrated circuits such as a processor in a computer or optical components such as might be used in a communication link.
- There are three principal aspects of this reliability:
  - Lifetime, inherent failure and design issues related to the electronic parts technology and packaging;
  - Effects of space radiation and the space environment on these technologies;
  - Creation and maintenance of the assurance support infrastructure required for mission success.
- NEPP interests span electronic parts technologies
  - Emerging semiconductors and packages
  - Commonly used "mission building blocks"
  - New state-of-the-art commercial products
- NEPP is multi-disciplinary
  - Including radiation, materials, test, experimentation, process and specification experts across NASA and its partners
- NEPP has close, cooperative and long-standing relationships with government and non-government entities worldwide
- NEPP provides unique capabilities within NASA
  - Evaluate technologies in advance of mission needs
  - Provide assistance with risk management of technology insertion

Sample challenges for radiation testing of "simple" memories

<table>
<thead>
<tr>
<th>Category</th>
<th>1997</th>
<th>2007</th>
<th>Implication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>SRAM</td>
<td>SDRAM DDR2</td>
<td>More complex architecture</td>
</tr>
<tr>
<td>Feature Size</td>
<td>&gt;=1.0 μm</td>
<td>&lt;=90 nm</td>
<td>Miniscule target</td>
</tr>
<tr>
<td>Density</td>
<td>4 Mb</td>
<td>1 Gb</td>
<td>Large tester data storage; difficult data analysis</td>
</tr>
<tr>
<td>Speed</td>
<td>&lt;50 MHz</td>
<td>&gt;1 GHz</td>
<td>Drives challenges for at-speed testing and data collection; transient propagation; thermal/mechanical challenges</td>
</tr>
<tr>
<td>Package</td>
<td>DIP or LCC</td>
<td>TSOP or FBGA</td>
<td>Difficult access for heavy ion and high-temperature testing</td>
</tr>
<tr>
<td>Notes</td>
<td>Mostly ceramic, simple operating modes</td>
<td>Plastic, flip-chip, many operating modes</td>
<td>Complex signatures for error and data analysis; &quot;Unknown&quot; features</td>
</tr>
</tbody>
</table>
NEPP Has a Wide Range of FY08 Efforts

- A few samples follow highlighting work on state-of-the-art technologies
  - Keys to missions in early to mid design phases
- NEPP's sister program, NEPAG, focuses on challenges more relevant to the missions that are "bending metal"

CMOS Scaling
New Challenges

Sample Efforts on Advanced
Electronic Technologies

Other Sample NEPP
Technology Areas

Improving Understanding of
Risk and Test Methods

Can we test anything completely?

"Complete" Single Event Effect (SEE) Radiation Test Matrix for a commercial SDRAM (does not include temperature variations)

<table>
<thead>
<tr>
<th>3</th>
<th>Number of Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>68</td>
<td>Modes of Operation</td>
</tr>
<tr>
<td>4</td>
<td>Test Patterns</td>
</tr>
<tr>
<td>3</td>
<td>Frequencies of Operation</td>
</tr>
<tr>
<td>3</td>
<td>Power Supply Voltages</td>
</tr>
<tr>
<td>3</td>
<td>Hours per Ion per Test Matrix Point</td>
</tr>
</tbody>
</table>

66086 Hours
2754 Days
7.84 Years

Implications:
- Test planning and performance is now application specific instead
- Existing data sets must be viewed in the same light (application)
NEPP and FPGAs - A Sampling of Challenges
Can we "qualify" without breaking the bank?

- New Connectors
  - higher-speed, lower noise
  - serial/parallel
- New Silicon
  - 45nm CMOS
  - new materials
- New Architectures
  - new interconnects
  - new power distribution
  - new frequencies
- New Design/Process Tools
  - programming algorithms, application
  - design rules, simulation, layout
- New Workmanship
  - inspection, test flow
  - stacking, double-sided
  - signal integrity
- New Board Material
  - thermal coefficients
  - material interfaces
- New Packaging
  - inspection, test flow

FPGA Insertion Processes: Viewed as a System

FPGA Insertion Process

- Foundry
  - Technology
  - Yield
  - Quality Program
- Vendor
  - Design
  - Test
  - Quality Program
- User
  - Application
  - Design Process
  - Screening

Successful insertion requires significant contributions from all three areas.

FPGAs: Radiation Testing, Test Method Development, Data Interpretation and User Insertion

FPGAs: Packaging and Support Devices

Panel 3 of "NASA Electronic Parts and Packaging (NEPP) Program" Industrial Exhibit Poster to be presented by Kenneth LaBel at several conferences throughout 2008 (including CMSE, HEART, SEESYM, NSREC, and RADEX).