Ka-Band Transponder for Deep-Space Radio Science

A one-page document describes a Ka-band transponder being developed for use in deep-space radio science. The transponder receives in the Deep Space Network (DSN) uplink frequency band of 34.2 to 34.7 GHz, transmits in the 31.8- to 32.3 GHz DSN downlink band, and performs regenerative ranging on a DSN standard 4-MHz ranging tone subcarrier phase-modulated onto the uplink carrier signal. A primary consideration in this development is reduction in size, relative to other such transponders.

The transponder design is all-analog, chosen to minimize not only the size but also the number of parts and the design time and, thus, the cost. The receiver features two stages of frequency down-conversion. The receiver locks onto the uplink carrier signal. The exciter signal for the transmitter is derived from the same source as that used to generate the first-stage local-oscillator signal. The ranging-tone subcarrier is down-converted along with the carrier to the second intermediate frequency, where the 4-MHz tone is demodulated from the composite signal and fed into a ranging-tone-tracking loop, which regenerates the tone. The regenerated tone is linearly phase-modulated onto the downlink carrier.

This work was done by Matthew S. Dennis, Narayan R. Mysoor, William M. Folkner, Ricardo Mendoza, and Jaikrishna Venkatesan of United Space Alliance for Johnson Space Center. Further information is contained in a TSP (see page 1).

Replication of Space-Shuttle Computers in FPGAs and ASICs

A document discusses the replication of the functionality of the onboard space-shuttle general-purpose computers (GPCs) in field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs). The purpose of the replication effort is to enable utilization of proven space-shuttle flight software and software-development facilities to the extent possible during development of software for flight computers for a new generation of launch vehicles derived from the space shuttles. The replication involves specifying the instruction set of the central processing unit and the input/output processor (IOP) of the space-shuttle GPC in a hardware description language (HDL).

The HDL is synthesized to form a “core” processor in an FPGA or, less preferably, in an ASIC. The core processor can be used to create a flight-control card to be inserted into a new avionics computer. The IOP of the GPC as implemented in the core processor could be designed to support data-bus protocols other than that of a multiplexer interface adapter (MIA) used in the space shuttle. Hence, a computer containing the core processor could be tailored to communicate via the space-shuttle GPC bus and/or one or more other buses.

This work was done by Russell Roder and Eliezer Ahronovich of Goddard Space Flight Center and Milton C. Davis III of Purdue University. Further information is contained in a TSP (see page 1). GSC-14845-1

Demisable Reaction-Wheel Assembly

A document discusses work that obtains a low-dimensional model that captures both temporal and spatial flow by constructing spatial and temporal four-mode models for two classic flow problems. The models are based on the proper orthogonal decomposition at two reference Reynolds numbers. Model predictions are made at an intermediate Reynolds number and compared with direct numerical simulation results at the new Reynolds number.

This work was done by Virginia Kalb of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15130-1

Spatial and Temporal Low-Dimensional Models for Fluid Flow