WRATS Integrated Data Acquisition System

This new system substantially improves tiltrotor aeroelastic test methods.

NASA Langley Research Center, Hampton, Virginia

The Wing and Rotor Aeroelastic Test System (WRATS) data acquisition system (DAS) is a 64-channel data acquisition display and analysis system specifically designed for use with the WRATS 1/5-scale V-22 tiltrotor model of the Bell Osprey. It is the primary data acquisition system for experimental aeroelastic testing of the WRATS model for the purpose of characterizing the aeromechanical and aeroelastic stability of prototype tiltrotor configurations. The WRATS DAS was also used during aeroelastic testing of Bell Helicopter Textron's Quad-Tiltrotor (QTR) design concept, a test which received international attention. The LabVIEW-based design is portable and capable of powering and conditioning over 64 channels of dynamic data at sampling rates up to 1,000 Hz. The system includes a 60-second circular data archive, an integrated model swashplate excitation system, a moving block damping application for calculation of whirl flutter mode subcritical damping, a loads and safety monitor, a pilot-control console display, data analysis capabilities, and instrumentation calibration functions. Three networked computers running custom-designed LabVIEW software acquire data through National Instruments data acquisition hardware.

The aeroelastic model (see figure) was tested with the DAS at two facilities at NASA Langley, the Transonic Dynamics Tunnel (TDT) and the Rotorcraft Hover Test Facility (RHTF). Because of the need for seamless transition between testing at these facilities, DAS is portable. The software is capable of harmonic analysis of periodic time history data, Fast Fourier Transform calculations, power spectral density calculations, and on-line calibration of test instrumentation. DAS has a circular buffer archive to ensure critical data is not lost in event of model failure/incident, as well as a sample-and-hold capability for phase-correct time history data. The system has an interface to drive TDT text overlay display video monitors and an interface to trigger digital video recording

Wing and Rotor Aeroelastic Test System 9 (WRATS).

WRARTS DAS front panel graphical user interface.

The **WRATS** model was tested with the DAS at the Transonic Dynamics Tunnel at NASA Langley. Shown below is the LabVIEW-based WRATS DAS front-panel graphical user interface.

(DVR) systems.

DAS uses NI SCXI signal-conditioning hardware to power, amplify, and anti-alias-filter the 64 channels of sample-and-hold time-correlated data at sample rates up to 1,000 Hz. The WRATS data system as a whole maximizes efficient tiltrotor aeroelastic test practices at the TDT by allowing seamless integration of model swashplate stik-stir excitation commands with data acquisition capabilities and post-point damping analysis. Following analysis, the system reports key results to a MATLAB-based data logging system for archiving, organization, and reporting of test results.

In addition to test efficiency, the system improves the safety-of-flight environment of the test process by calculating and monitoring critical model loads, stress, and parameters in real time during testing. In the event of unsafe conditions or loads, audible, synthesized voice alerts are provided to the test crew in addition to visual display cues on the WRATS Loads Monitor displays, which are networked with the WRATS data system.

This work was done by David J. Piatak of Langley Research Center. Further information is contained in a TSP (see page 1). LAR-17486

Breadboard Signal Processor for Arraying DSN Antennas

The processors can be used to combine signals in interferometry and telecommunications.

NASA's Jet Propulsion Laboratory, Pasadena, California

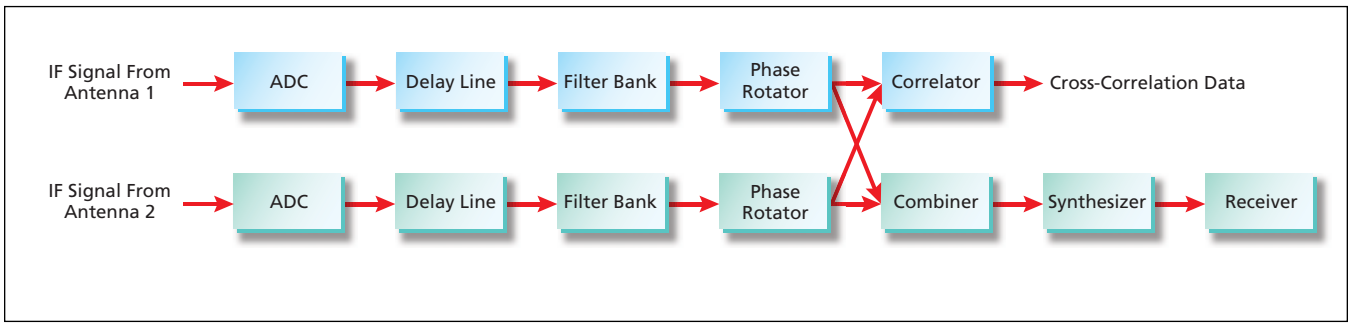
A recently developed breadboard version of an advanced signal processor for arraying many antennas in NASA's Deep Space Network (DSN) can accept inputs in a 500-MHz-wide frequency band from six antennas. The next breadboard version is expected to accept inputs from 16 antennas, and a following developed version is expected to be designed according to an architecture that will be scalable to accept inputs from as many as 400 antennas. These and similar signal processors could also be used for combining multiple wide-band signals in non-DSN applications, including very-long-baseline interferometry and telecommunications.

This signal processor performs functions of a wide-band FX correlator and a beam-forming signal combiner. [The term "FX" signifies that the digital samples of two given signals are fast Fourier transformed (F), then the fast Fourier transforms of the two signals are multiplied (X) prior to accumulation.] In this processor, the signals from the various antennas are broken up into channels in the frequency domain (see figure). In each frequency channel, the data from each antenna are correlated against the data from each other antenna; this is done for all antenna baselines (that is, for all antenna pairs). The results of the correlations are used to obtain calibration data to align the antenna signals in both phase and delay. Data from the various antenna frequency channels are also combined and calibration corrections are applied. The frequency-domain data thus combined are then synthesized back to the time domain for passing on to a telemetry receiver.

The inputs from the antennas are preprocessed signals in an intermediate-frequency (IF) band from 700 to 1,200 MHz. High-speed commercial off-the-shelf analog-to-digital-converter (ADC) integrated circuits sample the inputs to 8 bits at a rate of 1,280 MHz. The sample data are transmitted via fiber-optic links to signal-processing boards in a commercial high-performance, modular, digital chassis that conforms to an industry standard known as the Advanced Telecommunications Architecture (ATCA). The physical and electrical characteristics of an ATCA chassis are governed by a specification known as PICMG 3.0 (wherein "PICMG" signifies the PCI Industrial Computer Manufacturers Group and "PCI" signifies peripheral component interface).

Mounted on each signal-processing board are four field-programmable gate array (FPGA) integrated-circuit chips that are interconnected both on the board and through the ATCA back plane by serial links capable of operating at speeds up to 2.5 Gb/s. Each FPGA chip can be programmed, independently of the other FPGA chips, to perform such specific functions as implementing filter banks to convert time-domain data to frequency-domain data in frequency channels, wide- and narrow-band cross-correlation, combining of the individual frequency channels, and implementing synthesizing filter banks for converting frequency-domain data back to the time domain.

This work was done by Andre Jongeling, Elliott Sigman, Kumar Chandra, Joseph Trinh, Melissa Soriano, Robert Navarro, Stephen Rogstad, Charles Goodhart, Robert Proctor, Michael Jourdan, and Benno Rayhrer of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-43646



This **Block Diagram** is a simplified representation the signal flow downstream of the inputs from two antennas. Each filter bank converts time-domain data to frequency-domain data in 400 overlapping 1.25-MHz-wide frequency channels that span the IF range from 700 to 1,200 MHz. The combiner, synthesizer, and receiver were undergoing development at the time of reporting the information for this article.