Efficient Multiplexer FPGA Block Structures Based on G₄FETs

Fewer G₄FETs than conventional transistors would be needed to implement multiplexers.

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Generic structures have been conceived for multiplexer blocks to be implemented in field-programmable gate arrays (FPGAs) based on four-gate field-effect transistors (G₄FETs). This concept is a contribution to the continuing development of digital logic circuits based on G₄FETs and serves as a further demonstration that logic circuits based on G₄FETs could be more efficient (in the sense that they could contain fewer transistors), relative to functionally equivalent logic circuits based on conventional transistors.

Results in this line of development at earlier stages were summarized in two previous NASA Tech Briefs articles: “G₄FETs as Universal and Programmable Logic Gates” (NPO-41698), Vol. 31, No. 7 (July 2007), page 44, and “Efficient G₄FET-Based Logic Circuits” (NPO-44407), Vol. 32, No. 1 (January 2008), page 38. As described in the first-mentioned previous article, a G₄FET can be made to function as a three-input NOT-majority gate, which has been shown to be a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer components than are required for conventional transistor-based circuits performing the same logic functions. The second-mentioned previous article reported results of a comparative study of NOT-majority-gate...

A Four-to-One Multiplexer is a special case of a 2ⁿ-to-1 multiplexer, which can perform a variety of logic functions on 2ⁿ binary data inputs (x₀,...,xₓ⁻¹), and n control (selection) inputs (c₀,...,cₓ⁻¹). In this case, n = 2. The combination of the control inputs can be interpreted as a binary integer, c, in the range of 0 to 2ⁿ – 1.
(G4FET)-based logic-circuit designs and equivalent NOR- and NAND-gate-based designs utilizing conventional transistors. [NOT gates (inverters) were also included, as needed, in both the G4FET-and the NOR-and NAND-based designs.] In most of the cases studied, fewer logic gates (and, hence, fewer transistors), were required in the G4FET-based designs.

There are two popular categories of FPGA block structures or architectures: one based on multiplexers, the other based on lookup tables. In standard multiplexer-based architectures, the basic building block is a treelike configuration of multiplexers, with possibly a few additional logic gates such as ANDs or ORs. Interconnections are realized by means of programmable switches that may connect the input terminals of a block to output terminals of other blocks, may bridge together some of the inputs, or may connect some of the input terminals to signal sources representing constant logical levels 0 or 1.

The left part of the figure depicts a four-to-one G4FET-based multiplexer tree; the right part of the figure depicts a functionally equivalent four-to-one multiplexer based on conventional transistors. The G4FET version would contain 54 transistors; the conventional version contains 70 transistors.

VLSI Microsystem for Rapid Bioinformatic Pattern Recognition

Rapid processing is made possible by a massively parallel neural-computing architecture.

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A system comprising very-large-scale integrated (VLSI) circuits is being developed as a means of bioinformatics-oriented analysis and recognition of patterns of fluorescence generated in a microarray in an advanced, highly miniaturized, portable genetic-expression-assay instrument. Such an instrument implements an on-chip combination of polymerase chain reactions and electrochemical transduction for amplification and detection of deoxyribonucleic acid (DNA).

Commonly, the design of such an instrument provides for a sample and a reference channel, so that it can be used to perform a dual-label assay for identifying differentially expressed genes. A dual-label assay also reduces spurious variability attributable to aspects of spots in the microarray that affect both the sample and the reference specimen similarly. The logarithm of the relative intensities of the two fluorescent-dye-labeled specimens at each spot is calculated and used in analyzing the fluorescence image of the assay. Heretofore, analysis of the fluorescence image has typically involved sequential, pixel-by-pixel processing in a digital computer. Such processing does not enable real-time recognition of genetic patterns of interest — a significant drawback where, for example, it may be desirable or necessary to recognize dangerous microbes in the field. In contrast, a system like the one now being developed enables robust, real-time recognition.

The system (see figure) includes a chip, denoted a biochip, that contains VLSI circuitry for collecting the fluorescence inputs and generates analog signals proportional to the logarithms of the fluorescence-intensity ratios for the spots in the microarray. The outputs of the biochip are fed as inputs to another chip that contains a VLSI artificial neural network (ANN), which performs the processing for recognition of bioinformatic patterns of interest. The ANN design pro-

This work was done by Farrokh Vatan and Amir Fijany of Caltech for NASA’s Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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