A computer program defines an XML schema for specifying the interface to a generic FPGA from the perspective of software that will interact with the device. This XML interface description is then translated into header files for C, Verilog, and VHDL. User interface definition input is checked via both the provided XML schema and the translator module to ensure consistency and accuracy.

Currently, programming used on both sides of an interface is inconsistent. This process, which ensures that whenever an interface is changed, all of the code that uses the header files describing it is recompiled.

This work was done by Elizabeth R. Boro-son of Caltech for NASA’s Jet Propulsion Lab-oratory.

This software is available for commercial li-ensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-45748.