Solder Joint Health Monitoring Testbed
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Motivation
The solder joint failure detection method, called SJ-BIST, has been developed by Ridgetop Group Inc. under a Small Business Innovation Research (SBIR) contract. This technology was supported under the Department of Defense SBIR Program at the Naval Air Systems Command, Joint Strike Fighter. Future research items are still in the formulation stage. Ideas include investigating if this technology will work with Commercial-off-the-Shelf components.

System Description and Block Diagram
The system was designed to be easily integrated into research aircraft and to use existing instrumentation infrastructure, such as time and data recording. Each system consists of five test circuit boards, and generates one output stream. The output is formatted as temperature, pressure, altitude, and a variety of environmental data.

Circuit Board Description and Block Diagram
The circuit will be implemented on a multi-layer circuit board designed for a custom 12.5mm tape-and-reel header at 0.75mm centerline. The master and slave circuit boards use the same design, the FPGA bitstream is the only difference between the master and slave boards. The master board collects all of the data and is responsible for digitizing the output of accelerometers placed on each slave board. The FPGA will detect solder joint failures as time and data recording. The master board to digitize the output of accelerometers placed on each slave board.

Slave FPGA Description
The master FPGA design is responsible for recording the master board's input and for recording the output of the slave board's FPGA. The master FPGA will incorporate a 32kHz ADC to record the output of the slave board's FPGA. The master FPGA will incorporate a 32kHz ADC to record the output of the slave board's FPGA. The master FPGA will incorporate a 32kHz ADC to record the output of the slave board's FPGA.

Master FPGA Description
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Test Plan
Testing will be conducted at two phases. The first phase is to conduct testing in a simulated environmental chamber and to set up a table. The second phase is to conduct testing in an actual environment. The test board will be mounted on a rack and will be connected to a computer via a network connection. The test board will be connected to a computer via a network connection. The test board will be connected to a computer via a network connection.

Future Work
Future work includes implementing this technology with Commercial-off-the-Shelf components. This technology will be used to detect solder joint failures in real-time. The technology will be used to detect solder joint failures in real-time. The technology will be used to detect solder joint failures in real-time.

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