Motivation

The master FPGA is designed for acquiring its master sensor data and coordinating sensor data receiving and processing. The slave FPGA is designed for high-speed data collection (HDLC). The master FPGA is the primary data collector and processor, and the slave FPGAs are in charge of data collection and processing.

Circuit Board Description and Block Diagram

The circuit board includes a master FPGA and four slave FPGAs. The master FPGA receives data from the other four boards in the system and digitizes the accelerometer data for both the master and slave boards. The master FPGA also processes the data and sends it via HDLC to the master board. The slave FPGAs digitize the other sensor data and send it via HDLC to the master board.

Slave FPGA Description

The slave FPGA is described in detail in the previous paragraph. It is designed to receive sensor data from the master FPGA and process it for use in the system.

Master FPGA Description

The master FPGA is described in detail in the previous paragraph. It is designed to receive sensor data from the slave FPGAs and process it for use in the system.

Test Plan

Testing will involve installing the FPGA board into the flight instrument and conducting flight tests. The flight tests will be conducted in an altitude/temperature chamber and on a flight test bed. The objective of the flight tests is to validate the FPGA board's performance in a real-world environment.

Future Work

Future work includes designing and implementing a software algorithm to analyze the data collected by the FPGA board. This algorithm will be used to detect failures before they occur and to provide a higher level of confidence in the use of BGA packages.

Acknowledgments

The authors would like to thank the NASA Dryden Flight Research Center for providing the flight testbed and flight test data. They would also like to thank the Ridgetop Group for providing the FPGA development tools and support.

System Board Description and Block Diagram

The system board is designed to be easily integrated into research aircraft and to use existing instrumentation infrastructure. The board will run on 28VDC power, which is stepped down to 5V through a DC-DC converter. The 5V power will be provided to separate digital and analog circuits.

Research Program Overview

The research program is an ongoing effort to develop and validate a new technique for monitoring solder joint health in real-time. The program is a collaboration between Ridgetop Group and NASA Dryden Flight Research Center. The program is funded by the NASA Aviation Safety Program and the NASA Innovative Partnerships Program. The program is led by Michael M. Delaney and is supported by a team of researchers.

Solder Joint Failure Detection

The Solder Joint Failure Detection (SJ-BIST) block diagram is shown below. The SJ-BIST requires two dedicated FPGA I/O pins for each solder joint monitored. The SJ-BIST is designed to detect solder joint failures in real-time and to provide a warning to the system when a failure occurs.

Acknowledgments

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Future Work

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