The master and slave circuit boards use the same design, the FPGA bitstream is the only difference between the master and slave boards. The solder joints can only be inspected using X-ray or non-destructive ultrasonic inspection. An additional objective is to gather environmental data for future development of physics-innovative research (SBIR) contract.

An X-ray will detect failures before the unit has an operational fault. This enables a higher confidence in the use of BGA packages for higher speed data including pressure, temperature, and humidity. This data will provide insight into the failure modes of BGA packages to inform future developments.

The master FPGA is responsible for collecting data from the master board and recording the data on a PCM telemetry system. The slave FPGA is responsible for monitoring its own solder joint health and collecting low level data link control (HDLC) data. The master FPGA will send data frames over Ethernet for testing. The master FPGA will also be connected to a computer running a software RISC core processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

The system will run on 28VDC power which is stepe down to 5V through a DC-DC converter. The 5V power will be provided to separate voltage regulators to produce the voltage levels required by FPGA and other circuitry. The voltage levels required on the board are 5V, 3.3V, 1.8V, and 1.2V.

The board will have 256MB of SDRAM and 32MB of Flash memory. The onboard memory will allow the use of a MicroBlaze soft core RISC processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

The master FPGA block diagram shows the master FPGA design to be responsible for collecting data from the master board and recording the data on a PCM telemetry system. The master FPGA will send data frames over Ethernet for testing. The master FPGA will also be connected to a computer running a software RISC core processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

The slave FPGA description shows the slave FPGA design to be responsible for collecting data from the master board and recording the data on a PCM telemetry system. The master FPGA will send data frames over Ethernet for testing. The master FPGA will also be connected to a computer running a software RISC core processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

The test plan includes the following phases: pre-flight testing, on-ground testing, and in-flight testing. For ground testing, the PCM output will be monitored using an Omega 3000 PCM telemetry processing system. In flight, the data is formatted as an IRIG 106 compliant PCM stream. The master FPGA has sufficient resources available to implement a software RISC core processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

Future work includes investigating if this technology will work with Colonial I test beds and collecting data from other sets of circuit boards. The test bed for the Colonial I test bed is shown in the diagram. Thetest bed will be representative of environmental conditions encountered in an unpressurized avionics bay on high performance research aircraft. The data is formatted as an IRIG 106 compliant PCM stream. The master FPGA has sufficient resources available to implement a software RISC core processor to produce the voltage levels required by FPGA and other circuitry. The voltage levels required are on the board are 5V, 3.3V, 1.8V, and 1.2V.

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