The Solder Joint Health Monitoring Testbed was designed to monitor solder joint health in real-time, enabling the system to detect failures before they lead to operational faults and allowing for a higher confidence in the use of BGA packages in high reliability systems.

Digital temperature, humidity, and pressure sensors were placed on the circuit board to monitor environmental conditions. The data is formatted as an IRIG 106 compliant Pulse Code Modulation (PCM) stream and collected on all system boards. The master FPGA has multiple functions, including receiving data from the other four boards, digitizing accelerometer signals, and implementing a software RISC CPU to run prognosis algorithms once they are developed.

The master FPGA was responsible for collecting data frames over Ethernet. The circuit board will have 256MB of SDRAM and 32MB of Flash memory. The onboard memory will allow for the use of a MicroBlaze soft core RISC, and the change in resources allows for future expansion. The solder joint failure detection method, SJ-BIST, was supported under the Department of Defense SBIR Program at the Naval Air Systems Command, Joint Strike Fighter (JSF) program.

Testing will be conducted in two phases. The first phase is to conduct testing in an altitude/temperature chamber and on a small research aircraft. The second phase will take place in Baja California, Mexico. The SJ-BIST technology was developed by Ridgetop Group, who is also responsible for developing the testbed system.

Future Work
The Solder Joint Health Monitoring Testbed is an ongoing project, with plans for future development and testing in various environments. The system will be further refined and tested in real-world conditions to improve accuracy and reliability.