G4-FETs as Universal and Programmable Logic Gates

Logic functions could be implemented using fewer active circuit elements.

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An analysis of a patented generic silicon-on-insulator (SOI) electronic device called a G4-FET has revealed that the device could be designed to function as a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer discrete components than are required for conventional transistor-based circuits performing the same logic functions.

A G4-FET is a combination of a junction field-effect transistor (JFET) and a metal oxide-semiconductor field-effect transistor (MOSFET) superimposed in a single silicon island and can therefore be regarded as two transistors sharing the same body. A G4-FET can also be regarded as a single transistor having four gates: two side junction-based gates, a top MOS gate, and a back gate activated by biasing of the SOI substrate. Each of these gates can be used to control the conduction characteristics of the transistor; this possibility creates new options for designing analog, radio-frequency, mixed-signal, and digital circuitry.

With proper choice of the specific dimensions for the gates, channels, and ancillary features of the generic G4-FET, the device could be made to function as a three-input, one-output logic gate. As illustrated by the truth table in the top part of the figure, the behavior of this logic gate would be the inverse (the NOT) of that of a majority gate. In other words, the device would function as a NOT-majority gate. By simply adding an inverter, one could obtain a majority gate. In contrast, to construct a majority gate in conventional complementary metal oxide/silicon (CMOS) circuitry, one would need four three-input AND gates and a four-input OR gate, altogether containing 32 transistors.

The middle part of the figure schematically depicts three ways of realizing an inverter (NOT gate), two ways of realizing an AND gate, and two ways of realizing an OR gate by use of one or two NOT-majority gates. In addition (not shown in the figure), by using one of the three inputs as a programming or control input that is set to 0 or 1, a NOT-majority could be made to respond to the other inputs as either a NAND or a NOR gate, respectively. Inasmuch as the sets (NOT,AND), [NOT,OR], and [NAND,NOR] have previously been shown to be universal (in the sense that any digital computation or logic function could be realized by use of suitable combinations of members of these sets), the possibility of realizing these sets signifies that the NOT-majority gate is also universal.

The bottom part of the figure depicts a full adder, implemented by use of three NOT-majority gates and two inverters, that would put out two one-bit binary numbers in response to three input one-bit binary numbers. The design of this adder exploits the possibility of switching a NOT-majority gate between NAND and NOR functionality to minimize the number of gates needed. In contrast, the simplest implementation of
an equivalent full adder based on Boolean gates would include nine NAND gates and four inverters.

This work was done by Travis Johnson, Amir Fijany, Mohammad Mojarradi, Farkh Vatan, Nikzad Toomarian, Elizabeth Kolawa, Sorin Cristoloveanu, and Benjamin Blalock of Caltech for NASA’s Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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