



Fabrication of Buried Nanochannels From Nanowire Patterns

Sacrificial nanowires are buried, then etched away to form buried channels.

NASA's Jet Propulsion Laboratory, Pasadena, California

A method of fabricating channels having widths of tens of nanometers in silicon substrates and burying the channels under overlying layers of dielectric materials has been demonstrated. With further refinement, the method might be useful for fabricating nanochannels for manipulation and analysis of large biomolecules at single-molecule resolution. Unlike in prior methods, burying the channels does not involve bonding of flat wafers to the silicon substrates to cover exposed channels in the substrates. Instead, the formation and burying of the channels are accomplished in a more sophisticated process that is less vulnerable to defects in the substrates and less likely to result in clogging of, or leakage from, the channels.

In this method, the first step is to establish the channel pattern by forming an array of sacrificial metal nanowires on an SiO₂-on-Si substrate. In particular, the wire pattern is made by use of focused-ion-beam (FIB) lithography and a subsequent metallization/lift-off process. The pattern of metal nanowires is then transferred onto the SiO₂ layer by reactive-ion etching, which yields sacrificial SiO₂ nanowires covered by metal. After re-

moval of the metal covering the SiO₂ nanowires, what remains are SiO₂ nanowires on an Si substrate.

Plasma-enhanced chemical vapor deposition (PECVD) is used to form a layer of a dielectric material over the Si substrate and over the SiO₂ wires on the surface of the substrate. FIB milling is then performed to form trenches at both ends of each SiO₂ wire. The trenches serve as openings for the entry of chem-

icals that etch SiO₂ much faster than they etch Si. Provided that the nanowires are not so long that the diffusion of the etching chemicals is blocked, the sacrificial SiO₂ nanowires become etched out from between the dielectric material and the Si substrate, leaving buried channels. At the time of reporting the information for this article, channels 3 μm long, 20 nm deep, and 80 nm wide (see figure) had been fabricated by this method.

This work was done by Daniel Choi and Eui-Hyeok-Yang of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

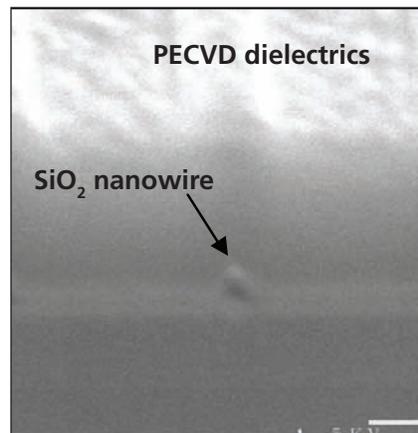
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*Innovative Technology Assets Management
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*Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
(818) 354-2240*

E-mail: iaoffice@jpl.nasa.gov

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This Scanning Electron Micrograph shows a cross section of a 20-by-80-nm channel formed between a silicon substrate and an overlying layer of dielectric material.

Diamond Smoothing Tools

Machined surfaces could be made much smoother.

Marshall Space Flight Center, Alabama

Diamond smoothing tools have been proposed for use in conjunction with diamond cutting tools that are used in many finish-machining operations. Diamond machining (including finishing) is often used, for example, in fabrication of precise metal mirrors.

A diamond smoothing tool according to the proposal would have a smooth spherical surface. For a given finish machining operation, the smoothing tool would be mounted next to the cutting

tool. The smoothing tool would slide on the machined surface left behind by the cutting tool, plastically deforming the surface material and thereby reducing the roughness of the surface, closing microcracks and otherwise generally reducing or eliminating microscopic surface and subsurface defects, and increasing the microhardness of the surface layer. It has been estimated that if smoothing tools of this type were used in conjunction with cut-

ting tools on sufficiently precise lathes, it would be possible to reduce the roughness of machined surfaces to as little as 3 nm.

A tool according to the proposal would consist of a smoothing insert in a metal holder. The smoothing insert would be made from a diamond/metal functionally graded composite rod preform, which, in turn, would be made by sintering together a bulk single-crystal or polycrystalline diamond, a diamond