Cumulative Timers for Microprocessors
Accumulated operating times and serial numbers would be displayed.

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It has been proposed to equip future microprocessors with electronic cumulative timers, for essentially the same reasons for which land vehicles are equipped with odometers (total-distance-traveled meters) and aircraft are equipped with Hobbs meters (total-engine-operating-time meters). Heretofore, there has been no way to determine the amount of use to which a microprocessor (or a product containing a microprocessor) has been subjected. The proposed timers would count all microprocessor clock cycles and could only be read by means of microprocessor instructions but, like odometers and Hobbs meters, could never be reset to zero without physically damaging the chip.

A timer according to the proposal could be either an external device connected to a microprocessor or embedded within the microprocessor. The external implementation could be retrofit to a pre-existing microprocessor. In the external implementation (see figure), the timer would include a prescaler; an inter-integrated-circuit (I2C) or a serial peripheral interface (SPI) module; and a flash random-access memory (RAM) that would store a unique serial number and a prescaler-reduced count of clock cycles, both of which could be read over a one- or two-wire bus.

The serial number stored in the flash RAM would serve as the serial number of the microprocessor and of any equipment containing the microprocessor, for purposes of registering any warranty of the equipment and verifying the authenticity of the equipment. On a display generated by the microprocessor, the user could compare the electronically stored serial number with the serial number printed on a label affixed to the equipment and the serial number on the warranty registration and could read the accumulated operating time. Periodically, during normal operation, the microprocessor would attempt to interrogate the flash memory and would turn itself off if it were unable to read its proper serial number. Upon each such interrogation, the count stored in the flash memory would be incremented.

The internal implementation would function similarly to the external implementation, except that the serial number and the prescaler-reduced count of clock cycles would be stored in either (1) part of the flash RAM used by the rest of the microprocessor or (2) a separate flash RAM dedicated to the timer. It would be necessary to design the microprocessor hardware...
and software so that there would be no way to decrement the count or otherwise exert external control over the timer flash RAM.

This work was done by John O. Battle of Caltech for NASA’s Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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