A technique of monitoring digital closed-loop feedback systems has been conceived. The basic idea is to obtain information on the performances of closed-loop feedback circuits in such systems to aid in the determination of the functionality and integrity of the circuits and of performance margins.

The need for this technique arises as follows: Some modern digital systems include feedback circuits that enable other circuits to perform with precision and are tolerant of changes in environment and the device’s parameters. For example, in a precision timing circuit, it is desirable to make the circuit insensitive to variability as a result of the manufacture of circuit components and to the effects of temperature, voltage, radiation, and aging. However, such a design can also result in masking the indications of damaged and/or deteriorating components.

The present technique incorporates test circuitry and associated engineering-
telemetry circuitry into an embedded system to monitor the closed-loop feedback circuits, using “spare gates” that are often available in field programmable gate arrays (FPGAs). This technique enables a test engineer to determine the amount of performance margin in the system, detect “out of family” circuit performance, and determine one or more trend(s) in the performance of the system.

In one system to which the technique has been applied, an ultra-stable oscillator is used as a reference for internal adjustment of 12 time-to-digital converters (TDCs). The feedback circuit produces a pulse-width-modulated signal that is fed as a control input into an amplifier, which controls the circuit’s operating voltage. If the circuit’s gates are determined to be operating too slowly or rapidly when their timing is compared with that of the reference signal, then the pulse width increases or decreases, respectively, thereby commanding the amplifier to increase or reduce, respectively, its output level, and “adjust” the speed of the circuits. The nominal frequency of the TDC’s pulse width modulated outputs is approximately 40 kHz.

In this system, the technique is implemented by means of a monitoring circuit that includes a 20-MHz sampling circuit and a 24-bit accumulator with a gate time of 10 ms. The monitoring circuit measures the duty cycle of each of the 12 TDCs at a repetition rate of 28 Hz. The accumulator content is reset to all zeroes at the beginning of each measurement period and is then incremented or decremented based on the value of the state of the pulse width modulated signal. Positive or negative values in the accumulator correspond to duty cycles greater or less, respectively, than 50 percent.

This work was done by Richard Katz and Igor Kleyner of Goddard Space Flight Center. Further information is contained in a TSP (see page 1), GSC-15489-1.