



## **Small Microprocessor for ASIC or FPGA Implementation**

*Goddard Space Flight Center, Greenbelt, Maryland*

A small microprocessor, suitable for use in applications in which high reliability is required, was designed to be implemented in either an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA). The design is based on commercial microprocessor architecture, making it possible to use available software development tools and thereby to implement the microprocessor at relatively low cost. The design features enhancements, including trapping during execution of il-

legal instructions. The internal structure of the design yields relatively high performance, with a significant decrease, relative to other microprocessors that perform the same functions, in the number of microcycles needed to execute macroinstructions.

The problem meant to be solved in designing this microprocessor was to provide a modest level of computational capability in a general-purpose processor while adding as little as possible to the power demand, size, and weight of a

system into which the microprocessor would be incorporated. As designed, this microprocessor consumes very little power and occupies only a small portion of a typical modern ASIC or FPGA. The microprocessor operates at a rate of about 4 million instructions per second with clock frequency of 20 MHz.

*This work was done by Igor Kleyner, Richard Katz, and Hugh Blair-Smith of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15493-1*

## **Source-Coupled, N-Channel, JFET-Based Digital Logic Gate Structure Using Resistive Level Shifters**

*John H. Glenn Research Center, Cleveland, Ohio*

A circuit topography is used to create usable, digital logic gates using N (negatively doped) channel junction field effect transistors (JFETs), load resistors, level shifting resistors, and supply rails whose values are based on the DC parametric distributions of these JFETs. This method has direct application to the current state-of-the-art in high-temperature (300 to 500 °C and higher) silicon carbide (SiC) device production, and defines an adaptation to the logic gate described in U.S. Patent 7,688,117 in that, by removing the level shifter from the output of the gate structure described in the patent (and applying it to the input of the same gate), a source-

coupled gate topography is created. This structure allows for the construction AND/OR (sum of products) arrays that use far fewer transistors and resistors than the same array as constructed from the gates described in the aforementioned patent. This plays a central role when large multiplexer constructs are necessary; for example, as in the construction of memory.

This innovation moves the resistive level shifter from the output of the basic gate structure to the front as if the input is now configured as what would be the output of the preceding gate, wherein the output is the two level shifting resistors. The output of this innovation can

now be realized as the lone follower transistor with its source node as the gate output. Additionally, one may leave intact the resistive level shifter on the new gate topography. A source-coupled to direct-coupled logic translator will be the result.

*This work was done by Michael J. Krasowski of Glenn Research Center. Further information is contained in a TSP (see page 1).*

*Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18636-1.*

## **High-Voltage-Input Level Translator Using Standard CMOS**

**High-voltage input circuitry would be combined with standard low-voltage CMOS circuitry.**

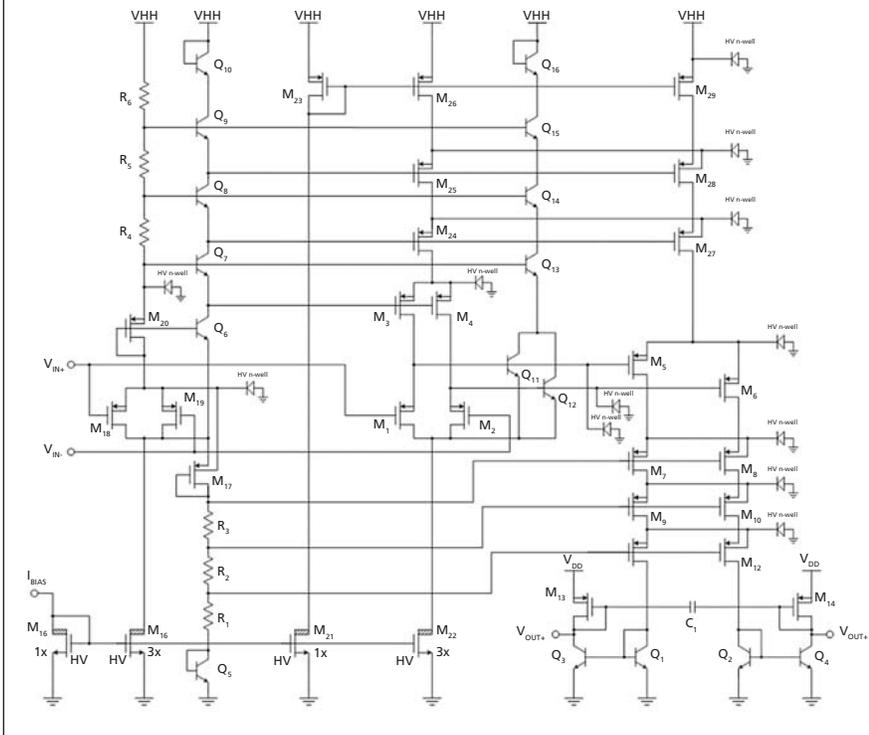
*NASA's Jet Propulsion Laboratory, Pasadena, California*

A proposed integrated circuit would translate (1) a pair of input signals having a low differential potential and a possibly high common-mode potential into (2) a pair of output signals having the same low differential potential and a low common-mode potential. As used

here, "low" and "high" refer to potentials that are, respectively, below or above the nominal supply potential (3.3 V) at which standard complementary metal oxide/semiconductor (CMOS) integrated circuits are designed to operate. The input common-mode potential

could lie between 0 and 10 V; the output common-mode potential would be 2 V. This translation would make it possible to process the pair of signals by use of standard 3.3-V CMOS analog and/or mixed-signal (analog and digital) circuitry on the same integrated-circuit

Input Common-Mode Range	0.3 to 10V
-3 dB Bandwidth	150 kHz
Common-Mode Rejection Ratio	>80 dB
Power Supply Rejection Ratio	>50 dB
Noise Characteristics	
MOS Flicker Noise@ 1Hz	≈ 90 nV/√Hz
Flicker Noise Corner	≈ 800 Hz
Broadband Noise	≈ 55 nV/√Hz



Several Performance Parameters of the proposed level translator were extracted from results of computational simulations. The proposed circuit schematic is shown.

chip. A schematic of the circuit is shown in the figure.

Standard 3.3-V CMOS circuitry cannot withstand input potentials greater than about 4 V. However, there are many applications that involve low-differential-potential, high-common-mode-potential input signal pairs and in which standard 3.3-V CMOS circuitry, which is relatively inexpensive, would be the most appropriate

circuitry for performing other functions on the integrated-circuit chip that handles the high-potential input signals. Thus, there is a need to combine high-voltage input circuitry with standard low-voltage CMOS circuitry on the same integrated-circuit chip. The proposed circuit would satisfy this need.

In the proposed circuit, the input signals would be coupled into both a level-

shifting pair and a common-mode-sensing pair of CMOS transistors. The output of the level-shifting pair would be fed as input to a differential pair of transistors. The resulting differential current output would pass through six standoff transistors to be mirrored into an output branch by four heterojunction bipolar transistors. The mirrored differential current would be converted back to potential by a pair of diode-connected transistors, which, by virtue of being identical to the input transistors, would reproduce the input differential potential at the output.

The common-mode-sensing pair would be used to set the control potential for a biasing circuit that would provide the proper terminal potentials for protecting all devices against excessive excursions of potential for a common-mode potential range of 0 to 12 V. The biasing circuit would include high-voltage-drain transistors capable of withstanding the full high input potentials on their drains; the incorporation of these transistors would enable simplification of part of the bias circuit and of the circuitry associated with the input transistor pairs. High-voltage n-wells would enable floating of substrates of p-channel metal oxide/semiconductor field-effect transistors to potentials as high as tens of volts, whereas devices containing standard n-wells break down at potentials between 6 and 7 V, even though maximum gate-to-source and drain-to-source potentials remain at 3.3 V.

The expected performance of the circuit has been studied in computational simulations. The table presents values of some performance parameters determined from the results of the simulations.

*This work was done by Jeremy A. Yager, Mohammad M. Mojarradi, and Tuan A. Vo of Caltech and Benjamin J. Blalock from University of Tenn., Knoxville for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-45762*

## Monitoring Digital Closed-Loop Feedback Systems

Designed-in test circuitry enables determination of performance margins and performance trends.

Goddard Space Flight Center, Greenbelt, Maryland

A technique of monitoring digital closed-loop feedback systems has been conceived. The basic idea is to obtain information on the performances of closed-loop feedback circuits in such systems to aid in the determination of the functionality and integrity of the circuits and of performance margins.

The need for this technique arises as follows: Some modern digital systems include feedback circuits that enable other circuits to perform with precision and are tolerant of changes in environment and the device's parameters. For example, in a precision timing circuit, it is desirable to make the circuit insensitive to variability as a re-

sult of the manufacture of circuit components and to the effects of temperature, voltage, radiation, and aging. However, such a design can also result in masking the indications of damaged and/or deteriorating components.

The present technique incorporates test circuitry and associated engineering-