Coaxial Cables for Martian Extreme Temperature Environments

NASA’s Jet Propulsion Laboratory, Pasadena, California

Work was conducted to validate the use of the rover external flexible coaxial cabling for space under the extreme environments to be encountered during the Mars Science Laboratory (MSL) mission. The antennas must survive all ground operations plus the nominal 670-Martian-day mission that includes summer and winter seasons of the Mars environment.

Successful development of processes established coaxial cable hardware fatigue limits, which were well beyond the expected in-flight exposures. In keeping with traditional qualification philosophy, this was accomplished by subjecting flight-representative coaxial cables to temperature cycling of the same depth as expected in-flight, but for three times the expected number of in-flight thermal cycles.

Insertion loss and return loss tests were performed on the coaxial cables during the thermal chamber breaks. A vector network analyzer was calibrated and operated over the operational frequency range 7.145 to 8.450 GHz. Even though some of the exposed cables function only at UHF frequencies (approximately 400 MHz), the testing was more sensitive, and extending the test range down to 400 MHz would have cost frequency resolution.

The Gore flexible coaxial cables, which were the subject of these tests, proved to be robust and displayed no sign of degradation due to the 3X exposure to the punishing Mars surface operations cycles.

This work was done by Rajeshuni Ramasham, Wayne L. Harvey, Sam Valas, and Michael C. Tsai of Caltech for NASA’s Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-47452

Using Spare Logic Resources To Create Dynamic Test Points

Goddard Space Flight Center, Greenbelt, Maryland

A technique has been devised to enable creation of a dynamic set of test points in an embedded digital electronic system. As a result, electronics contained in an application specific circuit [e.g., gate array, field programmable gate array (FPGA)] can be internally “probed,” even when contained in a closed housing during all phases of test.

In the present technique, the test points are not fixed and limited to a small number; the number of test points can vastly exceed the number of buffers or pins, resulting in a compact footprint. Test points are selected by means of spare logic resources within the ASIC(s) and/or FPGA(s). A register is programmed with a command, which is used to select the signals that are sent off-chip and out of the housing for monitoring by test engineers and external test equipment.

The register can be commanded by any suitable means: for example, it could be commanded through a command port that would normally be used in the operation of the system. In the original application of the technique, commanding of the register is performed via a MIL-STD-1553B communication subsystem.

This work was done by Richard Katz and Igor Kleyner of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15490-1