Making Wide-IF SIS Mixers With Suspended Metal-Beam Leads

Devices are fabricated on SOI substrates by use of silicon-micromachining techniques.

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A process that employs silicon-on-insulator (SOI) substrates and silicon (Si) micromachining has been devised for fabricating wide-intermediate-frequency-band (wide-IF) superconductor/insulator/superconductor (SIS) mixer devices that result in suspended gold beam leads used for radio-frequency grounding. The mixers are formed on 25-µm-thick silicon membranes. They are designed to operate in the 200 to 300 GHz frequency band, wherein wide-IF receivers for terospheric-chemistry and astrophysical investigations are necessary.

The fabrication process can be divided into three sections:

1. The front-side process, in which SIS devices with beam leads are formed on a SOI wafer;
2. The backside process, in which the SOI wafer is wax-mounted onto a carrier wafer, then thinned, then partitioned into individual devices; and
3. The release process, in which the individual devices are separated using a lithographic dicing technique.

The total thickness of the starting 4-in. (10.16-cm)-diameter SOI wafer includes 25 µm for the Si device layer, 0.5 µm for the buried oxide (BOX) layer, and 350 µm for the Si-handle layer. The front-side process begins with deposition of an etch-stop layer of SiO2 or AlN, followed by deposition of a Nb/AlN/Nb trilayer in a load-locked DC magnetron sputtering system. The lithography for four of a total of five layers is performed in a commercial wafer-stepping apparatus. Diagnostic test dies are patterned concurrently at certain locations on the wafer, alongside the mixer devices, using a different mask set. The conventional, self-aligned lift-off process is used to pattern the SIS devices up to the wire level.

The beam-leads are formed as extensions from the SIS devices by using a bilayer lift-off process with poly(methyl methacrylate) (PMMA) and photoresist. After defining the beam-leads, the interfacial layer between the PMMA and photoresist is etched in an oxygen plasma. Ultraviolet irradiation is used to expose the PMMA, which is then developed in chlorobenzene. The wafer is then placed in the sputtering system, where a seed layer of Nb/Au is deposited to enhance adhesion. The Au beam leads are grown to the desired thickness in an electron-beam evaporation system. After deposition, the unwanted gold is easily removed by lift-off in acetone.
In the next step, the backside process is initiated by wax mounting the SOI wafer onto a sapphire carrier wafer, as illustrated in the figure. The 350-µm Si-handle layer of the SOI wafer is removed by deep-trench reactive-ion etching (DRIE). Now further lithography is necessary on the 25-µm thick Si membrane layer that is held down onto a 4-in. (10.16-cm) wafer by a relatively high-melting-point wax. If the cooling on the DRIE system is not sufficient during the etching of the handle layer, the wax would start to flow at ~85 ºC, causing the Si membrane to wrinkle, which would prevent any backside lithography to be performed. A contact aligner is used to pattern the now-exposed 25-µm thick Si layer in order to partition the devices into individual mixers. Since an anisotropic etch is desired for patterning the 25-µm thick Si membrane, the DRIE apparatus is operated in the pulsed mode where SF₆ and C₂F₄ are flowed intermittently. The devices are then released by dissolving the front-side protection resist in acetone, followed by soaking in an N-methyl-pyrrolidone-based solution, which removes any residual photoresist. The devices are finally dipped in IPA.

Electrical measurements of the devices was performed at 4.2 K. Measurements were performed on devices that were on thinned 25-µm Si membranes and those devices where the handle layer was not removed. No change in device parameters such as current density (J_c), gap voltage, and sub-gap leakage current was observed, indicating the backside process did not introduce any thermal excursions, which would have been evident from increased leakage currents and reduced gap voltages. In addition, the J_c on the individual mixer chips correlated to the J_c that was measured on devices from the diagnostic chip. The data suggest that this wax-mounted backside lithography beam-lead process is compatible with conventional SIS device fabrication technology.

This work was done by Anupama Kaul, Bruce Bumble, Karen Lee, Henry LeDuc, Frank Rice, and Jonas Zmuidzinas of Caltech for NASA’s Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-41296