Making Wide-IF SIS Mixers With Suspended Metal-Beam Leads

A process that employs silicon-on-insulator (SOI) substrates and silicon (Si) micromachining has been devised for fabricating wide-intermediate-frequency-band (wide-IF) superconductor/insulator/superconductor (SIS) mixer devices that result in suspended gold beam leads used for radio-frequency grounding. The mixers are formed on 25-µm-thick silicon membranes. They are designed to operate in the 200 to 300 GHz frequency band, wherein wide-IF receivers for tropospheric-chemistry and astrophysical investigations are necessary.

The fabrication process can be divided into three sections:
1. The front-side process, in which SIS devices with beam leads are formed on a SOI wafer;
2. The backside process, in which the SOI wafer is wax-mounted onto a carrier wafer, then thinned, then partitioned into individual devices; and
3. The release process, in which the individual devices are separated using a lithographic dicing technique.

The total thickness of the starting 4-in. (10.16-cm)-diameter SOI wafer includes 25 µm for the Si device layer, 0.5 µm for the buried oxide (BOX) layer, and 350 µm for the Si-handle layer. The front-side process begins with deposition of an etch-stop layer of SiO2 or AlN/ NbAl trilayer-covered substrate is then patterned into individual devices by use of conventional integrated-circuit processing techniques. A wide parameter space was investigated over which devices were fabricated reproducibly and with high quality. The hysteretic nature of the current-voltage characteristic along with the high subgap ratio indicate the incident nitrogen ions chemically reacted with the Al layer as expected, to form a continuous AlN barrier. Chemical analysis of the barrier performed using x-ray photoelectron-spectroscopy confirmed the presence of AlN. Critical current density Ic ranged from 550 to 9,400 A/cm² with subgap-to-normal resistance ratios ranging from 50 to 12.6. The Ic was found to decrease with increasing dose and increasing beam energy. The run-to-run reproducibility was determined to be very good. The spatial variation of the ion current density was also measured and correlated with Ic for a 76-mm Si wafer. The junctions were also found to be stable on annealing up to temperatures of 250 °C. This technique could be applied to form other metal nitrides at room temperatures for device applications where a high degree of control is desired.

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In the next step, the backside process is initiated by wax mounting the SOI wafer onto a sapphire carrier wafer, as illustrated in the figure. The 350-µm Si-handle layer of the SOI wafer is removed by deep-trench reactive-ion etching (DRIE). Now further lithography is necessary on the 25-µm-thick Si membrane layer that is held down onto a 4-in. (10.16-cm) wafer by a relatively high-melting-point wax. If the cooling on the DRIE system is not sufficient during the etching of the handle layer, the wax would start to flow at ~85°C, causing the Si membrane to wrinkle, which would prevent any backside lithography to be performed. A contact aligner is used to pattern the now-exposed 25-µm-thick Si layer in order to partition the devices into individual mixers. Since an anisotropic etch is desired for patterning the 25-µm-thick Si membrane, the DRIE apparatus is operated in the pulsed mode where SF₆ and C₂F₄ are flowed intermittently. The devices are then released by dissolving the front-side protection resist in acetone, followed by soaking in an N-methyl-pyrrolidone-based solution, which removes any residual photoresist. The devices are finally dipped in IPA.

Electrical measurements of the devices were performed at 4.2 K. Measurements were performed on devices that were on thinned 25-µm Si membranes and those devices where the handle layer was not removed. No change in device parameters such as current density ($J_c$), gap voltage, and sub-gap leakage current was observed, indicating the backside process did not introduce any thermal excursions, which would have been evident from increased leakage currents and reduced gap voltages. In addition, the $J_c$ on the individual mixer chips correlated to the $J_c$ that was measured on devices from the diagnostic chip. The data suggest that this wax-mounted backside lithography beam-lead process is compatible with conventional SIS device fabrication technology.

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