Current Single Event Effects Compendium of Candidate Spacecraft Electronics for NASA

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***Abstract*— We present the results of single event effects (SEE) testing and analysis investigating the effects of radiation on electronics. This paper is a summary of test results.**

***Index Terms*—Single event effects, spacecraft electronics, digital, linear bipolar, and hybrid devices.**

I. Introduction

The performance of electronic devices in a space radiation environment is often limited by its susceptibility to SEE. Interpreting the results of SEE testing of complex devices is quite difficult. As discussed elsewhere [1], SEE test data is often application specific and adequate understanding of the test conditions is critical.

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Given this limitation of test data (application-specific), studies discussed here were undertaken to establish the sensitivities of candidate spacecraft electronics as well as new electronic devices to heavy ion and proton-induced single event upset (SEU), single event latchup (SEL), and single event transients (SET). For total ionizing dose (TID) and displacement damage results, see a companion paper submitted to the 2010 IEEE NSREC Radiation Effects Data Workshop entitled: "Current Total Ionizing Dose and Displacement Damage Compendium of Candidate Spacecraft Electronics for NASA" by D. Cochran, *et al*. [2].

II. Test Techniques and Setup

A. Test Facilities

All SEE tests were performed between February 2009 and February 2010. Heavy ion experiments were conducted at Lawrence Berkeley National Laboratory (LBNL) [3], and at Texas A&M University Cyclotron (TAMU) [4]. Both of these facilities are suitable for providing a variety of ions over a range of energies for testing. The devices under test (DUTs) were irradiated with heavy ions having linear energy transfers (LETs) ranging from 0.59 to 120 MeV•cm^2/mg. Fluxes ranged from $1x10^2$ to $1x10^7$ particles/cm^2/s, depending on device sensitivity. Representative ions used are listed in Table I. LETs between the values listed were obtained by changing the angle of incidence of the ion beam with respect to the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion [5]. Energies and LETs available varied slightly from one test date to another.

Proton SEE tests were performed at three facilities: the University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL) [6], the Indiana University Cyclotron Facility (IUCF) [7], and at a 2 MeV Van de Graaff particle accelerator. Proton test energies incident on the DUT are listed in Table II.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [8] [9]. The laser light had a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e - or about 37% - of its intensity at the surface) of 2 µm. A nominal pulse rate of 1 kHz was utilized.

TABLE I: HEAVY ION TEST FACILITIES AND TEST HEAVY IONS

	Ion	Energy (MeV)	Surface LET in Si (MeV•cm²/mg) (Normal Incidence)	Range in Si (μm)
LBNL	^{18}O	184	2.2	227
	^{22}Ne	216	3.5	175
	^{40}Ar	400	9.7	130
	^{65}Cu	659	21	110
	^{86}Kr	886	31	110
	^{136}Xe	1330	59	97
	10 MeV per AMU tune			
TAMU	^{20}Ne	300	2.5	316
	^{40}Ar	599	7.7	229
	^{63}Cu	944	17.8	172
	^{84}Kr	1259	25.4	170
	^{109}Ag	1634	38.5	156
	^{129}Xe	1934	47.3	156
	15 MeV per AMU tune			
	^{22}Ne	545	1.8	799
	^{40}Ar	991	5.5	493
	^{84}Kr	2081	19.8	332
	^{139}Xe	3197	38.9	286
	25 MeV per AMU tune			

TABLE II: PROTON TEST FACILITIES

University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL), energy tunes ranged from 6.5 to 63 MeV, flux ranged from 8×10^7 to 1×10^9 particles/cm²/s.
Indiana University Cyclotron Facility (IUCF), energy ranged from 63 to 198 MeV, flux ranged from 5×10^5 to 3×10^9 particles/cm²/s.

TABLE III: LASER TEST FACILITY

Naval Research Laboratory (NRL) Pulsed Laser SEE Test Facility Laser: 590 nm, 1 ps pulse width, beam spot size ~1.2 μm

B. Test Method

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages. We recognize that high-temperature and worst-case power supply conditions are recommended for single event latchup (SEL) device qualification.

1) SEE Testing - Heavy Ion:

Depending on the DUT and the test objectives, one or more of three SEE test methods were typically used:

Dynamic – the DUT was exercised continually while being exposed to the beam. The events and/or bit errors were counted, generally by comparing the DUT output to an unirradiated reference device or other expected output (Golden chip or virtual Golden chip methods) [10]. In some cases, the effects of clock speed or device operating modes were investigated. Results of such tests should be applied with caution due to the application-specific nature of the results.

Static – the DUT was loaded prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased – the DUT was biased and clocked while power consumption was monitored for SEL or other destructive effects. In most SEL tests, functionality was also monitored.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs and for hard errors, such as single event gate rupture (SEGR). Detailed descriptions of the types of errors observed are noted in the individual test results [11].

SET testing was performed using a high-speed oscilloscope. Individual criteria for SETs are specific to the device being tested. Please see the individual test reports for details [11].

Heavy ion SEE sensitivity experiments include measurement of the Linear Energy Transfer threshold (LET_{th}) and cross section at the maximum measured LET. The LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/cm^2. In the case where events are observed at the smallest LET tested, LET_{th} will either be reported as less than the lowest measured LET or determined approximately as the LET_{th} parameter from a Weibull fit. In the case of SEGR experiments, measurements are made of the SEGR threshold V_{ds} as a function of LET at a fixed V_{gs}.

2) SEE Testing - Proton

Proton SEE tests were performed in a manner similar to heavy ion exposures. However, because protons cause SEE via indirect ionization of recoil particles, results are parameterized in terms of proton energy rather than LET. Because such proton-induced nuclear interactions are rare, proton tests also feature higher cumulative fluences and particle flux rates than heavy ion experiments.

3) Pulsed Laser Facility Testing

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produced a spot size of about 1.2 μm at full-width half-maximum (FWHM). The X-Y-Z stage can be moved in steps of 0.1 μm for accurate positioning of SEU sensitive regions in front of the focused beam. An illuminator together with a charge coupled device camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

III. TEST RESULTS OVERVIEW

Abbreviations and conventions are listed in Table IV. Abbreviations for principal investigators (PIs) are listed in Table V, and SEE results are summarized in Table VI. Unless otherwise noted, all LETs are in MeV•cm^2/mg and all cross sections are in cm^2/device. This paper is a summary of results. Complete test reports are available online at http://radhome.gsfc.nasa.gov [11].

TABLE IV: ABBREVIATIONS AND CONVENTIONS

LET = linear energy transfer (MeV•cm^2/mg)
LET_{th} = linear energy transfer threshold (the minimum LET value for which a given effect is observed for a fluence of 1x10^7 particles/cm^2 – in MeV•cm^2/mg)
< = SEE observed at lowest tested LET
> = no SEE observed at highest tested LET
σ = cross section (cm^2/device, unless specified as cm^2/bit)
$σ_{max\ measured}$ = cross section at maximum measured LET (cm^2/device, unless specified as cm^2/bit)
ADC = analog to digital converter
App. Spec. = application specific
BiCMOS = bipolar complementary metal oxide semiconductor
CMOS = complementary metal oxide semiconductor
DUT = device under test
EDAC = error detection and correction
FPGA = field programmable gate array
H = heavy ion test
L = laser test
LCDT = low cost digital tester
LDC = lot date code
N/A = not available
P = proton test (SEE)
PI = principal investigator
POL = point of load
SEE = single event effect
SEFI = single event functional interrupt
SEL = single event latchup
SET = single event transient
SEU = single event upset
SiGe = silicon germanium
SEGR = single event gate rupture
V_{ds} = drain-source voltage
V_{gs} = gate-source voltage

TABLE V: LIST OF PRINCIPAL INVESTIGATORS

Principal Investigator (PI)	Abbreviation
Melanie Berg	MB
Martin Carts	MaC
Dakai Chen	DC
Hak Kim	HK
Kenneth LaBel	KL
Ray Ladbury	RL
Jean-Marie Lauenstein	JML
Cheryl Marshall	CM
Paul Marshall	PM
Timothy Oldham	TO
Jonathan Pellish	JP
Anthony (Tony) Sanders	AS
Michael Xapsos	MX

TABLE VI: SUMMARY OF SEE TEST RESULTS

Part Number	Manufacturer	LDC	Device Function	Tech-nology	Particle: (Facility/Date) P.I.,	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	App. Spec. Test (Y/N)	Supply Voltage	Sample Size (Number Tested)	Reference
ADC :										
ADC14155	National Semi-conductor	No LDC (test chip)	ADC	CMOS	P: (UCD09JUN) MB	Low energy proton testing to investigate direct ionization. Errors were observed at proton energies near 1MeV and above; All low energy errors were analog (no digital errors detected); Potential direct ionization was observed.	N	5V	2	[12] [13]
ADS5483	Texas Instrument	delidded by TI markings: AZ5483 TI 83K E7N0 G	ADC	Comple mentary Bipolar (BiCom3)	H: (TAMU09MAY) MB (w/Robert MacDowell) P: (IU09AUG) MB	H: LET_{th} <8.6 (no LET SEE); SEL LET_{th} >75 P: SEE σ ranged from 2x10^{-10} cm^2/device at 75MeV to 2.5x10^{-10} cm^2/device at 198MeV.	N	3.3V, 5V	H: 2 P: 4	[13] [14]
FPGA:										
RTAX2000S	Actel	0526	RTAX-S FPGA	Antifuse Tech-nology/ CMOS	H: (TAMU09DEC) MB	SEL LET_{th} >80; 2.5 < SEU LET_{th} <8.6	Y	1,5V Core, 2.5V, 3.3V	2	[15]
XC5VLX30T-1FFG665GU	Xilinx	0849	Virtex V FPGA	65nm CMOS	H: (TAMU09SEPT) MB; P: (UCD09JUN) MB; P: (IU09AUG) MB	H: SEL LET_{th} >75; SEU LET_{th} <2; P: SEUs observed for all energies tested (0.9, 1.4, 2.3, 5.9, 7.8, 13.2, 21.8, and 63.8 MeV); SEU σ = 5x10^{-17} cm^2/bit at 0.9MeV; SEU $σ_{max\ measured}$ = 2x10^{-14} cm^2/bit at ~ 20MeV.	Y	1,2V, 1.8V, 2.5V, 3.3V	3	[17]

Part Number	Manufacturer	LDC	Device Function	Tech-nology	Particle: (Facility/Date) P.I.,	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	App. Spec. Test (Y/N)	Supply Voltage	Sample Size (Number Tested)	Reference
Linear Devices:										
LTC6400	Linear Technology	0746; 0705	Differential Amplifier	SiGe BiCMOS	H: (TAMU09MAY) DC; P: (IU09AUG) DC	H: SEL LET_{th} > 49.6; SET LET_{th} < 7.4 SET σ increases linearly with frequency. SETs from 10 MHz signals are relatively minor. At 100 MHz, the SETs appear mostly as short duration voltage spikes. At 1000 MHz, the majority of SETs "erase" the signal for several cycles. P: SET $\sigma_{max\ measured}$ 1.5×10^{-11} cm^2 for a fluence of 1×10^{12} particles/cm^2, with the device operating at 200 MHz. No SETs were observed at 10 MHz.	N	3 V	2 (May); 1 (Aug)	[18] [19] [20]
THS4304	Texas Instrument	OCT04	Operational Amplifier	SiGe BiCMOS	H: (TAMU09AUG) DC	SET LET_{th} < 4.4 for 200 MHz waveforms, 15.6 for 100 MHz waveforms, and 31.2 for 10 MHz waveforms	N	2.5 V	2	[20] [21]
Memory Devices:										
Part Number: unavailable	Manufacturer: unavailable	LDC and die markings: un-available	Phase Change Memory (PCM)	90nm CMOS Non-volatile Memory	H: (TAMU09AUG) HK, KL; H: (TAMU09DEC) HK, KL	A commercial sample of a 90nm CMOS phase change non-volatile memory was tested for heavy ion SEE tolerance at TAMU. Static and dynamic tests were performed with a variety of test patterns including checkerboard and inverse checkerboard. Static testing indicated that the phase change storage cells were hard to the highest tested LET of 112. No permanent device failures were observed. Even at elevated temperature (70ºC) and V_{dd} +10%, the device did not suffer permanent failures, though SEL was observed. However, the device showed low SEFI threshold at LET below 2.9 suggesting that control circuits are the weak link. Though non destructive, its low SEL LET_{th} below 2.9 cannot be ignored either.	N	2.7; 3.0; 3.6 V	4	N/A
K4B1GO846D-HCH9	Samsung	0813 Markings: SEC813H CH9 GNL037B B	DDR3 SDRAM	65 nm CMOS	H: (TAMU09AUG) RL P: (IU09AUG) RL	H: SEU LET_{th}<2.8; $\sigma_{max\ measured}$ ~10^{-3} cm^2/dev; MCU: LET_{th}~10; $\sigma_{max\ measured}$ ~5×10^{-4} cm^2/dev; Block Error: LETth~2.8; $\sigma_{max\ measured}$ ~5×10^{-4} cm^2/dev; Stuck bits seen near end of run; SEFI seen at high LET, high fluence (10^{-7} cm^2< $\sigma_{max\ measured}$ <10^{-4} cm^2) P: Tested at 25 MHz with PLL disabled. Proton SEU seen with 80 and 198 MeV protons. Block errors seen with 198 MeV protons.	Y	1.8 V	2	[22]

Part Number	Manufacturer	LDC	Device Function	Tech-nology	Particle: (Facility/Date) P.I.,	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	App. Spec. Test (Y/N)	Supply Voltage	Sample Size (Number Tested)	Reference
K9F4G08U0A-PCB0	Samsung	0840; 0843; 0846; 0901; 0907	4Gbit NAND Flash Memory	CMOS	H: (TAMU09MAY) TO; AS H: (TAMU09AUG) TO w/F. Irom testing LDC 0907 only	Bit error LET_{th} ~2.8; Write mode failures were observed at 70ºC at LET 54.8.	N	3.3V for SEU and SEFI, 3.6V (3.3 +10%) for SEL	23	[23] [24]
MT29F4G08AA AWP	Micron	0744	4Gbit NAND Flash Memory	CMOS	H: (TAMU09AUG) TO w/ F. Irom	31< SEL LET_{th} <54.8; 2.8 < destructive failure (erase failure) < 8.4; Bit errors were observed at 2.8; SEFIs were observed at LET 8.4;	N	3.3V	1	[24] [25]
Power Devices:										
CSD16403Q5A	Texas Instrument	0916C 6W.08	25V N-Channel Power MOSFET	Commercial NexFET™ n-channel lat./vert. hybrid	H: (TAMU09DEC) JML	SEB last pass/first fail V_{ds}= 13V/14V for LET=27 (Kr) & 41.5 (Ag), at all test V_{gs}.	N	0Vgs, 5Vgs, 7Vgs	18	[26]
IRH7360SE	International Rectifier	No LDC. Markings R473288-21	Power MOSFET	Gen 4 n-channel VDMOS FET	H: (TAMU09MAR) JML	LET=28.1 (Kr): no failure at $0V_{gs}/400V_{ds}$; Failed at -$15V_{gs}/330V_{ds}$ (last pass $320V_{ds}$). LET=41.9 (Ag): SEGR at $0V_{gs}/210V_{ds}$ (last pass $200V_{ds}$) and at $-15V_{gs}/140V_{ds}$ (last pass $130V_{ds}$).	N	0Vgs; -15Vgs	11	[27]
ISL70001	Intersil	NA (Part in develop-ment)	POL DC/DC Converter	BiCMOS	H: (TAMU09MAY; TAMU09AUG) DC w/Intersil	SEL / SEB / SEGR LETth>86.4 up to 125ºC	N	5.7V	>10	[28]
MSK5820-2.5RH	M.S. Kennedy	0923	Voltage Regulator	Linear Bipolar Hybrid	L: (NRL09OCT) JP	Positive and negative transients were observed (−12 to +100 mV), up to a width of ~225 µs.	Y	V_{in} = 5 V, V_{out} = 2.5 V	1	[29]
MSK5900RH	M.S. Kennedy	0703	Voltage Regulator	Linear Bipolar Hybrid	L: (NRL09OCT) JP	Positive and negative transients were observed (−20 to +40 mV), up to a width of ~200 µs.	Y	V_{in} = 5 V, V_{out} = 2.5 V	1	[30]
TPS79133	Texas Instrument	0710	Voltage Regulator	BiCMOS	L: (NRL09JUN) DC	SET pulse includes a positive and negative voltage spike, with pulse amplitudes = -0.2 V to 0.2 V and pulse width (FWHM) = 10-20 µs for each spike. Pulse amplitude and width increase slightly at elevated temperature (373K).	N	3.3 V	4	[31]
Test Chips:										
Test Vehicle	IBM	No LDC (test chip)	SRAM	45 nm SOI CMOS	P: (UCD09JUN) JP P: (IU09AUG) JP	Completed further mapping of low-energy proton sensitivity. High-energy proton testing was done at approximately 25 MHz for better MCU statistics.	N	0.6-1.2 V	2, com-bined from all tests	[32]
Test Vehicle	Texas Instrument	No LDC (test chip)	SRAM	45 nm bulk CMOS	P: (GSFC09MAY) JP/MX H: (TAMU09MAY) JP/MX P: (UCD09JUN) JP/MX P: (IU09AUG) JP/MX H: (LBNL09SEP) JP/MX [33]	H: SEL observed at effective LETs as low as 30, though portions of SRAM are hard to SEL up to LET 60. P: No SEL observed with 198MeV protons.	N	1.2 V	6, com-bined from all tests	none

Part Number	Manufacturer	LDC	Device Function	Tech-nology	Particle: (Facility/Date) P.I.,	Test Results LET in MeV•cm^2/mg σ in cm^2/device, unless otherwise specified	App. Spec. Test (Y/N)	Supply Voltage	Sample Size (Number Tested)	Reference
Miscellaneous Devices:										
OV5633	Omnivision	No LDC (image sensor)	5 megapixel Image Sensor	CMOS	H: (TAMU09SEPT) CM/MaC	SEL LET_{th} > 87; Fluence corrected for time part spent in SEFI mode.	N	Core 1.5 V; I/O 1.8V; Analog 2.8 V; Pixel 2.8 V; MIPI 1.5V	4	none
Part Number: unavailable	Manufacturer: unavailable	LDC and die markings: un-available	Read Out Integrated Circuit (ROIC)	0.5 µm CMOS	H: (TAMU09SEPT) CM	No SEL observed at 40 K, 48 K and 80 K to $\sigma_{limiting}$ ~2x10^{-7} cm^2 for LET = 102; Single recoverable SEL event observed at 32 K to fluence = 3.5x10^6 cm^{-2} at LET = 102; At 20 K, ROIC sensitive to SEL for 12 = LET < 102 with 2.0x10^{-5} < σ < 3.7x10^{-4} cm^2 (lowest test LET). At 300 K, SEL σ ~ 1x10^{-3} cm^2 at LET = 87	N	5.7 V	2	[34]

IV. Test Results and Discussion

As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [11] describing in further detail the test method, SEE conditions/parameters, test results, and graphs of data.

This section contains summaries of testing performed on a selection of featured parts.

A. *Texas Instruments ADS5483 ADC*

This study was undertaken to determine the Single Event Effects (SEE), susceptibility of the Texas Instruments (TI) ADC converter: ADS5483. The DUTs were evaluated with heavy ions and protons.

There was a total of 7 ADC tested. 2 were made available for heavy ion testing, including 1 control sample. 4 devices were made available for proton testing. A TI Evaluation board with one embedded ADC (DUT) was used as a daughter card that was physically connected to the NASA Goddard low cost digital tester (LCDT). The TI Evaluation board number is ADS548xEVM. The identification information for these ADCs is as follows:

Test Chip: ADS5483
Lot # unknown - delidded by TI
Markings:
AZ5483
TI 83K
E7N0 G

The DUT technology is Texas Instruments complementary bipolar process BiCom3x. The following are some of the ADS5483 Features (please refer to the ADS5483 datasheet for a complete description):

- 16-bit resolution. 78 dBFS Noise Floor
- 170MSPS Sample Rate
- SFDR = 95dBc
- On-Chip High Impedance Analog Buffer
- Efficient DDR LVDS-Compatible Outputs
- Power-Down Mode: 70mW
- Industrial Temperature Range: -40˚C to 85˚C
- 3 Vpp Differential Input Range
- 5 V or 3.3 V Power supply

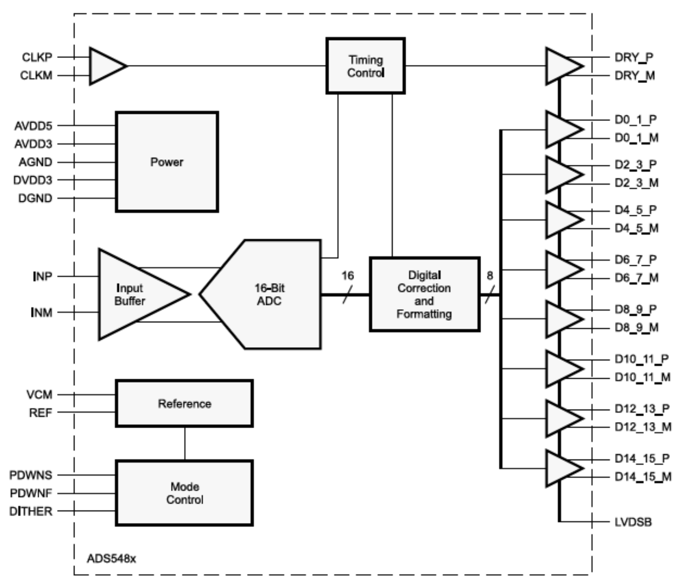

Fig. 1. Functional Block Diagram of the ADS5483.

For reliable SEU response analysis, it is important to filter out the non-SEU noise that is introduced from both the test vehicle and the ADC device. Subsequently, prior to radiation testing, system noise was measured. A minimal error-bound (EB) was calculated per test set-up such that no ADC output code errors existed during operation and pre-irradiation. The EB code value can be translated to its corresponding voltage level (V_{EB}) as illustrated in (1).

$$V_{EB} = \frac{EB * Vpp}{2^{Nb}} \quad (1)$$

Concerning (1), Nb is the number of ADC output bits (16-bits for the ADS5483) and V_{pp} is the peak-to-peak manufacturer supplied voltage range ($3V_{pp}$ for the ADS5483).

Regarding heavy ion testing, the ADS5483 DUT was tested at the TAMU using a 15 MeV/amu tune at room temperature. All tests were run with 10^3 <flux rate < 10^4 particles/cm^2/s. Effective LETs ranged from 2.5 MeV•cm^2/mg to 83.4 MeV•cm^2/mg by varying the ion and by varying the angle of incidence. All proton tests were performed at IUCF. Data was obtained for two proton energies: 78 Mev and 198 MeV. The ADC devices were operated at nominal room temperature using active cooling. A function generator was utilized as the clock and data input to the ADC. Measurements were taken by interfacing the ADC 16-bit digital outputs to the LCDT. The LCDT processed the output data and reported errors to the user host computer.

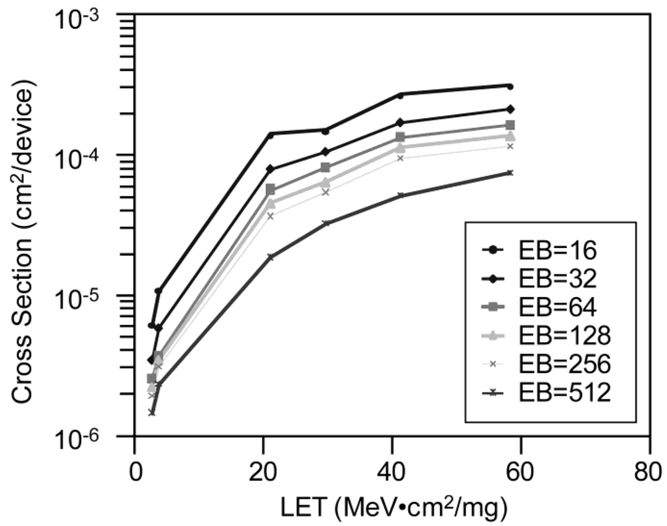

Fig. 2. Heavy Ion SEU Error Cross Sections.

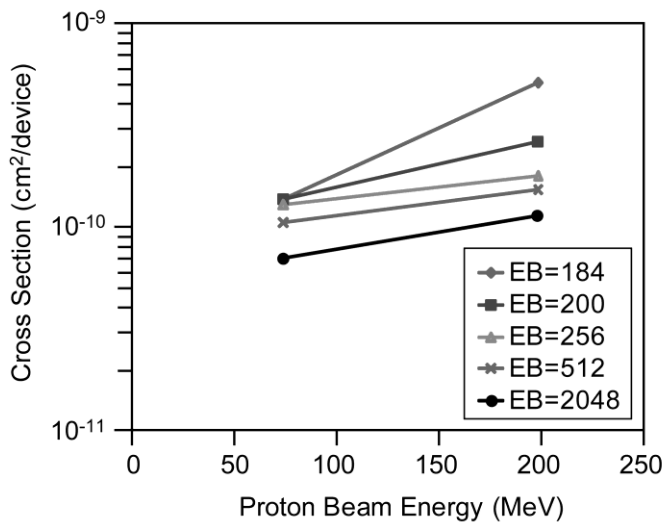

Fig. 3. Proton SEU Error Cross Sections.

As a summary, the SEU/SET response of the ADS5483 consists of:

1. Code upsets that only last for one ADC clock cycle.
2. Code upsets that last for multiple ADC clock cycles (bursts).
   a. Heavy ion bursts were not as frequent as proton bursts. The longest heavy ion burst lasted for 39 ADC clock cycles.
   b. Bursts due to 198 MeV proton strikes could last thousands of ADC clock cycles. However, at EB=7.8 mV and above, the burst duration and frequency is significantly reduced. This is due to the fact that most of the burst upsets were small upsets from the expected values – i.e. the errors jittered around the expected values. This suggests that the analog circuitry has a significant sensitivity to 198 MeV protons.
   c. Most upsets due to 73 MeV protons were single ADC clock cycle upsets.
3. No clock losses were observed – however, this is still under investigation.
4. SEU/SET rate did not increase significantly with frequency (10 MHz vs. 100 MHz) [13], [14].

B. *Actel RTAX2000S RTAX-S FPGA EDAC Memory Tests*

This study was undertaken to determine the single event destructive and transient susceptibility of the internal memory structures embedded in the RTAX-S FPGA family of devices. The DUTs were configured to have various forms of active embedded memory structures. The memory and its supportive circuitry were monitored for SET and SEU induced faults by exposing them to a heavy ion beam. The purpose of this RTAX-S memory evaluation was to enhance prior testing of the device. The study included both static and dynamic modes of memory control and operation for memory configurations that utilized the embedded EDAC circuitry provided by Actel versus memory configurations that did not contain EDAC. It is important to note that the embedded EDAC circuitry does not reside in the hardened by design user-cells of the RTAX. Therefore, the embedded circuitry is assumed to be more susceptible than custom user designed EDAC that would utilize the RTAX-S hardened cells.

There was one RTAX-S device that contained the memory configuration under evaluation. The sample size per device (in this case) was not the focus since they are production- high speed parts with very little variation across the CMOS process. The emphasis was to test variations over the design state space. The devices were manufactured on an advanced 0.15μm CMOS Antifuse Process Technology with 7 layers of metal. The manufacturer is Actel. The devices tested had LDC of 0526.

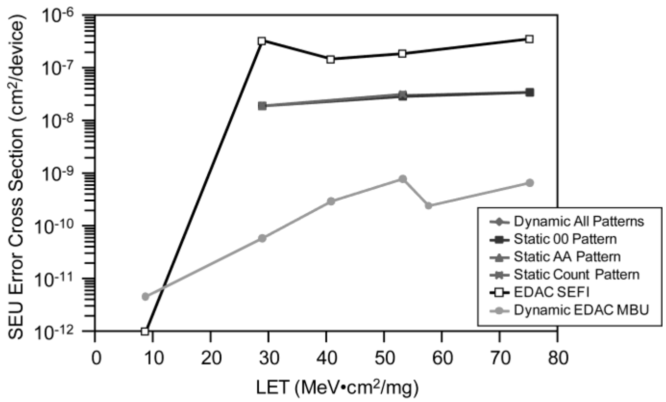

Fig. 4. SEU Error Cross Sections. Static and dynamic memory reads were evaluated for several patterns for memory structures with and without EDAC controls.

Fig. 4 illustrates that the memory bit-cell SEU cross sections over all data patterns were statistically equivalent. Dynamic tests consisted of read-write-modify cycles. Regarding memory cell SEU-cross sections, there was no statistical difference between dynamic memory operations during DUT irradiation versus static memory operation. With dynamic testing, multiple bit failures (MBUs) per address did occur at 8.5 MeV•cm^2/mg. Because the EDAC structures are Single Error Correct Double Error Detect (SECDED), memory reads that utilized the embedded EDAC structures had failures. No testing was performed below 8.5 MeV•cm^2/mg, therefore no on-set for memory MBU and EDAC failure has been determined. For LET > 20 MeV•cm^2/mg, EDAC SEFI's also occurred. An EDAC SEFI pertains to the event of the EDAC circuitry becoming stuck in a state where it cannot correct data and eventually corrupts good data. EDAC SEFIs at LETs >20 MeV•cm^2/mg were significant and can be avoided by the user creating a custom EDAC with the RTAX-S user fabric [15]. Note, also see J. George, et al., [16].

C. Linear Technology LTC6400 Differential Output Amplifier/ADC Driver

The LTC6400 is fabricated with the JAZZ-TOWER 0.35µm SiGe BiCMOS process. Two parts were irradiated at room temperature with the devices operating at V_{CC} = 3 V, V_{CM} = 1.25 V, sine wave inputs of 140 mV_{pp} (large signal) or 2 mV_{pp} (small signal), at frequencies of 10, 100, and 1000 MHz. Two ion species were used for this experiment: Ar and Kr.

Fig. 5 shows the SET cross-sections from large signals at 10, 100, and 1000 MHz. We observed SETs down to the lowest LET of 7.4 MeV•cm^2/mg for all frequencies of operation. The SET cross-sections increase linearly with increasing frequency. The worst case transients occur at 1000 MHz, where several cycles of the signal are erased from an SET. Fig. 6 shows an SET at 1000 MHz. No latchup events were observed. The supply current values remained relatively unchanged, at ~ 90 mA, throughout irradiation.

Additionally, we found that the LTC6400 was robust against high energy protons, with relatively low SET cross-sections. We irradiated 2 parts with 198 MeV protons. The increase in SET error cross-sections from 0° to 60° for DUT3 is unlikely due to angular effects that result from nuclear reactions, since the final 0° incident run produced a larger error cross-section than the initial normal incident run. We irradiated DUT4 at normal incidence to examine the effects of total dose and displacement damage on SET sensitivity. The significant scatter in the dataset suggests that the SET cross-sections more likely follow a Poisson distribution, and do not correlate strongly with accumulated dose. The different lot date codes of the parts may also contribute to the relatively large difference in the magnitudes of SET cross-sections.

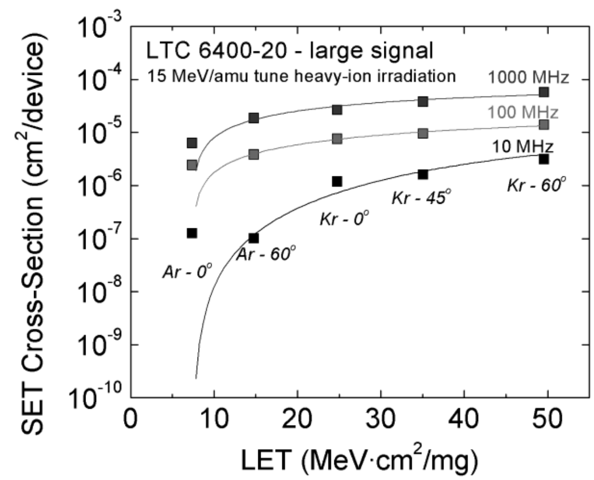

Fig. 5. Heavy-ion-induced SET error cross-sections for large signals at 10, 100 MHz, and 1 GHz.

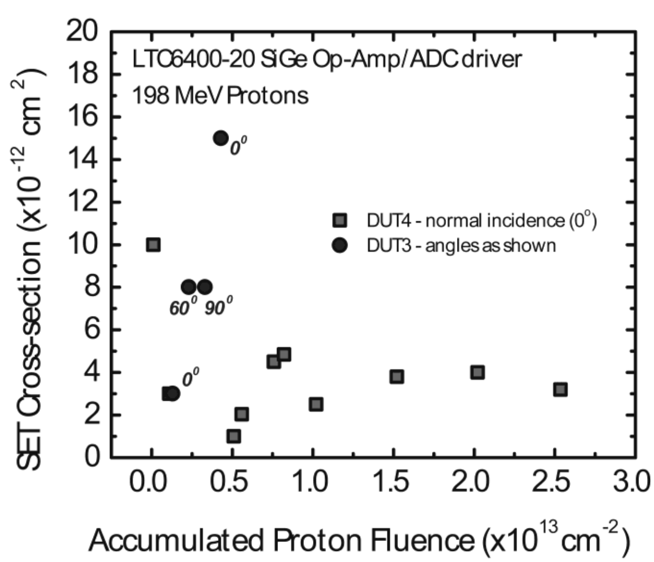

Fig. 6. SET cross section vs. accumulated dose for the LTC6400 operating at 200 MHz, irradiated with 198 MeV protons to a fluence of 1 × 10^{12} particles/cm^2.

D. Texas Instruments CSD16403QA Commercial Power MOSFET

This study was undertaken to determine the single event gate rupture (SEGR) and burnout (SEB) susceptibility of the commercial CSD16403QA power MOSFET under heavy ion irradiation. The device is a 100 amp, 25 volt n-channel power MOSFET, manufactured under Texas Instruments' recently acquired CICLON NexFET^{TM} commercial process technology. The NexFET technology is a hybrid lateral-vertical power MOSFET (Fig. 7) featuring a lateral channel under a planar gate connecting the source to the lightly doped drain extension region (LDD), and a highly doped vertical drain "sinker" that brings the current flow vertically down to the backside drain contact. We believe that this test is the first to evaluate the heavy-ion response for this device type.

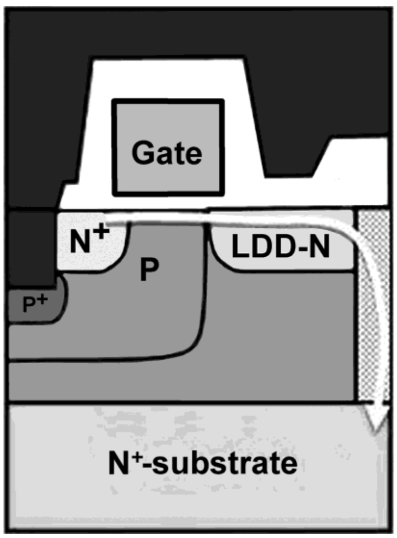

Fig. 7. Cartoon showing the structure of a n-type NexFET™ power MOSFET. From: Electronics Design, Strategy, News, 12 Feb 2009.

Tests were conducted at normal incidence to the surface. Each device was biased at one of three gate-source voltage (Vgs) biases, and the drain-source voltage (Vds) was incremented between beam runs until device failure was observed. Currents were monitored at the gate and drain nodes during testing, and voltage transients were recorded across a small sense-resistor placed behind the drain stiffening capacitor. All device failures occurred during irradiation and were due to single event burnout, although in each instance the gate ruptured. As can be seen in Fig. 8, the SEE safe operating area is 52% of the maximum rated drain voltage, independent of the gate bias applied during testing. This gate-voltage independence is a hallmark of single-event burnout. In addition, both krypton at an incident LET of 27.4 MeV•cm^2/mg and silver at an incident LET of 40.5 MeV•cm^2/mg yielded the same SEE response curves.

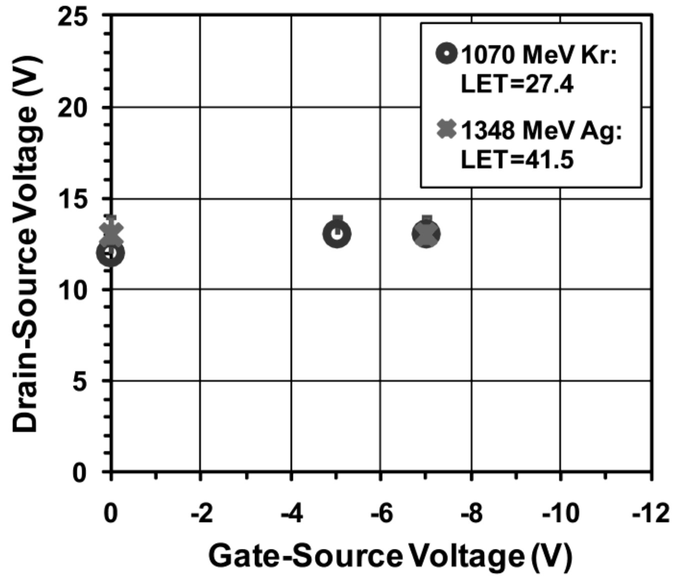

Fig. 8. SEE response curve.

Efforts to evaluate a p-channel NexFET were inconclusive due to the presence of an irremovable heat sink on top of the die obstructing more than 80% of the active region. As p-channel power MOSFETs do not suffer SEB, additional tests will reveal whether these commercial p-type structures will be naturally rugged under a heavy-ion space environment. [26]

E. M.S. Kennedy Voltage Regulators MSK5900RH and MSK5820-2.5RH

We undertook this study to characterize the application-specific SET behavior of the MSK5900RH and MSK5820-2.5RH low dropout voltage regulators using pulsed laser irradiation. Both regulators are hybrid integrated circuits, which contain controller circuitry that governs a power PNP bipolar transistor. The controller circuitry, manufactured by Linear Technology, is the LT1573 in the case of the MSK5900 and the RH1573K in the case of the MSK5820. The LT1573/RH1573 is a low dropout PNP regulator driver. The RH1573K uses the same mask set as the LT1573, but has a different passivation to improve its total ionizing dose response.

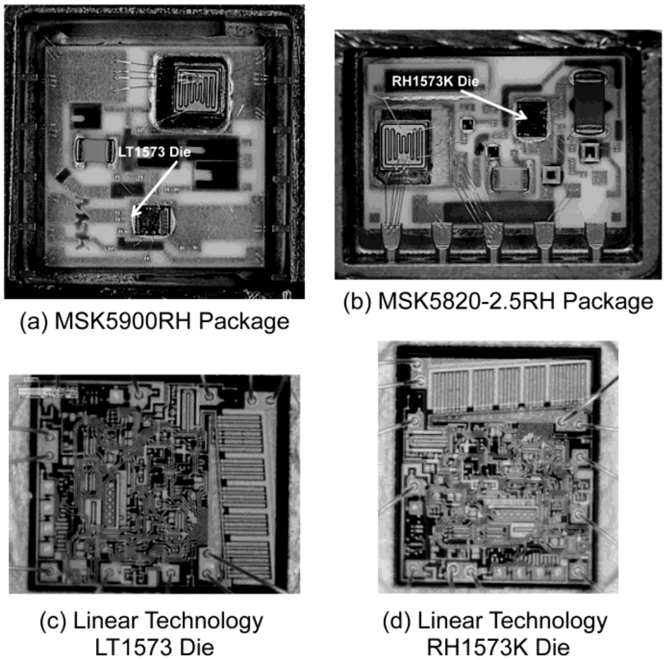

Fig. 9. Micrographs of the MSK5900RH and MSK5820-2.5RH bipolar hybrid integrated circuits and the PNP driver regulator dice within. Note that (c) and (d) have been rotated so that their orientation is the same as in (a) and (b). The views in (c) and (d) are the same as what the laser sees through the 100x objective.

Package and die micrographs of the MSK5900RH/LT1573 and MSK5820-2.5RH/RH1573 are shown in Fig. 9. The MSK5900RH is packaged in a 12-pin flatpack and the MSK5820-2.5RH is packaged in a 5-pin single-inline package. It is clear from Figs. 9(c) and (d) that the LT1573 and RH1573 have the same mask set. The main difference is that the MSK5900RH is a positive adjustable regulator tuned with an external resistor network and the MSK5820-2.5RH is a fixed positive voltage regulator. Both regulators were configured with a 5.0 V input and a +2.5 V output.

We used the pulsed laser facility at the Naval Research Laboratory to perform single-photon absorption on the M.S. Kennedy voltage regulators with a 590 nm wavelength beam. The pulse energy for these experiments was in excess of an equivalent LET of 100 MeV•cm^2/mg.

We scanned the laser spot across the entire surface of both the LT1573 in the MSK5900RH and the RH1573K in the MSK5820-2.5RH. Two load conditions were used for each component. The MSK5900RH was irradiated with 25 mA and 138 mA loads while the MSK5820-2.5RH was irradiated with 0.515 A and 2.45 A loads. Voltage transients were observed with all load conditions on each component. We observed both positive and negative transients (-20 to +40 mV), up to a width of approximately 200 µs on the MSK5900RH. The MSK5820-2.5RH also showed both positive and negative transients (-12 to +100 mV), up to a width of approximately 225 µs. These results are shown graphically in Fig. 10 and Fig. 11 [29] [30].

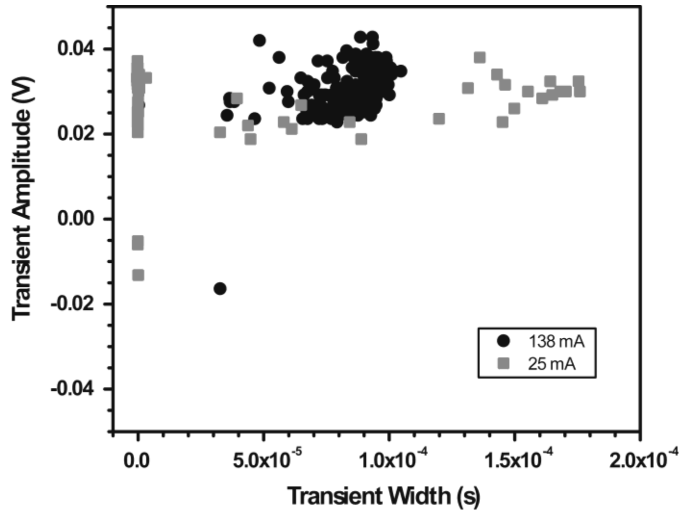

Fig. 10. MSK5900RH transients.

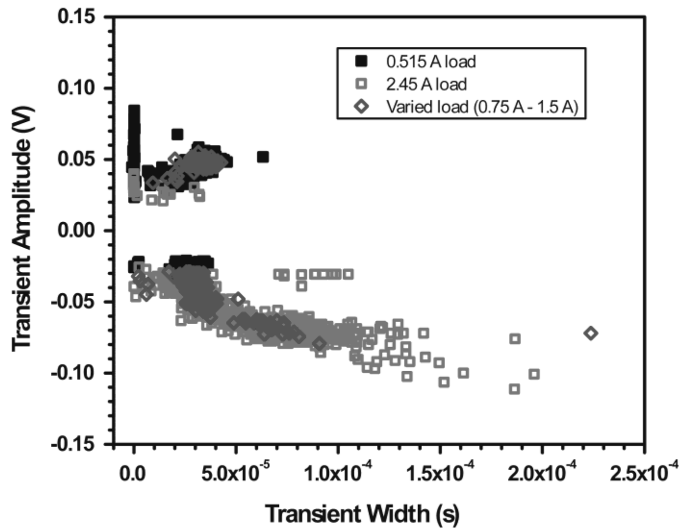

Fig. 11. MSK5820-2.5RH transients.

F. Intersil ISL70001 Point-of-load DC/DC Converter

The ISL70001SRH is a new point-of-load (POL) DC/DC converter developed by Intersil Coporation. The part has been qualified for total ionizing dose irradiation. Here we give a short summary of the single event effects performance from heavy-ion irradiations. Details of the part's radiation performance can be found in Intersil's publication. [28]

The ISL70001SRH was found to be free of SEL/SEB/SEGR up to an LET of 86.4 MeV•cm^2/mg, with the device operating at an input voltage of 5.7 V, output current of 7 A, output voltage of 1.8 V, and case temperature up to 125^{o}C.

The redundant PWM loop design of the ISL70001SRH is effective in limiting SETs. The worst case SET at an LET of 86.4 MeV•cm^2/mg was found to cause less than 1% change in the output voltage.

A SEFI phenomenon of the Softstart function was observed at an LET of 84.6 MeV•cm^2/mg and 3 V input voltage only. The ISL70001SRH shuts down and then restarts normally through the Softstart function. The estimated cross section for this phenomenon is 1.4 x 10^{-6} cm^2 at an LET of 84.6 MeV•cm^2/mg and 3V input. With a 5 V input, the SEFI cross section increased to ~ 6.5 x 10^{-8} cm^2. [28]

V. Summary

We have presented current data from SEE testing on a variety of mainly commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

VI. Acknowledgment

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