MODELING OF SONOS MEMORY CELL ERASE CYCLE

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INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

ERASE MODEL DEVELOPMENT

- Applying Gauss’ Law to the floating gate provides
  \[ Q_{FG} = C_{oxg} \left( V_{FG} - V_{GB} + \frac{C_{oxg}}{C_{oxg} + C_{tun}} (V_{FG} - V_{MS}) \right) + C_{oxg} (V_{FG} - V_{DB}) \]
  \[ + C_{oxg} (V_{FG} - V_{SB}) \]  
  \[ (1) \]
- During Erase cycle device is in accumulation mode
  \[ \phi_{b} \text{ should be on the order of a few hundredths of a volt and can be neglected} \]
- Taking the time derivative of equation 1, and realizing that
  \[ \frac{dQ_{FG}}{dt} = -i_{tun} \]
  \[ \frac{dQ_{FG}}{dt} = -i_{tun} = C_{oxg} \left( \frac{dV_{FG}}{dt} \right) - \frac{C_{oxg}}{C_{tun}} \left( \frac{dV_{FG}}{dt} \right) \]  
  \[ (2) \]
- Rearranging equation 2 to solve for the floating gate voltage provides
  \[ \frac{dV_{FG}}{dt} = \frac{C_{oxg}}{C_{tun}} \left( \frac{dV_{FG}}{dt} \right) - \frac{C_{oxg}}{C_{tun}} \left( \frac{dV_{FG}}{dt} \right) \]
  \[ \frac{dV_{FG}}{dt} = -\frac{i_{tun}}{C_{oxg}} \]  
  \[ (3) \]
- Equation 3 can be solved for the floating gate voltage by numerical methods.
- Now the tunneling Electric Field can be calculated.
  \[ E_{tun} = \frac{V_{FG} - \phi_{S}}{t_{tun}} \]  
  \[ (4) \]
- Then the tunnel current can be calculated using the Fowler-Nordheim equation
  \[ i_{tun} = e \alpha \beta \frac{V_{FG} - \phi_{S}}{t_{tun}} \exp \left( \frac{H_{Fnerase}}{E_{tun}} \right) \]
  \[ (5.1) \]
  \[ i_{tun} = e \alpha \beta \frac{V_{FG} - \phi_{S}}{t_{tun}} \exp \left( \frac{H_{Fnerase}}{E_{tun}} \right) \]
  \[ (5.2) \]
- Fowler-Nordheim constants
  \[ \alpha = 2.37 \times 10^{8} \]
  \[ \beta = 1.23 \times 10^{-6} \]
- Now an updated value for the floating gate charge can be obtained from
  \[ \frac{dQ_{FG}}{dt} = -i_{tun} \]
- Finally an updated value for the threshold voltage can be calculated using
  \[ V_{th} = V_{th0} - \frac{Q_{FG}}{C_{oxg}} \]  
  \[ (7) \]
- A software flowchart is shown in Figure 2.
- A logarithmic series was implemented for time steps t.
- Each of the equations was solved for each time step.

RESULTS

- For the SONOS erase operation \( V_{GB} \) was set to -8 VDC, \( V_{DB} \) and \( V_{SB} \) were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.
- The calculated tunnel current is shown in Figure 4. The calculated threshold voltage and the threshold voltage from the Cho & Kim device is shown in Figure 5.

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

REFERENCES


Figure 1: SONOS Device Layout

- SONOS Device parameters
  - Tunneling oxide thickness (\( t_{tun} \)) – 6nm
  - Floating gate thickness – 6nm
  - Oxide thickness (\( t_{ox} \)) – 7nm
  - Channel length (\( l \)) – 0.35\( \mu \)m
  - Device width (\( w \)) – 0.25\( \mu \)m
  - Gate length (\( l' \))
  - Gate overlap over Drain/Source (\( x_{j} \))
- Calculated Capacitances
  - \( C_{oxg} = \frac{C_{ox}/t_{ox}}{w \cdot l'} \)
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- \( \gamma = l + 2x_{j} \)
- \( A_{in} = w \cdot l' \)