MODELING OF SONOS MEMORY CELL ERASE CYCLE

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INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

SONOS Device

- The modeled SONOS device is shown in Figure 1.

![SONOS Device Layout](image)

Figure 1: SONOS Device Layout

- SONOS device parameters
  - Tunneling oxide thickness ($t_{tunnel}$) – 6nm
  - Floating gate thickness – 6nm
  - Oxide thickness ($t_o$) – 7nm
  - Channel length ($l$) – 0.35µm
  - Device width ($w$) – 0.25µm
  - Gate length ($l'$)
  - Gate overlap over Drain/Source ($x_j$)

- Calculated Capacitances
  - $C_{sg} = (c_{sg}/w) l'$
  - $C_{otun} = (c_{otun}/w) A_{un}$
  - $C_{cg} = (c_{cg}/w) A_{un} x_j$
  - $C_{tun} = (c_{tun}/w) x_j$
  - $C_{oxg} = (c_{oxg}/w) x_j$
  - $C_{gs} = C_{sg} + C_{otun} + C_{cg} + C_{tun}$
  - $C_{oxs} = (c_{oxs}/w) x_j$
  - $l' = l + 2x_j$
  - $A_{un} = w x_j$

ERASE MODEL DEVELOPMENT

- Applying Gauss’ Law to the floating gate provides

$$Q_{FG} = C_{sg} (V_{FG} - V_{GB}) + C_{otun} (V_{FG} - V_{DB}) + C_{cg} (V_{FG} - V_{BG}) + C_{oxg} (V_{FG} - V_{BG})$$

During Erase cycle device is in accumulation mode

- $V_o$ should be on the order of a few hundredths of a volt and can be neglected
- Taking the time derivative of equation 1, and realizing that

$$dQ_{FG}/dt = dV_{FG}/dt$$

Rearranging equation 2 to solve for the floating gate voltage provides

$$(dV_{FG}/dt) = (C_{tun} dV_{GB}/dt) - C_{cg} (dV_{GD}/dt)$$

Equation 3 can be solved for the floating gate voltage by numerical methods.

- Now the tunneling Electric Field can be calculated.

$$E_{tun} = (V_{FG} - V_{GB})/t_{tun}$$

Then the tunnel current can be calculated using the Fowler-Nordheim equation

$$I_{tun} = I_{tun,free} A_{un} E_{tun}^2 \exp(-\phi_{Fnerase}/E_{tun})$$

For the SONOS erase operation $V_{GB}$ was set to -8 VDC, $V_{DB}$ and $V_{SB}$ were set to 0 VDC.

RESULTS

- For the SONOS erase operation $V_{GB}$ was set to -8 VDC, $V_{DB}$ and $V_{SB}$ were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.

![Tunnel Current](image)

Figure 4: Tunnel Current

![Threshold Voltage](image)

Figure 5: Threshold Voltage

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

REFERENCES