MODELING OF SONOS MEMORY CELL ERASE CYCLE

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INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

SONOS Device

- The modeled SONOS device is shown in Figure 1.

![Figure 1: SONOS Device Layout](image1.png)

- The Floating gate voltage is shown in Figure 3.

ERASE MODEL DEVELOPMENT

- Applying Gauss’ Law to the floating gate provides

  \[ \frac{dV_{FG}}{dt} = \sum_{i} \left( \frac{C_{ox,i}}{C_{ox}} \right) \left( V_{FG} - V_{GB} \right) + \frac{C_{tun}}{C_{ox}} \left( V_{FG} - V_{DB} \right) + \frac{C_{oxs}}{C_{ox}} \left( V_{FG} - V_{GS} \right) \]

- During erase cycle device is in accumulation mode
  - \( \phi_0 \) should be on the order of a few hundredths of a volt and can be neglected
  - Taking the time derivative of equation 1, and realizing that
    \( \frac{dQ_{FG}}{dt} = \frac{dV_{FG}}{dt} \cdot C_{ox} \)
  - Rearranging equation 2 to solve for the floating gate voltage provides
    \( \frac{dV_{FG}}{dt} = \frac{C_{tun}}{C_{ox}} \cdot \frac{dV_{DB}}{dt} + \frac{C_{oxs}}{C_{ox}} \cdot \frac{dV_{GS}}{dt} \)

- Applying Gauss’ Law to the floating gate provides

\[ \frac{dV_{FG}}{dt} = \frac{C_{tun}}{C_{ox}} \cdot \frac{dV_{DB}}{dt} + \frac{C_{oxs}}{C_{ox}} \cdot \frac{dV_{GS}}{dt} \]

- Equation 3 can be solved for the floating gate voltage by numerical methods.
- Now the tunneling Electric Field can be calculated.

\[ E_{tun} = \frac{V_{FG} - \phi_S}{t_{ox,tun}} \]

- Then the tunnel current can be calculated using the Fowler-Nordheim equation

\[ I_{tun} = \alpha \cdot F_{tun} \cdot A_{tun} \cdot E_{tun}^2 \cdot \exp \left( -\beta \cdot E_{tun} \right) \]

- For the SONOS erase operation \( V_{GB} \) was set to -8 VDC, \( V_{DB} \) and \( V_{GS} \) were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.

RESULTS

- The calculated tunnel current is shown in Figure 4. The calculated threshold voltage and the threshold voltage from the Cho & Kim device is shown in Figure 5.

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

REFERENCES