MODELING OF SONOS MEMORY CELL ERASE CYCLE
THOMAS A. PHILLIPS\textsuperscript{a}, TODD C. MACLEOD\textsuperscript{a}, and FAT D. HO\textsuperscript{b}

\textsuperscript{a}National Aeronautics and Space Administration, Marshall Space Flight Center, Huntsville, Alabama, 35812, U.S.A.
\textsuperscript{b}The University of Alabama in Huntsville, Department of Electrical and Computer Engineering, Huntsville, Alabama 35899, U.S.A.

INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

ERASE MODEL DEVELOPMENT

- Applying Gauss’ Law to the floating gate provides
  \[ Q_{FG} = C_{fg}(V_{FG} - V_{GB}) + C_{ox}(V_{FG} - \phi) + C_{sg}V_{FG} \]
  \[ V_{FG} = \frac{Q_{FG}}{C_{fg}} \]  \( (1) \)
- During Erase cycle device is in accumulation mode
  - \( \phi \) should be on the order of a few hundredths of a volt and can be neglected
- Taking the time derivative of equation 1, and realizing that
  \[ \frac{dQ_{FG}}{dt} = \frac{dC_{fg}}{dt} \frac{dV_{FG}}{dt} = \frac{dC_{FG}}{dt} \frac{dV_{FG}}{dt} \]
  \[ \text{Cox}(V_{FG} - \phi) \]
- Rearranging equation 2 to solve for the floating gate voltage provides
  \[ (dV_{FG}/dt) = C_{fg}(dV_{BE}/dt) - I_{tun}/C_{total} \]  \( (3) \)
- Equation 3 can be solved for the floating gate voltage by numerical methods.
- Now the tunneling Electric Field can be calculated.
  \[ E_{tun} = \frac{V_{FG} - \phi}{L_{tun}} \]  \( (4) \)
- Then the tunnel current can be calculated using the Fowler-Nordheim equation
  \[ I_{tun} = \frac{F_{n_ERASE}}{E_{tun}} L_{tun} \exp(-\alpha E_{tun}) \]  \( (5.1) \)
  \[ I_{tun} = \frac{F_{n_ERASE}}{E_{tun}} L_{tun} \exp(-\alpha E_{tun}) \]  \( (5.2) \)
- Fowler-Nordheim constants
  \[ F_{n_ERASE} = 1.23e-6 \]  \[ \alpha = 2.37e+8 \]
- Now an updated value for the floating gate charge can be obtained from
  \[ \frac{dQ_{FG}}{dt} = -I_{tun} \]
- Finally an updated value for the threshold voltage can be calculated using
  \[ V_{th} = V_{FG} - \frac{Q_{FG}}{C_{fg}} \]  \( (7) \)

RESULTS

- For the SONOS erase operation \( V_{GB} \) was set to -8 VDC, \( V_{DB} \) and \( V_{SB} \) were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

REFERENCES