MODELING OF SONOS MEMORY CELL ERASE CYCLE

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INTRODUCTION

- Utilization of Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile semiconductor memories as a flash memory has many advantages.
- These electrically erasable programmable read-only memories (EEPROMs) utilize low programming voltages, have a high erase/write cycle lifetime, are radiation hardened, and are compatible with high-density scaled CMOS for low power, portable electronics.
- In this paper, the SONOS memory cell erase cycle was investigated using a nonquasi-static (NQS) MOSFET model.
- Comparisons were made between the model predictions and experimental data.

SONOS Device

- The modeled SONOS device is shown in Figure 1.
- The calculated tunnel current is shown in Figure 4.
- The actual device parameters

\[ \begin{align*}
C_{\text{oxg}} &= \varepsilon_{\text{ox}}/t_{\text{ox}} \\
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C_{\text{oxg}} &= \varepsilon_{\text{ox}}/t_{\text{ox}} \\
\gamma &= 1 + 2 \chi \\
A_{\text{int}} &= w^l
\end{align*} \]

RESULTS

- For the SONOS erase operation $V_{\text{GB}}$ was set to -8 VDC, $V_{\text{DB}}$ and $V_{\text{SB}}$ were set to 0 VDC.
- The calculated floating gate voltage is shown in Figure 3.

ERASE MODEL DEVELOPMENT

- Applying Gauss' Law to the floating gate provides

\[ Q_{\text{FG}} = C_{\text{oxg}} \left( V_{\text{FG}} - V_{\text{GB}} \right) + C_{\text{oxg}} \left( V_{\text{FG}} - V_{\text{MS}} \right) + C_{\text{oxg}} \left( V_{\text{FG}} - V_{\text{DB}} \right) + C_{\text{oxg}} \left( V_{\text{FG}} - V_{\text{BD}} \right) \]

- During Erase cycle device is in accumulation mode

\[ \phi_0 \text{ should be on the order of a few hundredths of a volt and can be neglected} \]

- Taking the time derivative of equation 1, and realizing that

\[ dQ_{\text{FG}}/dt = -I_{\text{tun}} \text{ leads to} \]

\[ dQ_{\text{FG}}/dt = -I_{\text{tun}} = C_{\text{oxg}} \left( dV_{\text{FG}}/dt \right) - C_{\text{oxg}} \left( dV_{\text{DB}}/dt \right) \]

- Rearranging equation 2 to solve for the floating gate voltage provides

\[ (dV_{\text{FG}}/dt) = \frac{C_{\text{oxg}} (dV_{\text{FG}}/dt) - C_{\text{oxg}} (dV_{\text{DB}}/dt)}{C_{\text{oxg}}} \]

- Equation 3 can be solved for the floating gate voltage by numerical methods.

- Now the tunneling Electric Field can be calculated.

\[ E_{\text{tun}} = \frac{V_{\text{FG}} - V_{\text{DB}}}{t_{\text{ox}}} \]

- Then the tunnel current can be calculated using the Fowler-Nordheim equation

\[ I_{\text{tun}} = \frac{C_{\text{oxg}} E_{\text{tun}}^2}{\alpha \sqrt{\pi}} \exp(-\beta \sqrt{E_{\text{tun}}}) \]

- Rearranging equation 2 to solve for the floating gate charge

\[ \frac{dQ_{\text{FG}}}{dt} = -I_{\text{tun}} = E_{\text{tun}} \frac{dV_{\text{FG}}}{dt} \]

- Finally an updated value for the threshold voltage can be calculated using

\[ V_{\text{th}} = V_{\text{FG,0}} - \left( Q_{\text{FG}}/C_{\text{oxg}} \right) \]

- A software flowchart is shown in Figure 2.

CONCLUSION

- A nonquasi-static model was developed for the SONOS memory cell erase cycle.
- The floating gate voltage, tunnel current, and threshold voltages were calculated based on the SONOS device parameters.
- The calculated threshold voltage curve had a slightly different slope than the threshold voltage curve from the Cho & Kim device, but there was still fairly good agreement between the two curves.

REFERENCES