CHARACTERISTICS OF A NONVOLATILE SRAM MEMORY CELL UTILIZING A FERROELECTRIC TRANSISTOR

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Abstract

The SRAM cell circuit is a standard for volatile data storage. When utilizing one or more ferroelectric transistors, the hysteresis characteristics give unique properties to the SRAM circuit, providing for investigation into the development of a nonvolatile memory cell. This paper discusses various formations of the SRAM circuit, using ferroelectric transistors, n-channel and p-channel MOSFETs, and resistive loads. With varied source and supply voltages, the effects on the timing and retention characteristics are investigated, including retention times of up to 24 hours.

Keywords: SRAM, nonvolatile, ferroelectric
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Introduction

The SRAM cell is a standard circuit for volatile memory storage. When one more ferroelectric field-effect transistors (FeFETs) are introduced into the circuit, it is possible to develop a nonvolatile memory cell. Ferroelectric-based memory cells offer benefits over existing nonvolatile memories, such as FLASH. While FLASH may offer lower cost and better storage densities, ferroelectric memory offers the potential for faster performance, lower power consumption and voltage requirements, and more write cycles.

The focus of this series of experiments was to investigate the performance of a ferroelectric-based SRAM cell, specifically the response time of Node 2 with respect to an applied or removed voltage at Node 1, and the overall capability of the circuit to perform as a nonvolatile memory cell.

SRAM Circuit Configuration

An SRAM circuit was constructed in various configurations utilizing traditional MOSFETs and FeFETs as driver transistors. The FeFETs were provided by Joe Evans of Radiant Technologies, Inc. in Albuquerque, New Mexico. The FeFETs were NMOS transistors and featured a channel width of 400 um and a channel length of 4 um. PMOS FeFETs were not available for SRAM testing.

Some of the key configuration differences investigated were:

- The impact of placing a single FeFET into the SRAM circuit on the Node 1 side of the circuit, with a traditional n-channel MOSFET at Node 2
- The impact of placing a single FeFET into the SRAM circuit on the Node 2 side of the circuit, with a traditional n-channel MOSFET at Node 1
- The impact of replacing both n-channel MOSFETs with FeFETs
- The usage of PMOS transistors as loads in comparison with resistors
- The effect of different load resistor values

Summary

When utilizing one or more ferroelectric transistors, the hysteresis characteristics give unique properties to the SRAM circuit, providing for investigation into the development of a nonvolatile memory cell. Tests proved that it was possible for the circuit to retain a stored value for nearly one day with supply power removed. In addition to retention, the timing characteristics with ferroelectric transistors at both Nodes 1 and 2 show similar results to those of the traditional n-channel MOSFETs. Also, the SRAM cell results in quicker response times for lower load resistances, with 5 kOhm being the optimal case. Overall, the SRAM cell using ferroelectric transistors performs rather well as a nonvolatile memory cell, even though the circuit was not optimized for memory retention applications.

References:

When replacing the PMOS loads with resistors, lower resistances provide quicker response times at Node 2 of the SRAM circuit.