A typical prior CMOS APS operates in a row-at-a-time (“rolling-shutter”) readout mode, which gives rise to exposure skew. In contrast, the proposed APS would operate in a sample-first/read-out mode, which gives rise to exposure noise. When an APS of prior design is operated in row-at-a-time readout, the contents of the memory array would be read out sequentially by use of a capacitive transimpedance amplifier (CTIA) at a maximum data rate of 10 MHz. This data rate is compatible with an update rate of almost 10 Hz, even in full-frame operation.

In the multiwindow readout mode, this APS could operate with ultralow noise. When an APS of prior design is operated in row-at-a-time readout, the main component of noise in each pixel is the reset noise at the sensing node. In the proposed APS, the reset levels for an array of 1,024 by 1,024 pixels containing high-performance photodiode-based APS circuitry. The reset noise at the sensing node. In the proposed APS, the reset levels for an array of 1,024 by 1,024 pixels containing high-performance photodiode-based APS circuitry. The pixel pitch would be 9 µm. The memory array would be large enough to hold differential signals acquired from all 8 windows during a frame period. Following the rapid sampling from all the windows, the contents of the memory array would be read out sequentially by use of a capacitive transimpedance amplifier (CTIA) at a maximum data rate of 10 MHz. This data rate is compatible with an update rate of almost 10 Hz, even in full-frame operation.

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