

National Aeronautics and Space Administration



# Electronics Health Management

Prognostics Center of Excellence, NASA ARC

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Prognostics Center of Excellence  
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NASA Ames Research Center

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# Agenda

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- Motivation and Background
- Accelerated Aging Systems for Prognostics
  - Thermal overstress system for Power Transistors
  - Electrical overstress system for Power Transistors
  - Electrical overstress system for Electrolytic Capacitors
- Device stress pre-conditioning by lightning injection
- Prognostics Model Development
- Prediction of Remaining Life
- Discussion and Closing Remarks

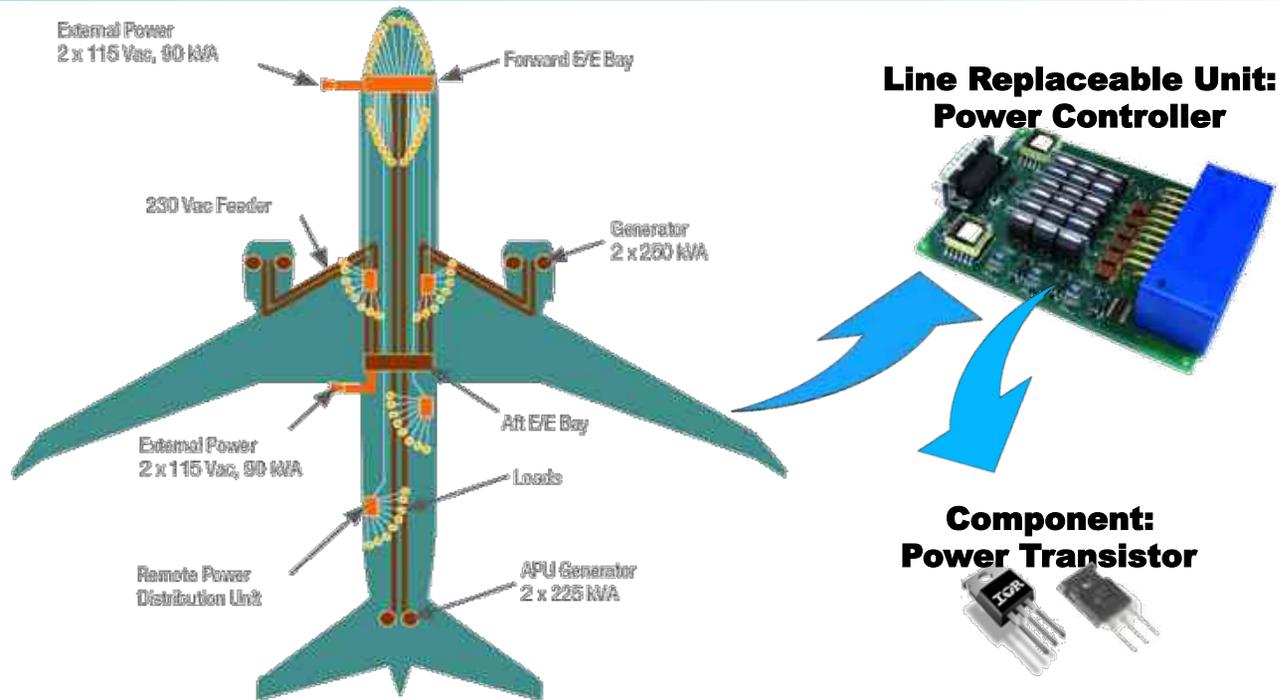
# Motivation (1/2)

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- Future aircraft systems will rely more on electronic components
- Electronic components have increasingly critical role in on-board, autonomous functions for
  - Vehicle controls, communications, navigation, radar systems
  - Power electronic devices such as power MOSFETs and IGBTs are frequently used in high-power switching circuits
  - The integrated navigation (INAV) module combines output of the GPS model and inertial measurement unit.
    - The filter capacitor of the power supply is the component which fails most often
      - faulty operation generates navigations errors in INAV
- Assumption of new functionality increases number of electronics faults with perhaps unanticipated fault modes
- We need understanding of behavior of deteriorated components to develop capability to anticipate failures/predict remaining RUL

# Motivation (2/2)



Images courtesy : Boeing

- Components under study:
  - **Power MOSFET:** IRF520Npbf, TO-220 package, 100V/9.27A
  - **IGBT:** IRG4BC30KD, TO-220 package, 600V/16A
  - **Electrolytic Capacitor:** 2200  $\mu$ F, 10V

# High level research efforts

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- **Prognostics models and algorithms**
  - Identification of precursors of failure for MOSFETs under different failure mechanism conditions
  - Identification of precursors of failure for different IGBT technologies (CALCE)
  - Modeling of degradation process MOSFETs
  - Development of prognostics algorithms
- **Prognostics for output capacitor in power supplies (Vanderbilt)**
  - Electrical overstress and thermal overstress
  - Development of prognostics algorithms
- **Accelerated Life Testing**
  - Thermal overstress aging of MOSFETs and IGBTs
  - Electrical overstress aging testbed MOSFETs
  - Electrical overstress aging testbed for Capacitors
- **Effects of lightning events of MOSFETS (LaRC)**
- Effects of ESD events of MOSFETS and IGBTs
- Effects of radiation on MOSFETS and IGBTs

# Research Approach

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Identification of failure modes and their relationship to their particular failure mechanisms



Identification of precursors of failure which play an essential role in the prediction of remaining life



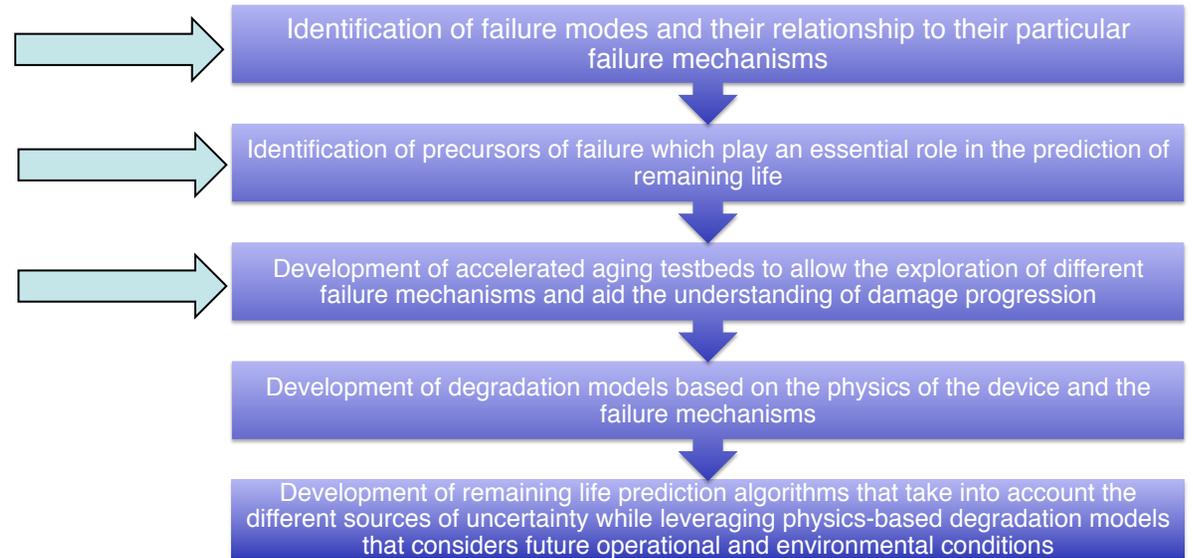
Development of accelerated aging testbeds that facilitate the exploration of different failure mechanisms and aid the understanding of damage progression



Development of degradation models based on the physics of the device and the failure mechanisms



Development of remaining life prediction algorithms that take into account the different sources of uncertainty while leveraging physics-based degradation models that considers future operational and environmental conditions



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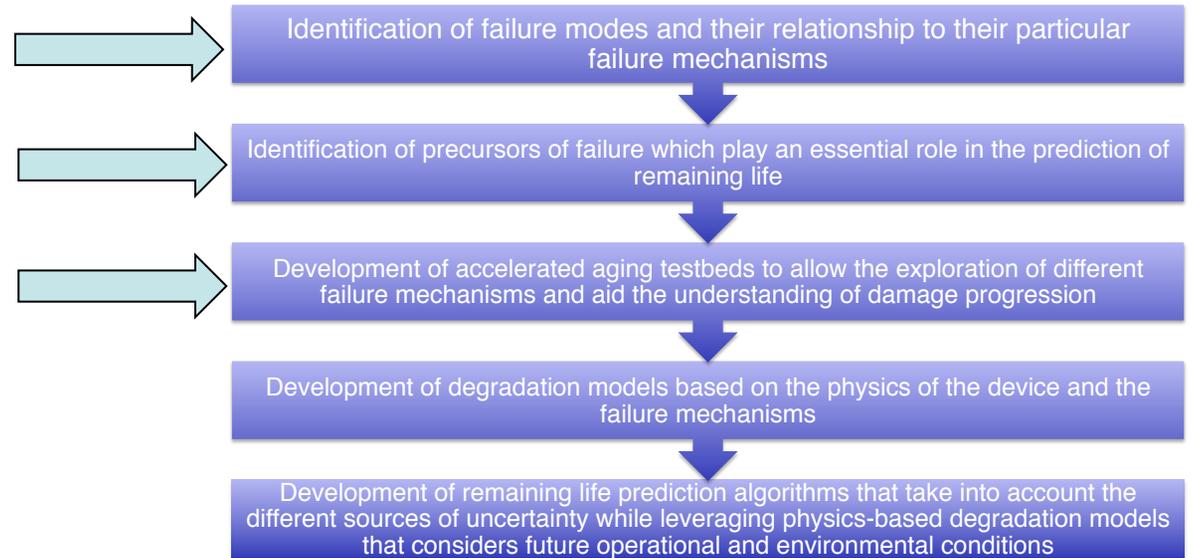
# ACCELERATED AGING SYSTEMS FOR PROGNOSTICS

# Accelerated Aging

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- Traditionally used to assess the reliability of products with expected lifetimes in the order of thousands of hours
  - in a considerably shorter amount of time
- Provides opportunities for the development and validation of prognostic algorithms
- Such experiments are invaluable since run-to-failure data for prognostics is rarely or never available
- Unlike in the reliability studies, prognostics is concerned not only with time to failure of devices but with the degradation process leading to an irreversible failure
  - This requires in-situ measurements of key output variables and observable parameters in the accelerated aging process with the associated time information
- Thermal, electrical and mechanical overstresses are commonly used for accelerated aging tests of electronics



Accelerated Aging Systems for Prognostics

# THERMAL OVERSTRESS AGING OF POWER TRANSISTORS

# Accelerated Aging Methodology

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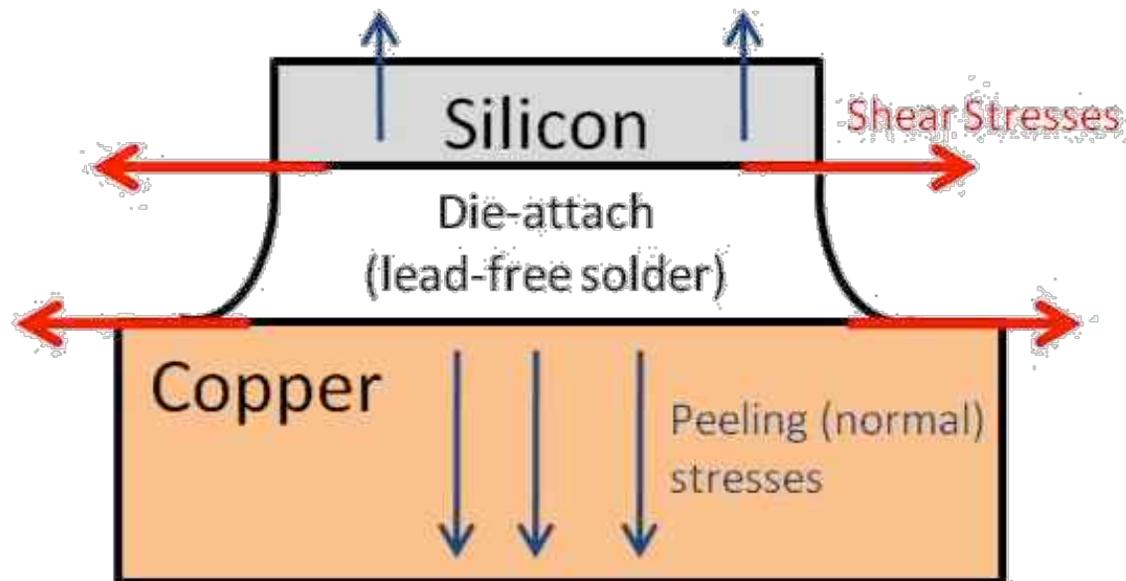


- The main strategy is the application of thermal overstress in the form of thermal cycles
- This is achieved by
  - Power cycling the devices without use of any external heat sink
  - Causing self heating during the power switching operation
- The goal is to induce package related failures like die-attach damage
- Failure is defined as
  - Latch up
  - Loss of gate control (failure to turn ON)
  - Thermal runaway

# Thermal-Mechanical Stresses



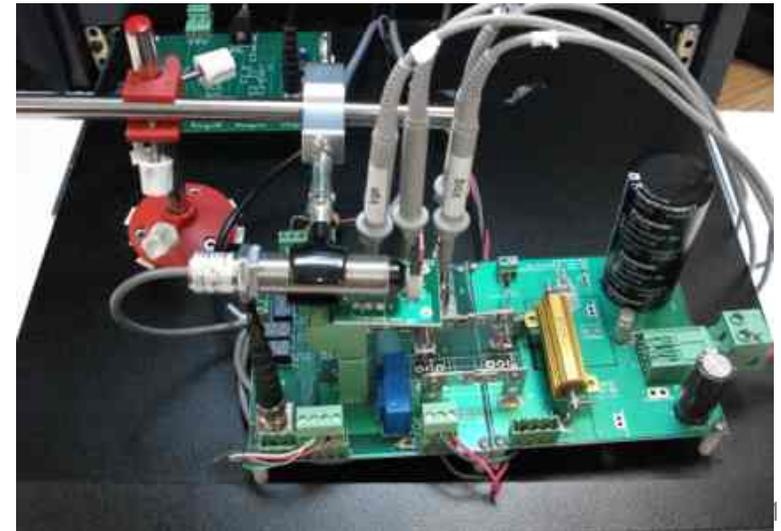
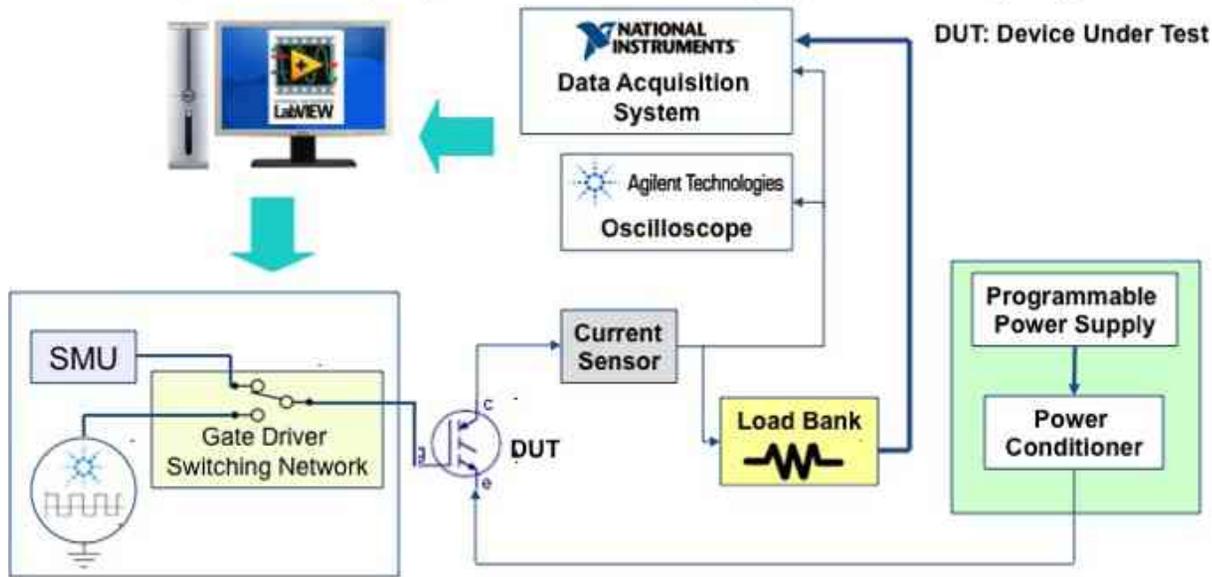
- The device structure can be regarded as a bi-metal assembly
  - Copper (internal heat sink) is the substrate
  - Silicon die is attached to the substrate with solder (die-attach)
- Thermally mismatched assembly due to difference in coefficient of thermal expansion (ppm/°C).
  - Copper: 16-18,
  - Silicon: 2.6-3.3, and
  - Lead-free Solder: 20-22.9



# System Description



Experiment setup high-level schematic for aging via thermal cycling

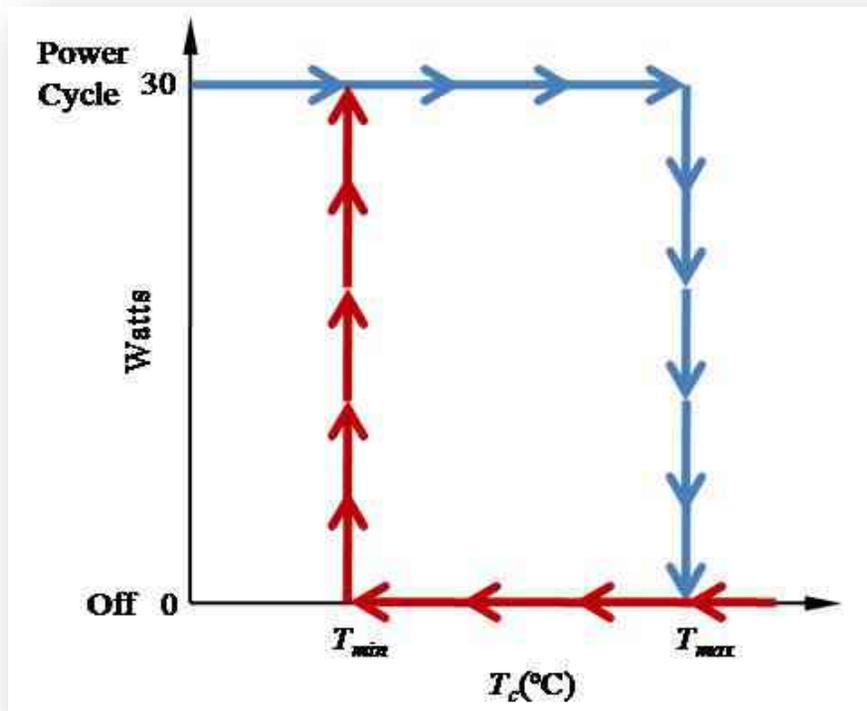


# Aging Experiments

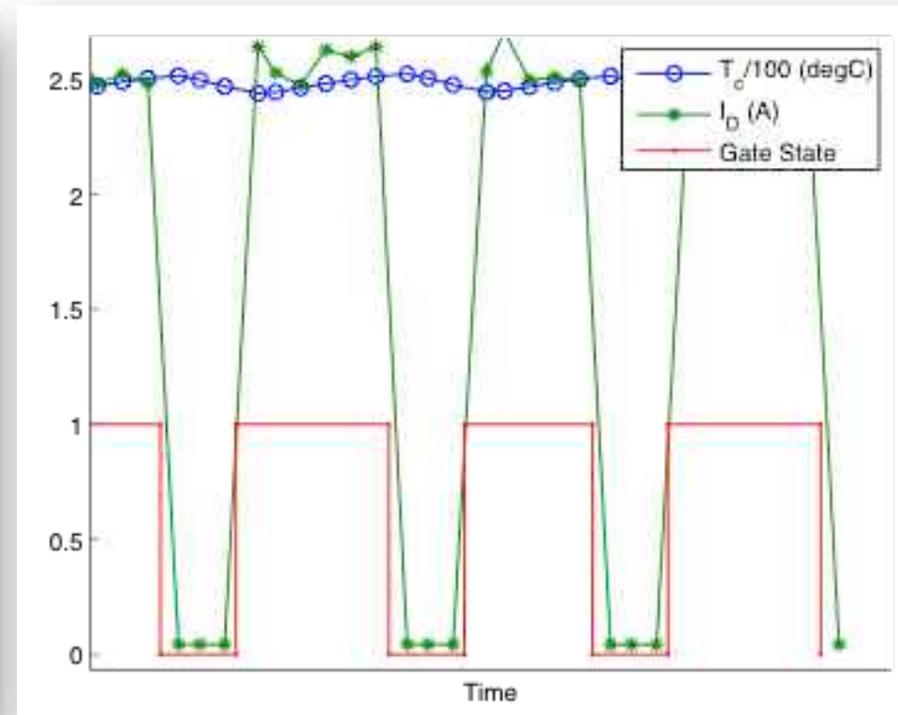


- Hysteresis control is used to provide thermal cycles needed for acceleration

Case temperature control law



Accelerated aging regime



# Die-Attach Damage Assessment (1/3)

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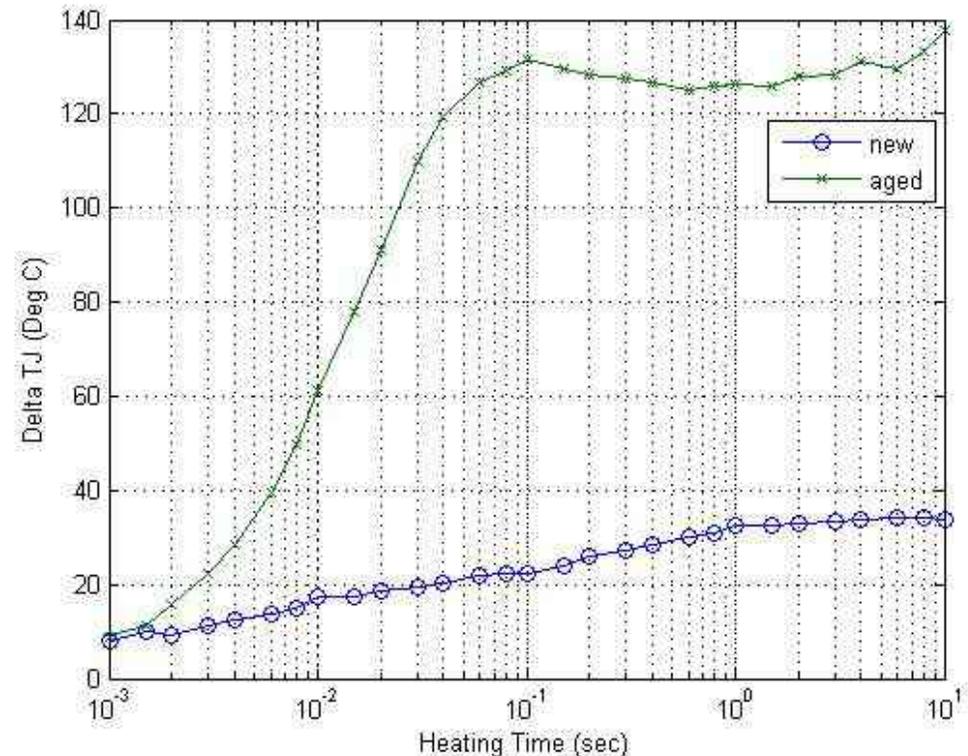


- Collecting the ground truth data
  - Heat transfer performance due to thermal conduction decreases with die-attach damage
    - Voids, cracks, other mechanical damage
  - MIL-750 standard method 3161 provides a methodology for thermal impedance measurements for power MOSFET
    - Delta source-drain voltage method
    - Body diode is used to measure junction temperature
  - Heating curves can provide an assessment of the thermal characteristics of the die-attach

# Die-Attach Damage Assessment (2/3)



- Results for Device #11
- 1 sec. heating time
- Same power applied to both tests (same heating profile)
- Steep slope starting at  $\sim 10\text{ms}$  is indicative of the die attach damage
- This method can be included as a BIT in order to periodically assess die-attach damage



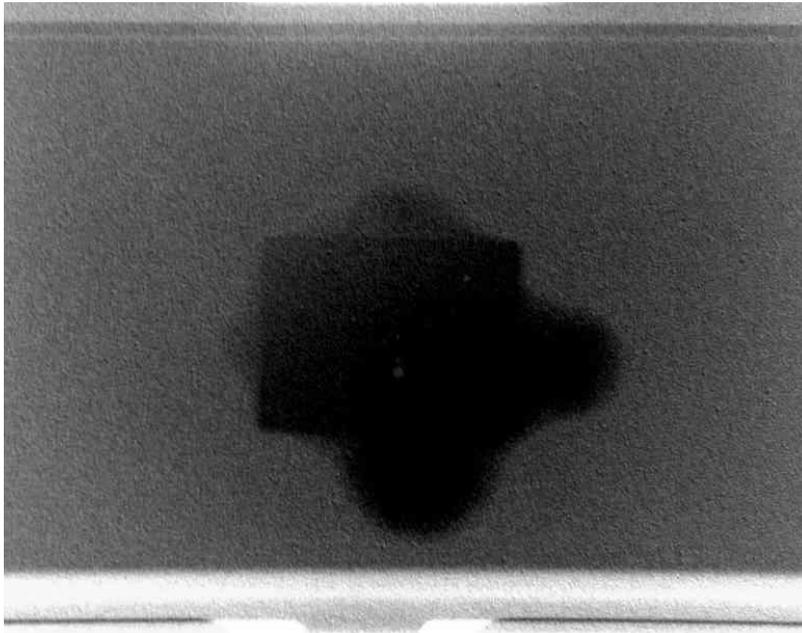
**Aged device under thermal cycling heats up considerably faster than a pristine device**

# Die-Attach Damage Assessment (2/3)

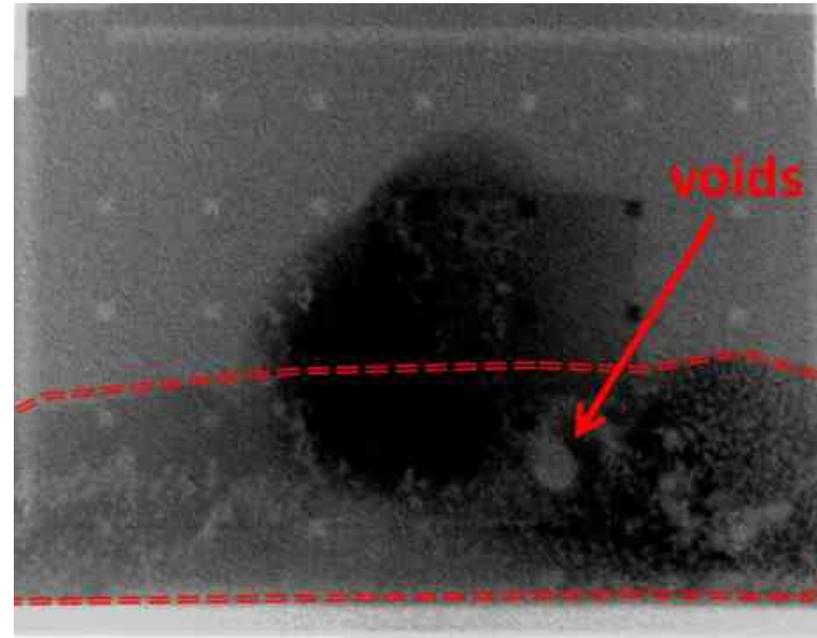


- Damage of the die-attach interface can also be observed visually using failure analysis techniques like X-Ray (below) and Scanning Acoustic Microscopy

**Pristine device**



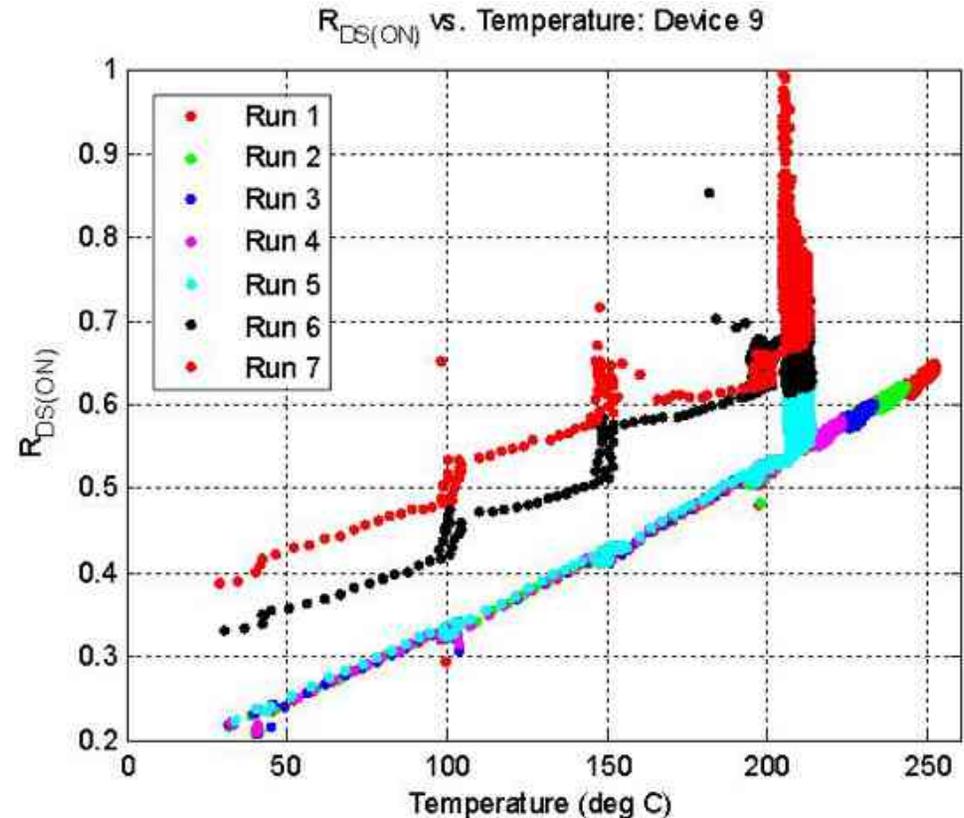
**Aged device (#8)**

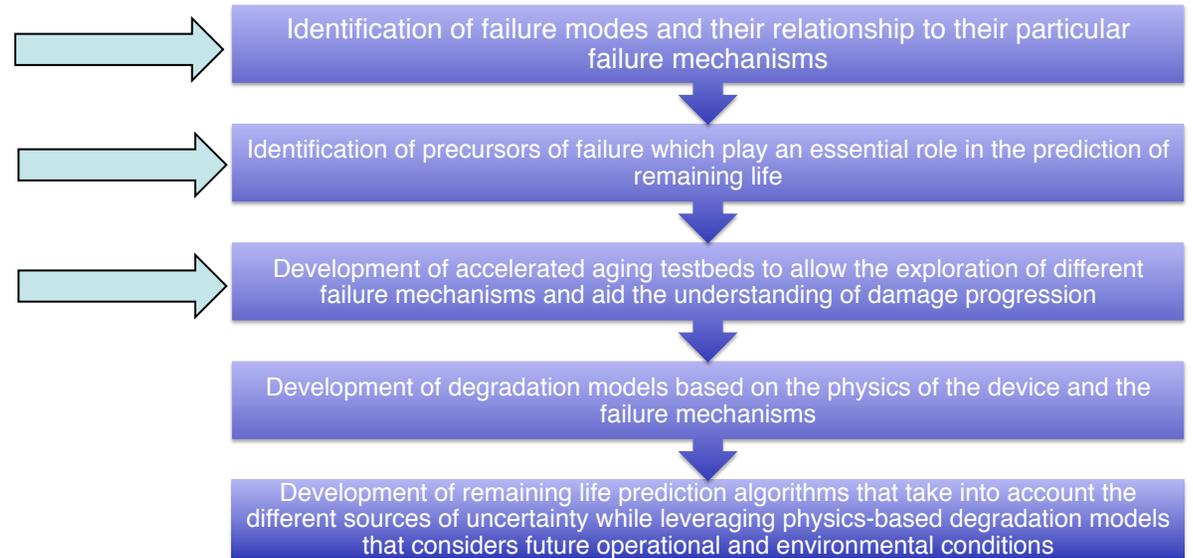


# Precursor of Failure



- As case temperature increases, ON-resistance increases
- This relationship shifts as the degradation of the device increases
- For a degraded state, ON-resistance will be higher at any given case temperature
- This is consistent with the die-attach damage since it results on increased junction temperature operation
- This plot can be used directly for fault detection and diagnostics of the die-attach failure mechanism





Accelerated Aging Systems for Prognostics

# **ELECTRICAL OVERSTRESS AGING OF POWER TRANSISTORS**

# Accelerate aging strategy (1/3)

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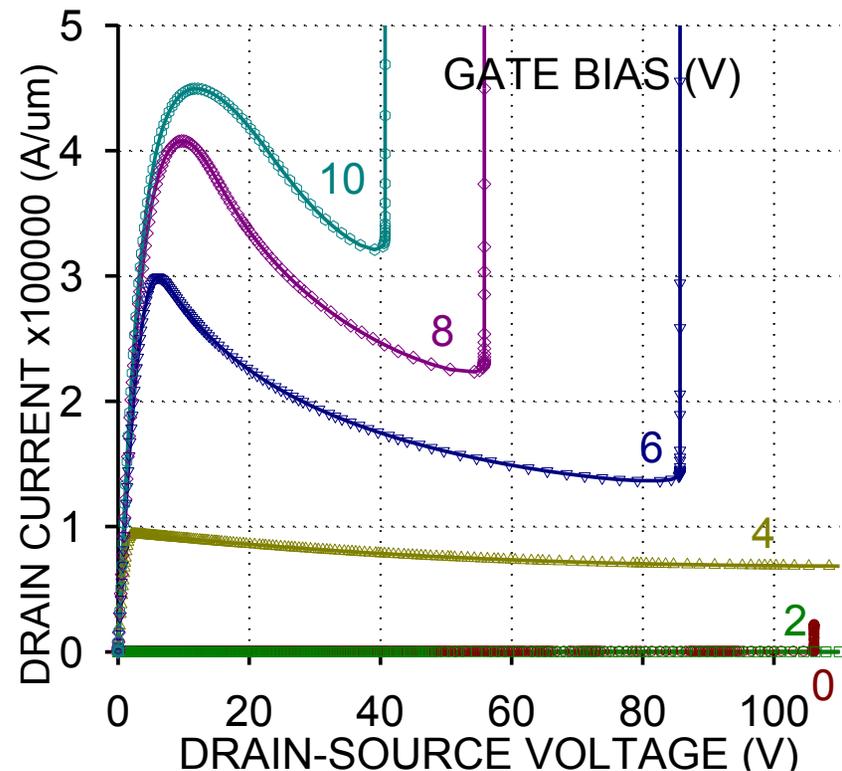
- The main strategy is the
  - application of electrical overstress
  - fixed junction temperature in order to avoid thermal cycles
  - avoid package related failures
- Accelerated test conditions are achieved by electrical operation regime of the devices at temperatures within the range below maximum ratings and above the room temperatures.

# Accelerate aging strategy (2/2)



- The highest acceleration factor for aging can be achieved in the proximity of the SOA boundary
- Instability points represent the critical voltages and currents limiting the SOA
- An electrical regime close to the SOA boundary serves as the accelerator factor (stressor) and it is expected to reduce the life of the device
- The safe operation area boundary shifts closer to the origin as the temperature increases

Simulated I-V characteristics and instability boundary at 300°K for power MOSFET.



# Aging system description (1/3)

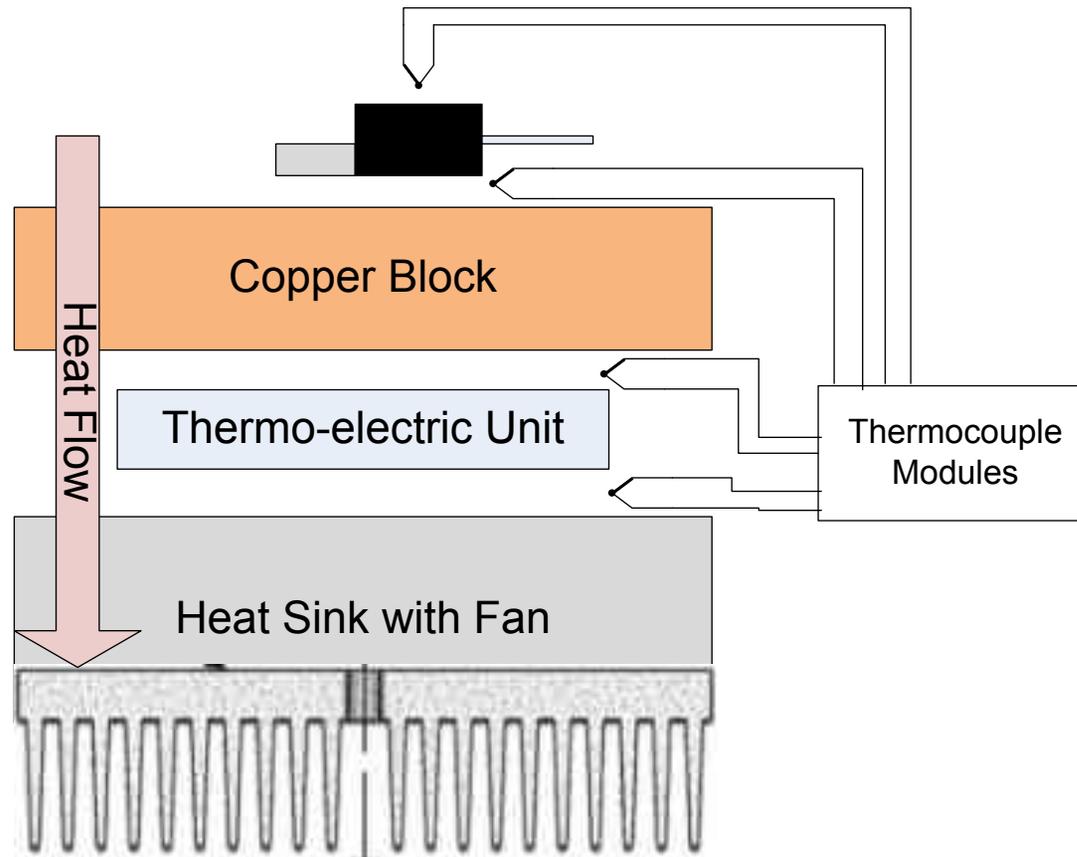
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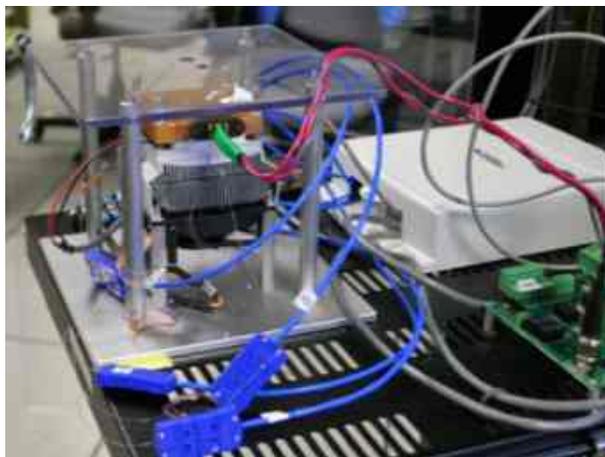
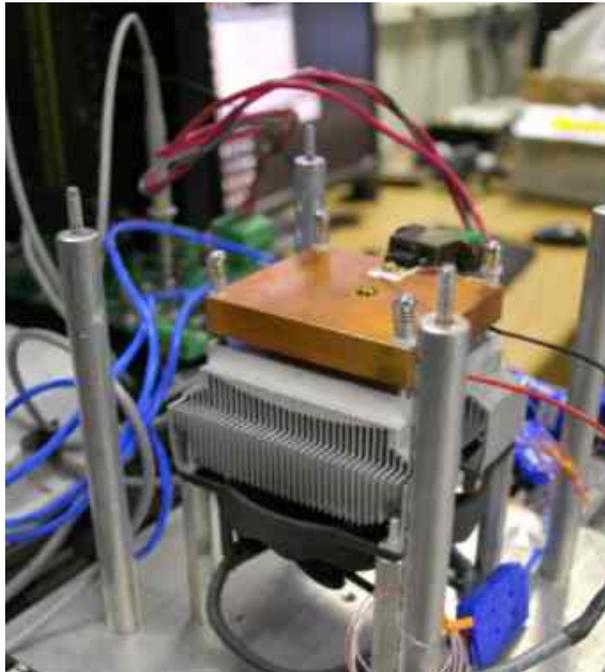
- Three main components in terms of hardware
  - Electrical operation unit of the device
    - custom made printed circuit boards for the instrumentation circuitry and gate drivers
    - commercially available power supplies and function generator to control the operation of the DUT
  - An in-situ measurement unit of key electrical and thermal parameters
    - commercially available measurement and data acquisition for slow and high speed measurements
  - Thermal block section for monitoring and control of the temperature



## Thermal block for measurement and control of device temperature



# Aging system description (3/3)



# Experiment on power MOSFET (1/2)

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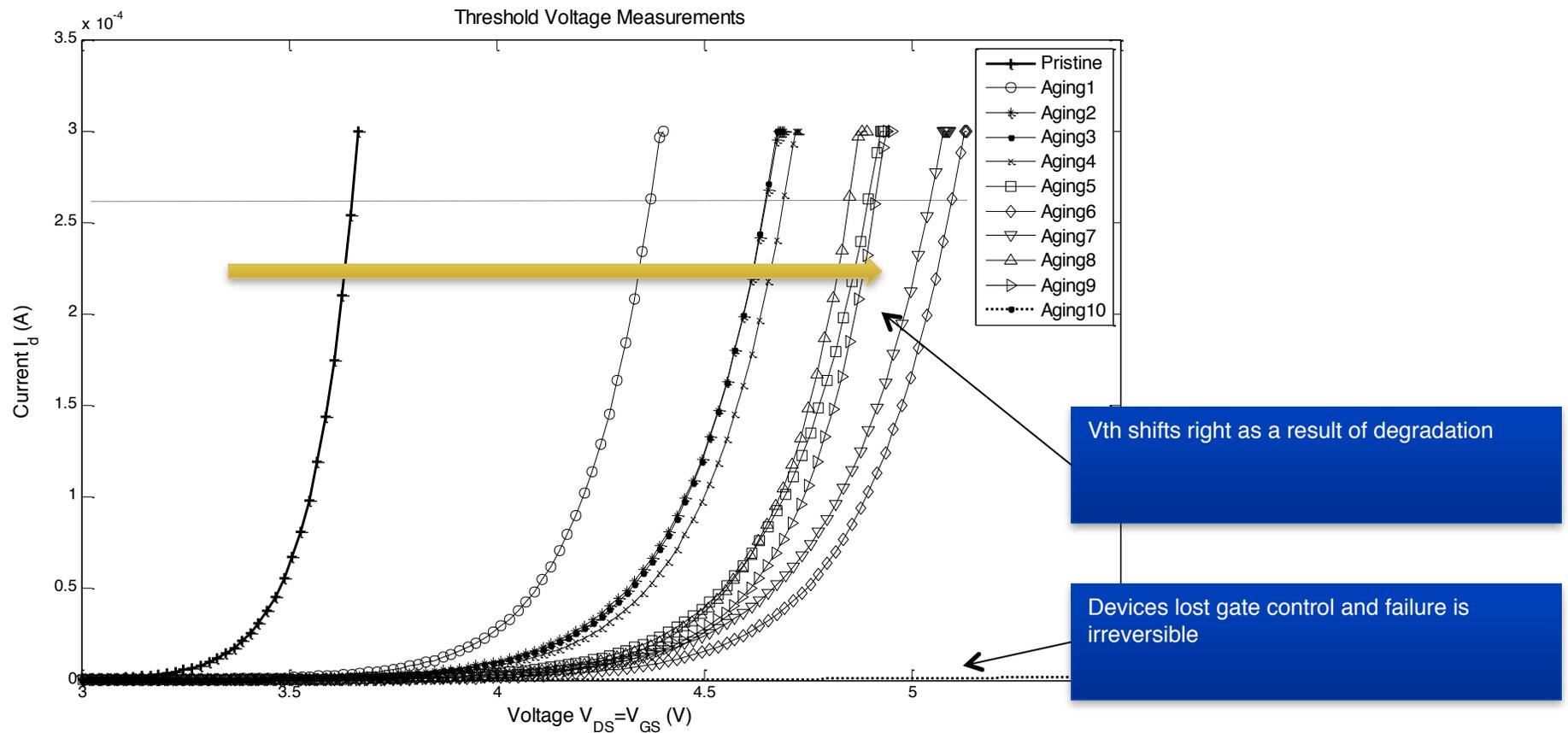


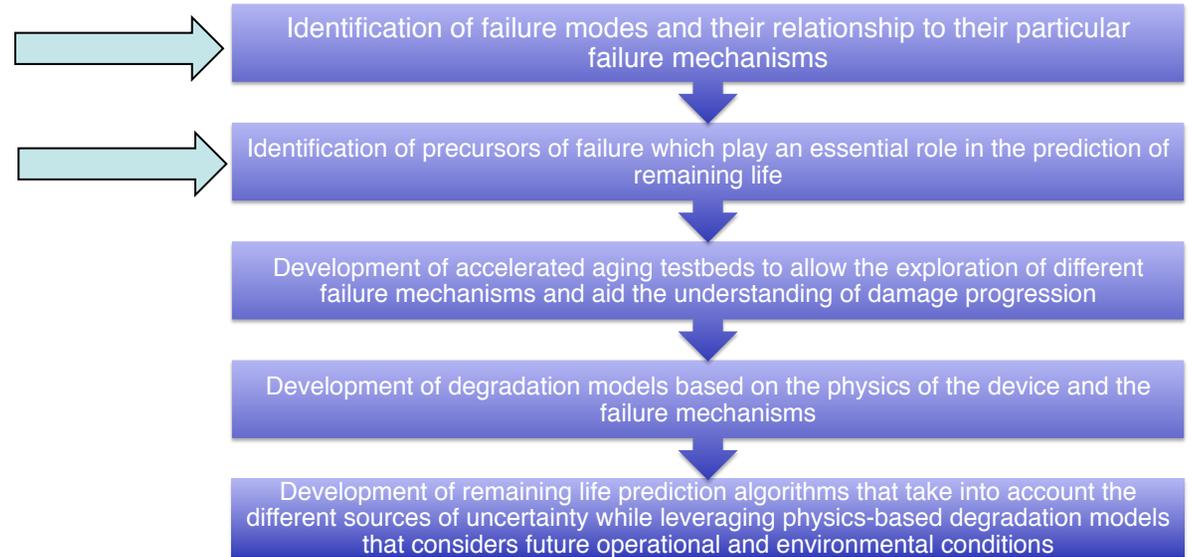
- IRF520Npbf power MOSFET
  - TO220 package, 100V/9A.
- Electrical overstress used as acceleration factor. High potential at the gate
  - $V_{gs}=50V$ ,  $V_{gs}$  rating is 20V max.
  - $V_{ds}=2.4V$  with a 0.2 ohm load.
- Temperatures kept below maximum rating  $T_{jmax}=175^{\circ}C$
- Objective is to induce failure mechanism on the gate structure

# Experiment on power MOSFET (2/2)



- Degradation process as observed on threshold voltage ( $V_{th}$ )





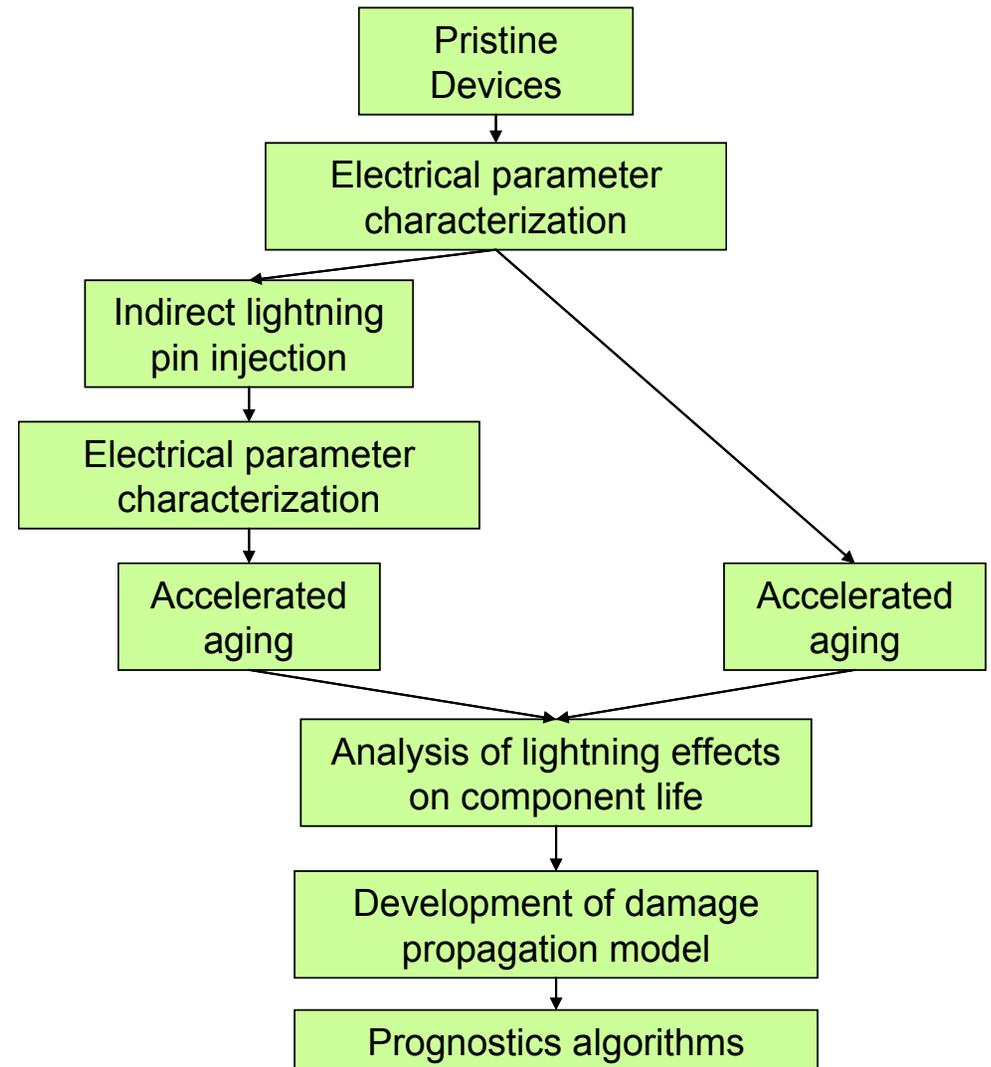
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# DEVICE STRESS PRECONDITIONING BY LIGHTNING INJECTION

# Hypothesis



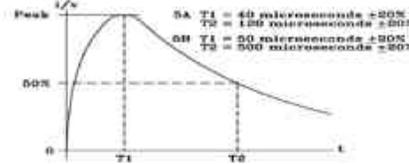
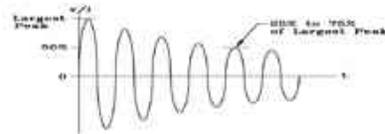
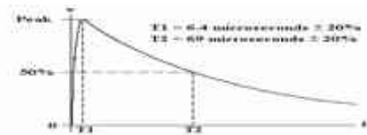
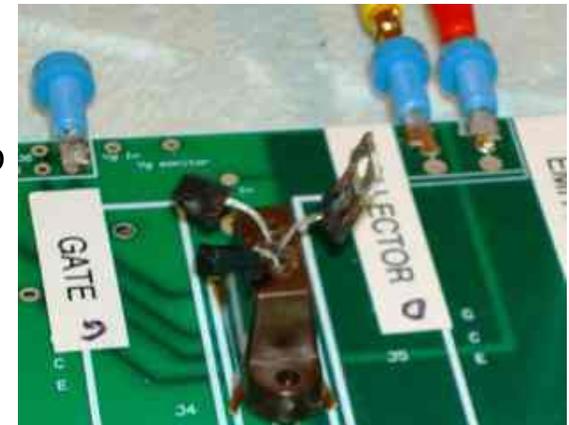
- Lightning events on electronics components could result in partial damage or failure
- Damage accumulates as a result of repeated events or other extreme operation and/or environmental conditions
- Damage incurred is not large enough to render the device inoperable, but its performance and robustness is diminished
- The accumulated damage could result in a decrease in the remaining lifetime
- There are leading indicators of failure that could be used to develop a prognostics solution



# Approach



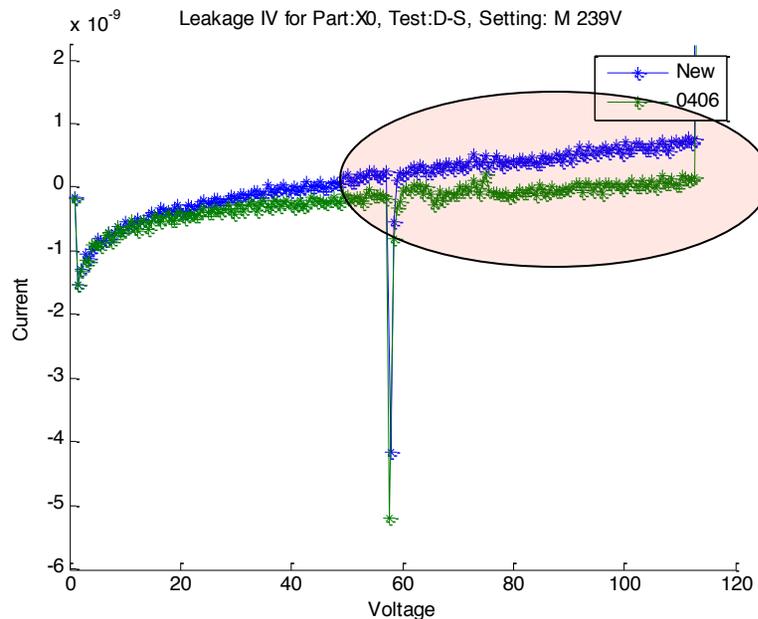
- NASA Ames and LaRC IVHM researchers tested a set of 400 identical MOSFETs, by pin-injecting standard lightning waveforms to induce fault modes and to degrade performance.
- Pre-Tests Identified damage levels for each pin configuration. (i.e., Gate-Source, Gate-Drain, Drain-Source). “High” Test Level defined as highest possible 20-strokes test-level without damage. “Medium” = 0.9 x “High”. “Low” = 0.8 x “High”.
- Tested 5 samples of each device, at 5, 10, 20 strokes, at each Level.
- Lightning waveform voltages up to 1700V, and currents up to 1460A, were applied to various MOSFET pin configurations. Safety Hazards and Precautions were identified by the research team before testing, and all test personnel participated in a safety briefing.
- MOSFETs will be evaluated using the NASA Ames Aging and Characterization Platform for semiconductor components, for the purpose of developing predictive algorithms as part of IVHM prognostic health management program goals.
- Most Tests focused on Lightning Waveform #4. Some testing also performed using Waveforms #3, 5A and 5B



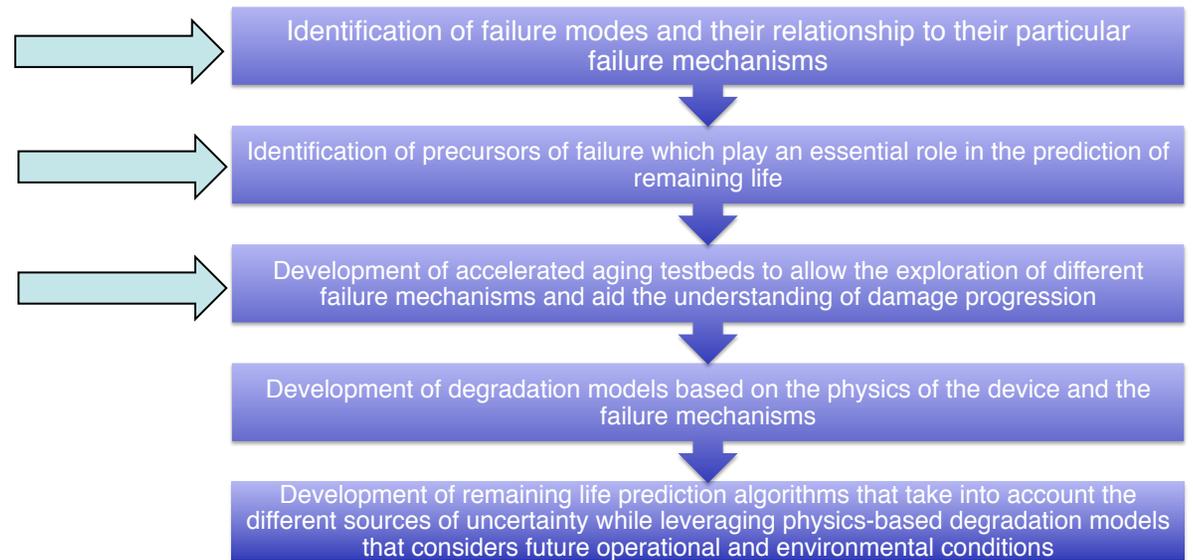
# Results



- Current work focused on identification of key electrical parameters that show detection of damage and serve as failure precursor candidates for prognostics
- Leakage current parameters show a change due to injection of waveform 4 from the drain to the source of the MOSFET after 5 strokes.



Shift in electrical parameters indicative of damage due to repeated application of lightning waveform



Accelerated Aging Systems for Prognostics

# **ELECTRICAL OVERSTRESS AGING OF ELECTROLYTIC CAPACITORS**

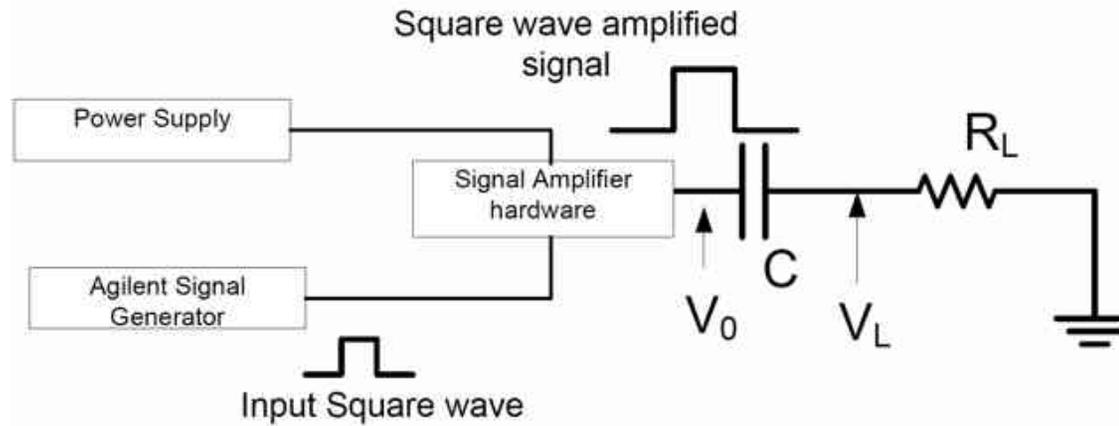
# Accelerated aging system

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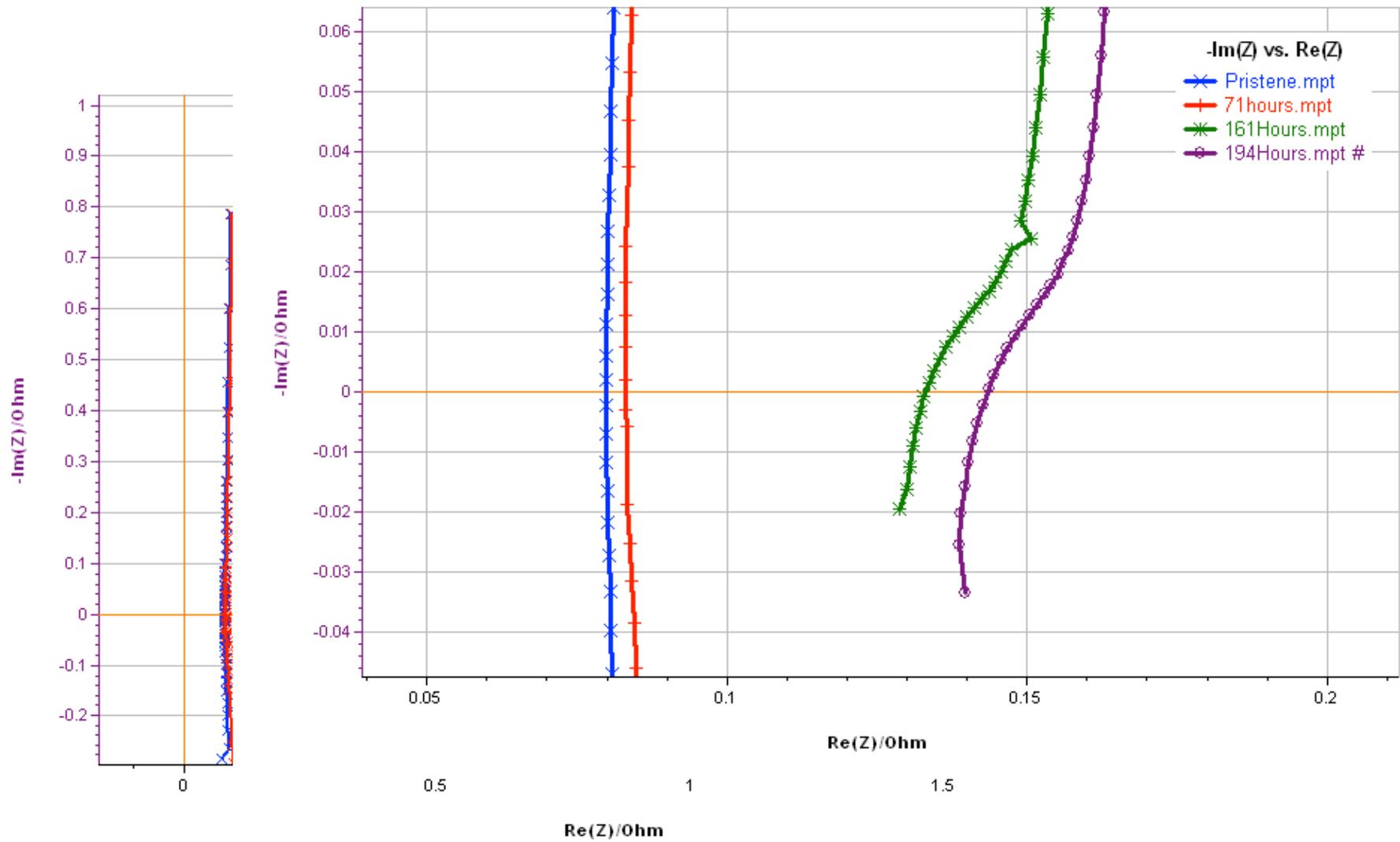


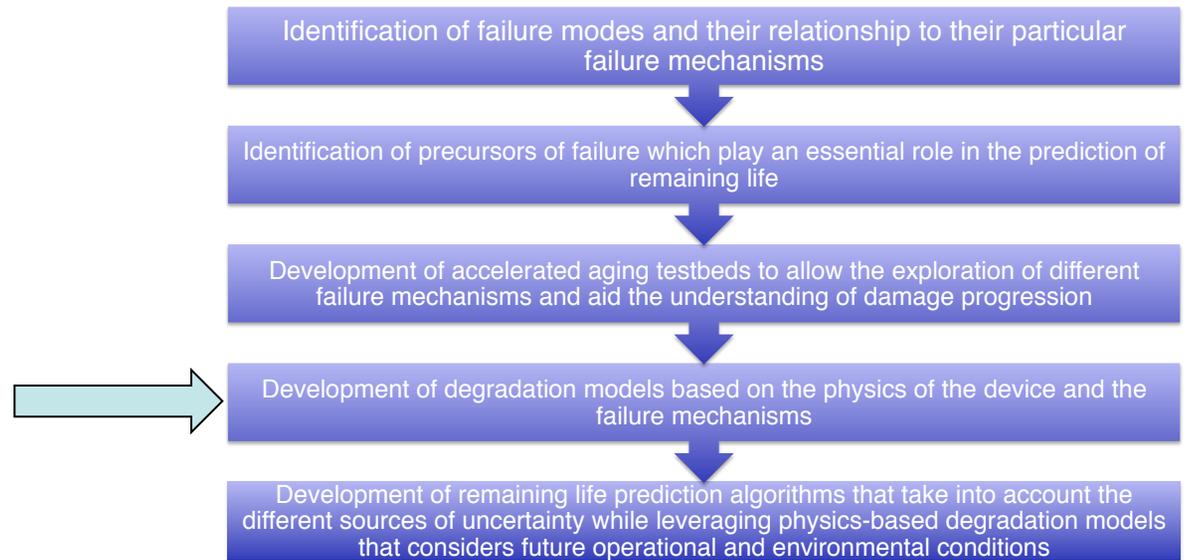
- Allows for the understanding of the effects of failure mechanisms, and the identification of leading indicators of failure essential for the development of physics-based degradation models and RUL prediction
- Electrolytic capacitor 2200uF, 10V and 1A
- Electrical overstress >200 hr
  - Square signal at 200 mHz with 12V amplitude and 100 ohm load

# Electrical Overstress Aging System



# Degradation observed on EIS measurements





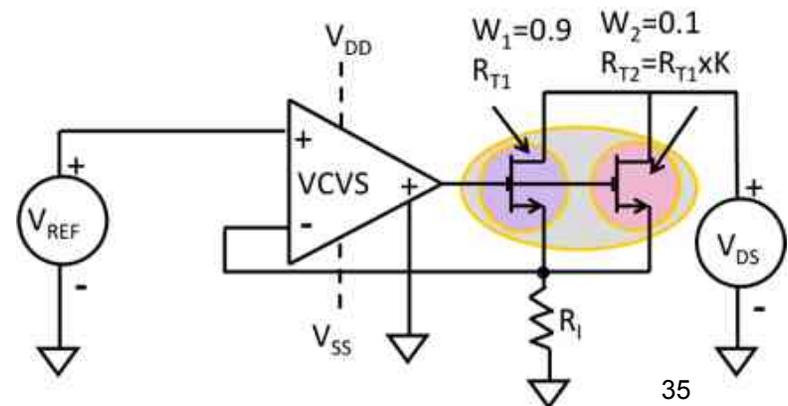
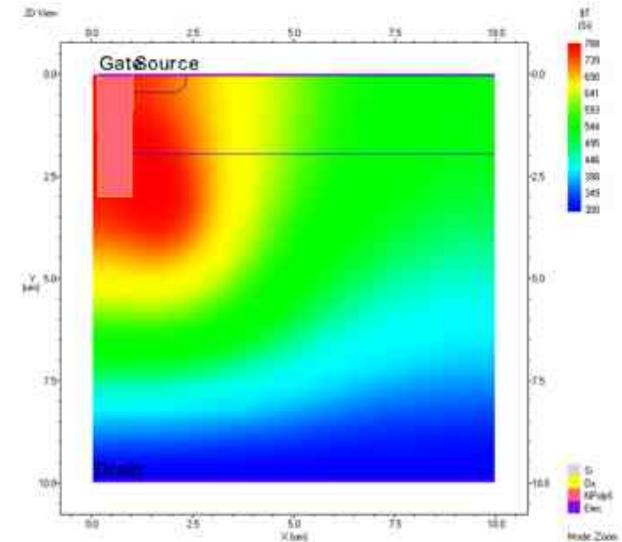
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# PROGNOSTICS MODEL DEVELOPMENT

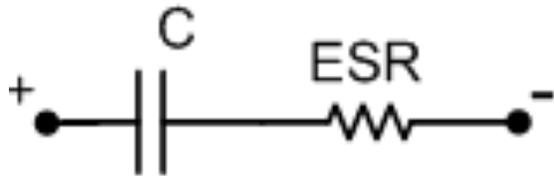
# Modeling for Power MOSFET under electrical overstress



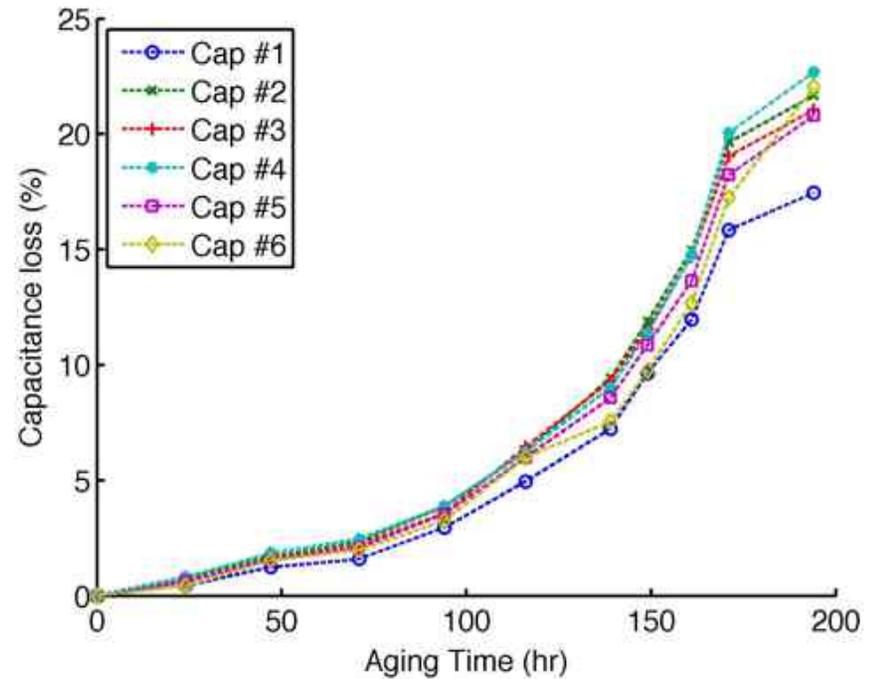
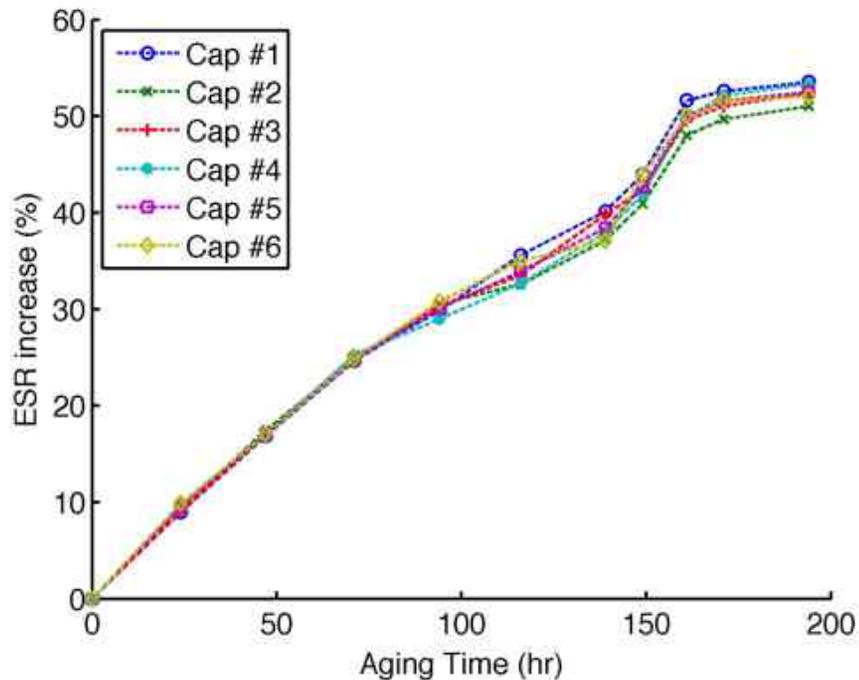
- Two-transistor model is shown to be a good candidate for a degradation model for model-based prognostics.
- The model parameters  $K$ , and  $W1$  could be varied as the device degrades as a function of usage time, loading and environmental conditions.
- Parameter  $W1$  defines the area of the healthy transistors.
  - The lower this area, the larger the degradation in the two-transistor model.
- In addition, parameter  $K$  serves as a scaling factor for the thermal resistance of the degraded transistors
  - The larger this factor, the larger the degradation in the model.



# Degradation modeling for Capacitor (1/2)



C and Equivalent Series Resistance (ESR) are estimated from EIS measurements

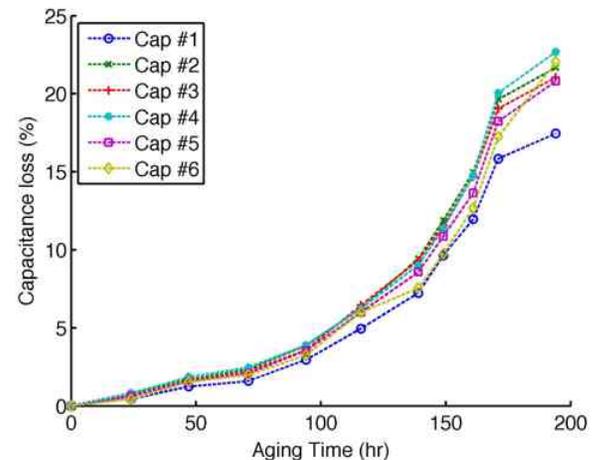


# Degradation modeling for Capacitor (2/2)



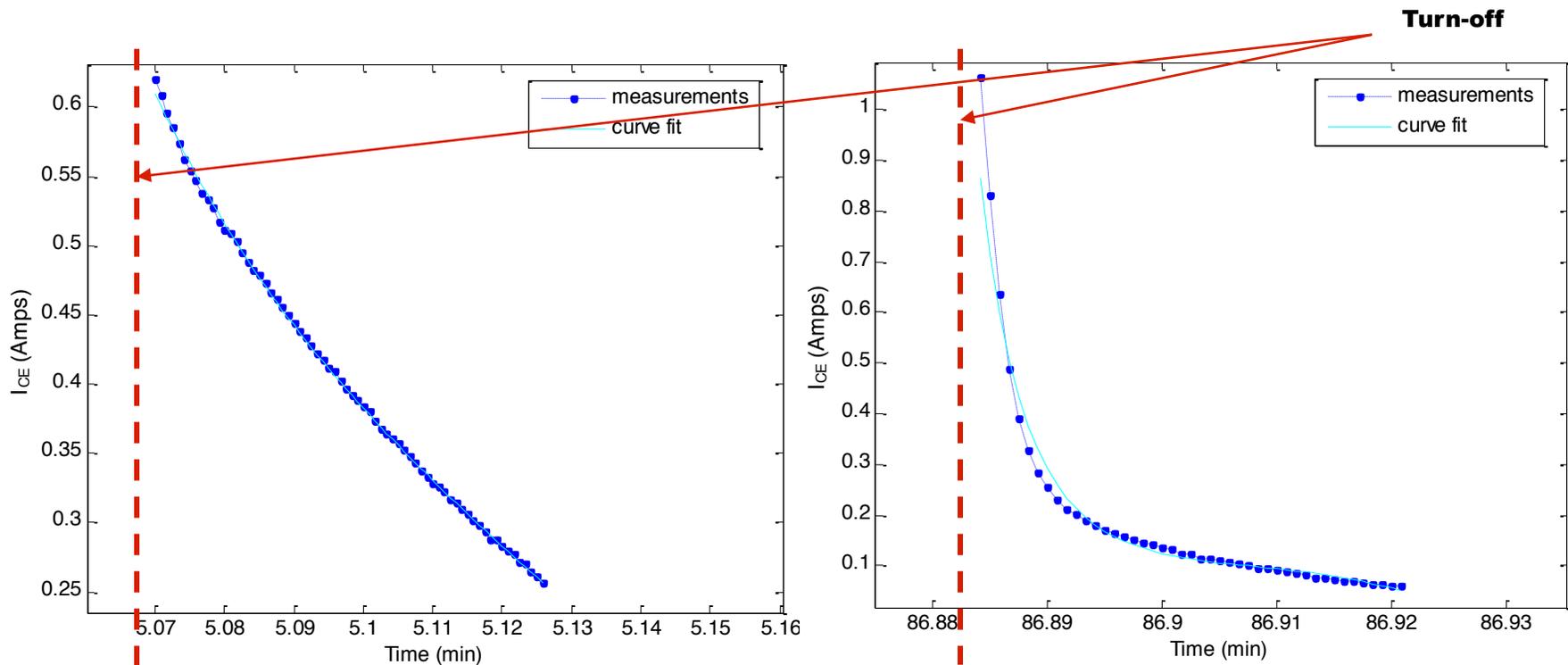
- Empirical model based on observed degradation from capacitance parameter
- Using accelerated aging data to estimate degradation model parameters
- Assumed exponential model based on capacitance loss
- Parameter estimation with least-squared regression

$$C_k = e^{\alpha t_k} + \beta$$





- Failure precursors observed in collector current  $I_{CE}$ 
  - The tail current falls more sharply after aging



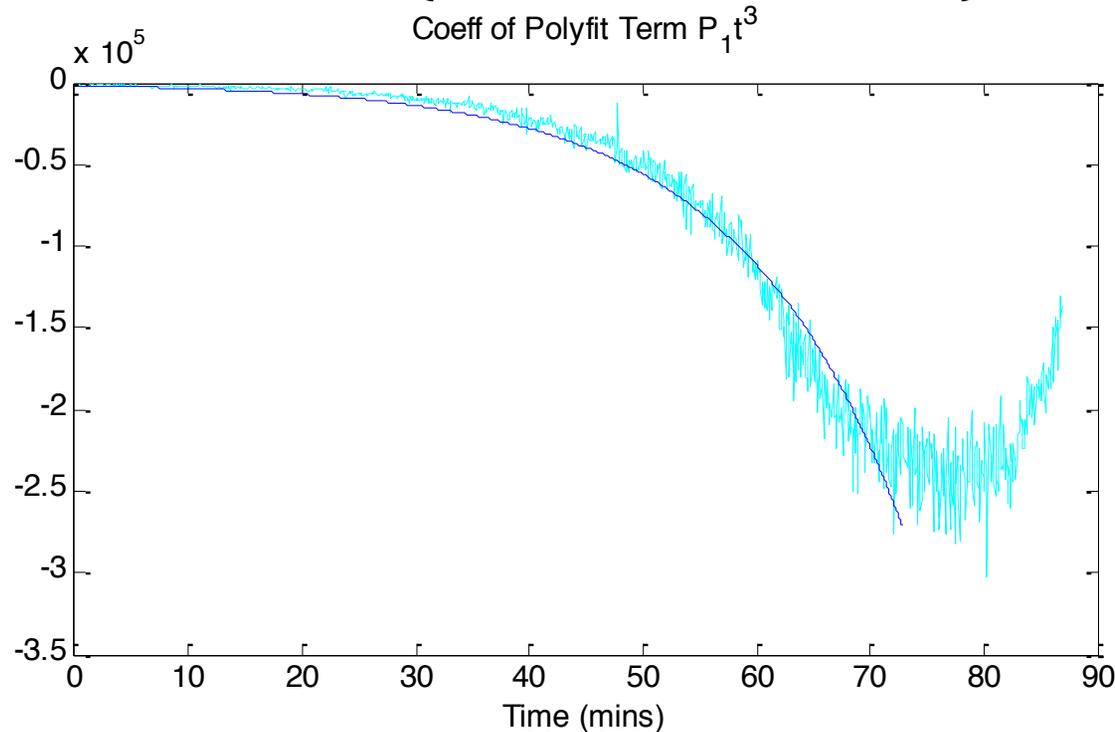
**Change in IGBT Off-state Current Decay with Aging**

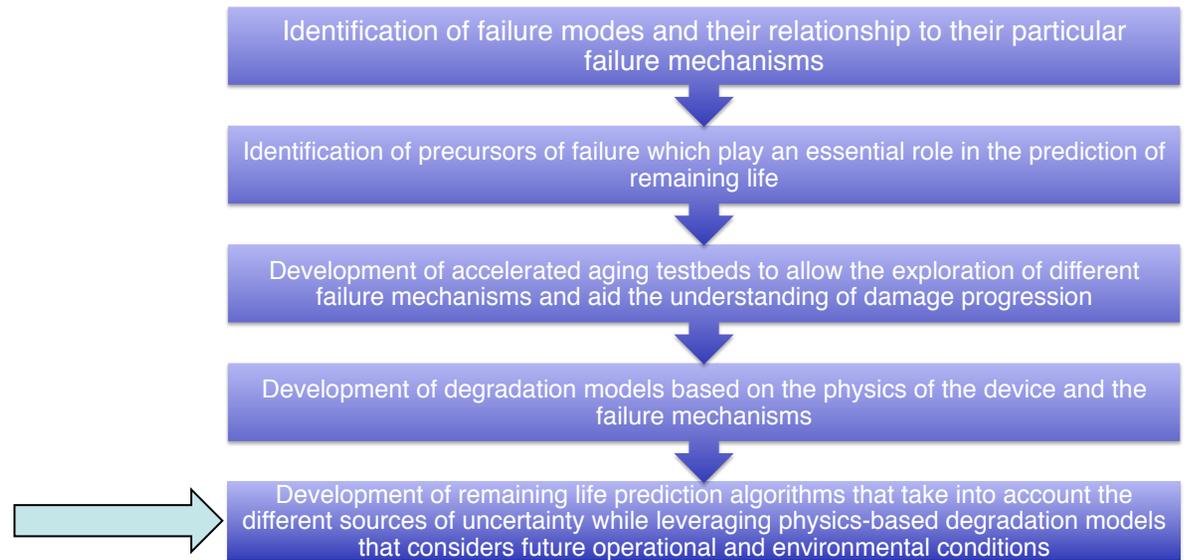
# Degradation modeling of IGBT under thermal stress (1/2)



- Empirical model based on degradation data
- Parameters need to be estimated

$$I_{CE}(t) = \exp\{P_1 t^3 + P_2 t^2 + P_3 t + P_4\}$$





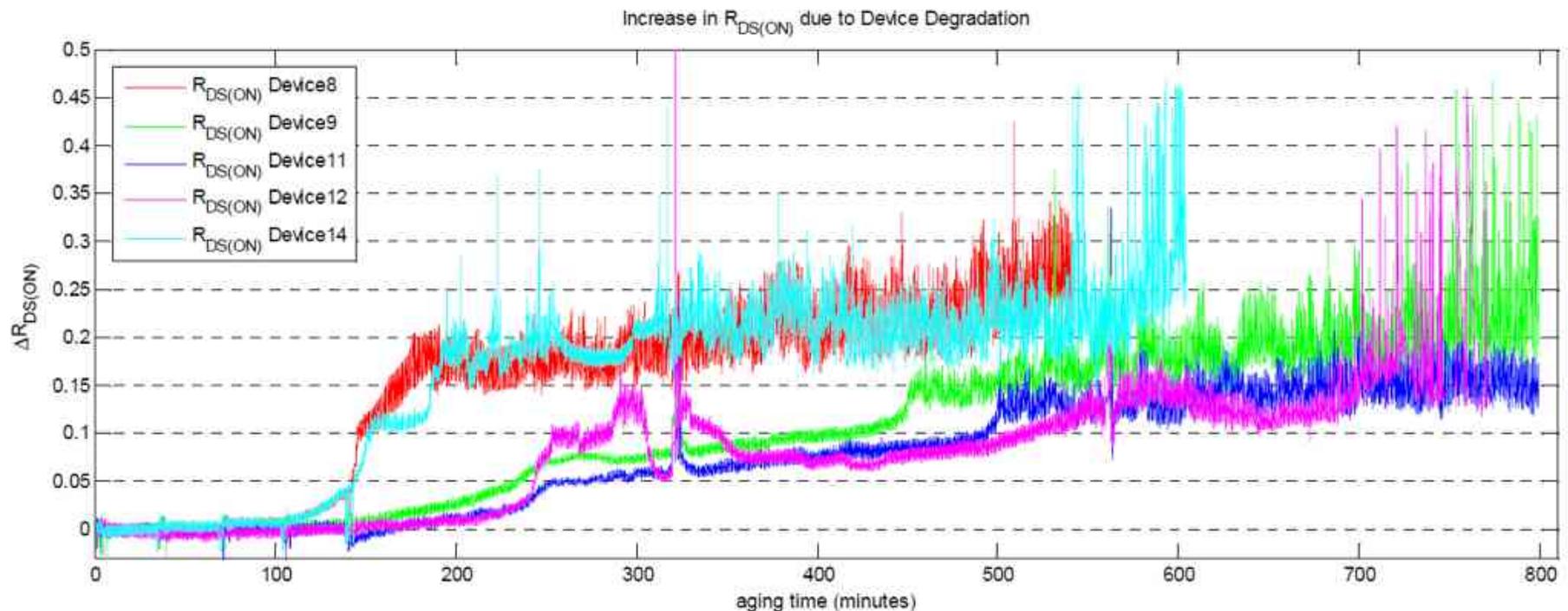
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# PREDICTION OF REMAINING LIFE

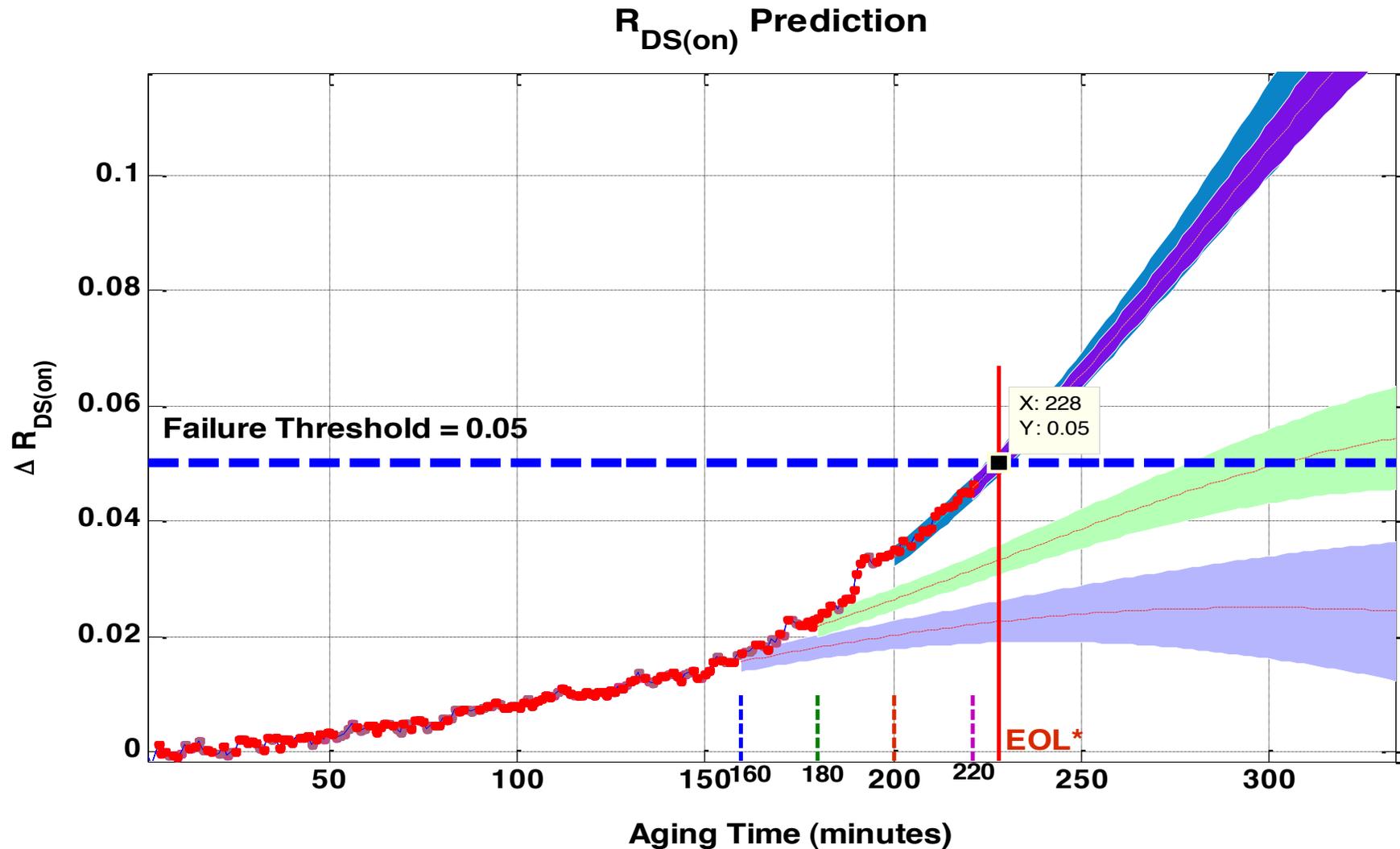
# Data-driven prognostics for Power MOSFETs under thermal stress



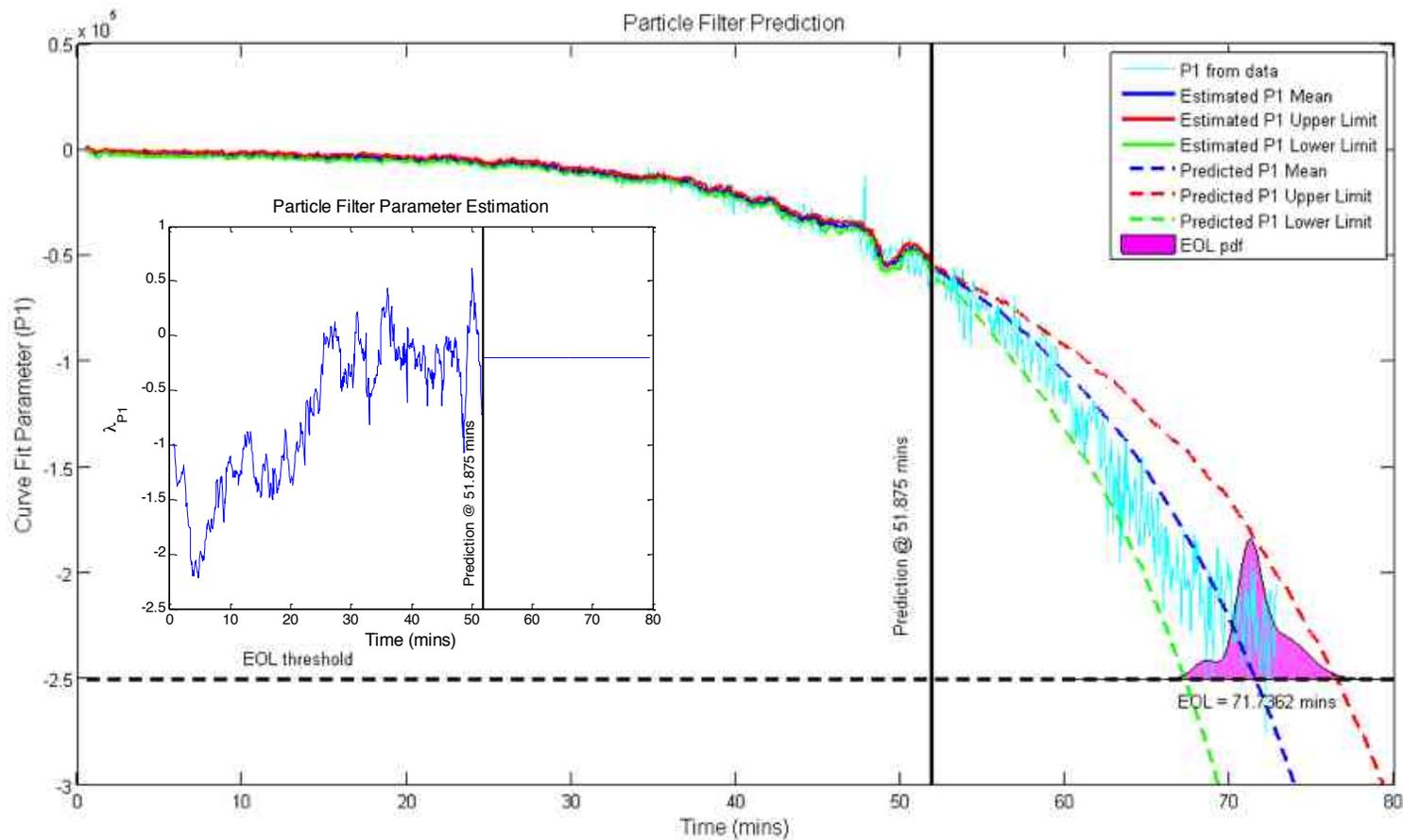
- Change in ON-resistance as a function of aging time
- Normalized based on pristine condition values
- $RDSON = RDSON_{nominal} + RDSON_{temperature} + RDSON_{degradation}$
- Gaussian Process Regression Algorithm used to predict RUL



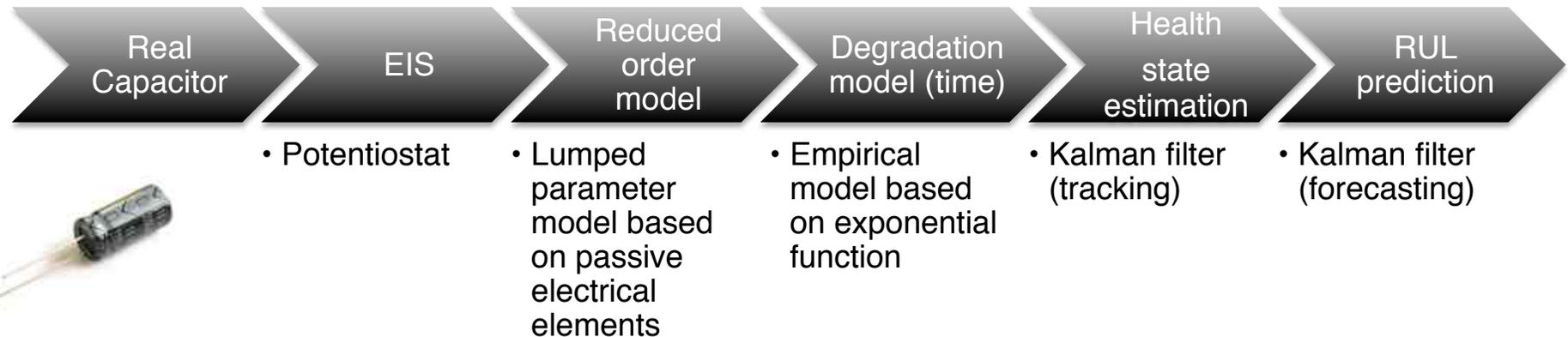
# Data-driven prognostics for Power MOSFETs under thermal stress



# Prognostics with Particle Filter for IGBT under thermal stress

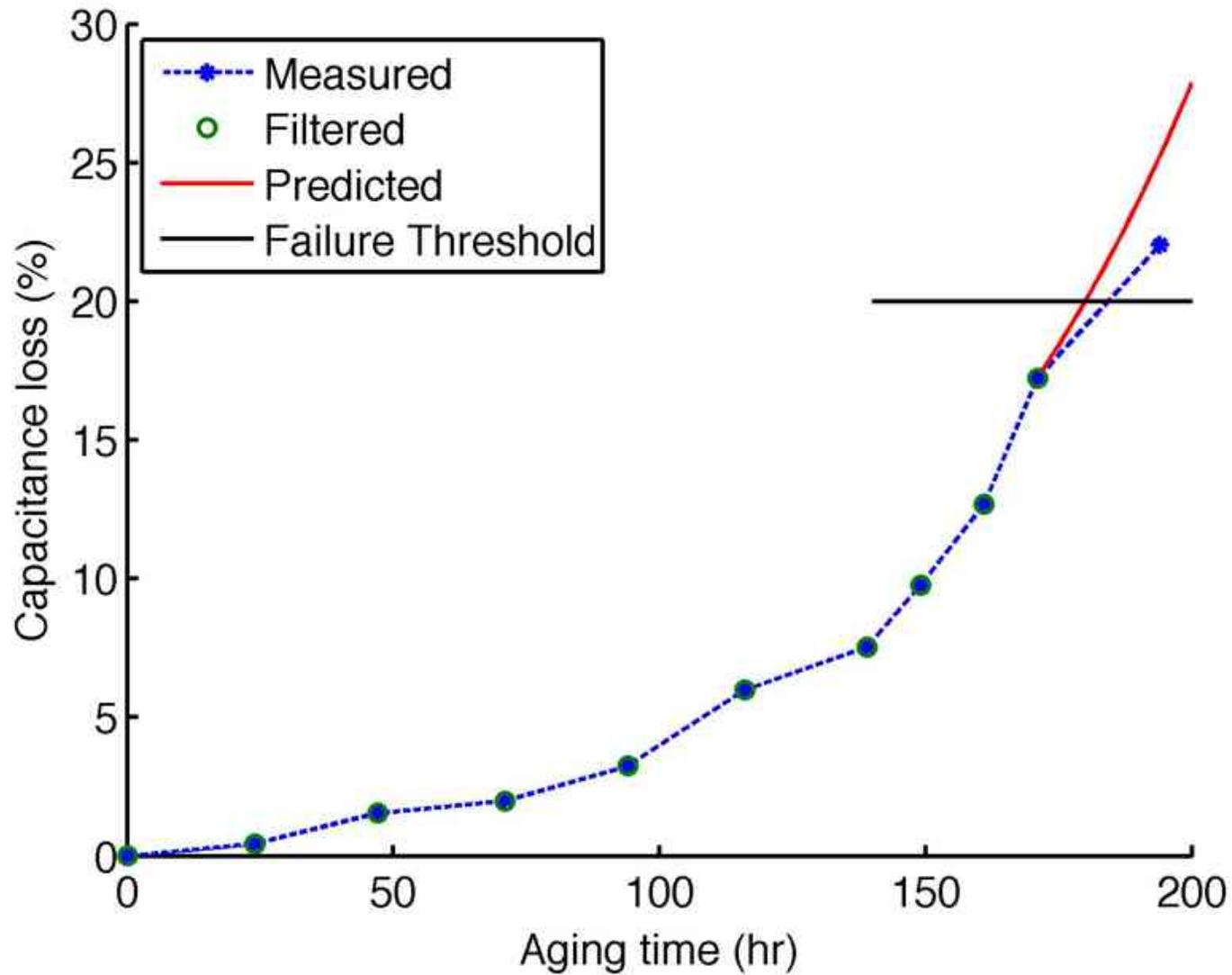


# Kalman Filter based prognostics for Capacitor under electrical overstress



- Implementation of prognostics algorithm with Kalman filter
- Capacitance loss considered as state variable
- EIS measurements and lumped parameter model used to obtain measured capacitance loss values
- Empirical degradation model used to generate the state transition equation
- Use Cap #6 to test predictions
- Failure threshold of 20% drop on capacitance based on MIL-C-62F

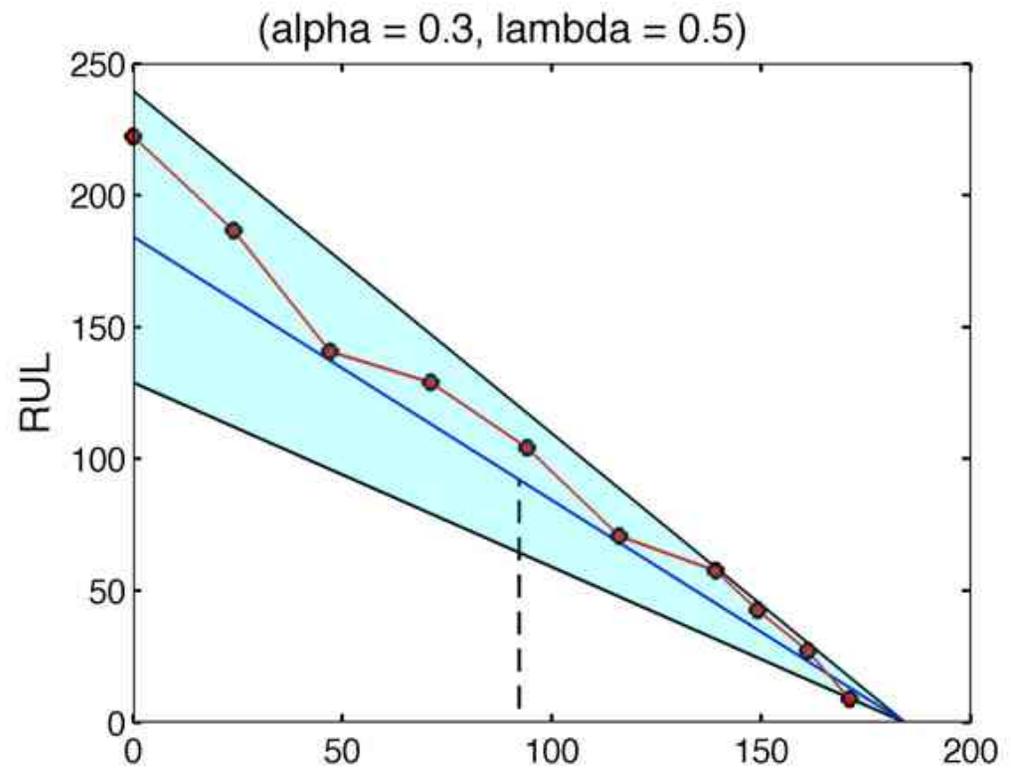
# Kalman Filter based prognostics for Capacitor under electrical overstress



# Kalman Filter based prognostics for Capacitor under electrical overstress



RUL forecasting time (hr)	RUL estimate (hr)	Ground truth (hr)
0	222.2	184.24
24	186.55	160.24
47	140.66	137.24
71	128.98	113.24
94	104.18	90.24
116	70.71	68.24
139	57.58	45.24
149	42.61	35.24
161	27.20	23.24
171	8.94	13.24





Prognostics for Electronics

# **DISCUSSION AND CLOSING REMARKS**

# Discussion

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- Accelerated aging methodologies for electrolytic components have been designed and accelerated aging experiments have been carried out.
- The methodology is based on imposing electrical and/or thermal overstresses via electrical power cycling in order to mimic the real world operation behavior.
- Data are collected in-situ and offline in order to periodically characterize the devices' electrical performance as it ages.
- The data generated through these experiments are meant to provide capability for the validation of prognostic algorithms (both model-based and data-driven).
- Furthermore, the data allow validation of physics-based and empirical based degradation models for this type of capacitor. A first set of models and algorithms has been designed and tested on the data.

# Publications (1/3)

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- [1] G. Sonnenfeld, K. Goebel, and J. R. Celaya, "An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors," in *IEEE AUTOTESTCON 2008*, pp. 208–215, 2008.
- [2] J. R. Celaya, N. Patil, S. Saha, P. Wycoki, and K. Goebel, "Towards accelerated aging methodologies and health management of power MOSFETs," in *Annual Conference of the Prognostics and Health Management Society, 2009*, (San Diego, CA), 2009.
- [3] J. R. Celaya, S. Saha, P. Wycoki, and K. F. Goebel, "Effects of lightning injection on power-MOSFETs," in *Annual Conference of the Prognostics and Health Management Society, 2009*, (San Diego, CA), 2009.
- [4] J. J. Ely, T. X. Nguyen, G. N. Szatkowski, S. V. Koppen, J. J. Mielnik, R. K. Vaughan, P. F. Wysocki, J. R. Celaya, and S. Saha, "Lightning pin injection testing on MOSFETs," *NASA Technical Memorandum*, vol. TM-2009-215794, 2009.
- [5] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics," *IEEE Transactions on Reliability*, vol. 58, no. 2, pp. 271–276, 2009.
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Questions

**THANK YOU!**

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