High-Speed, Multi-Channel Serial ADC LVDS Interface for Xilinx Virtex-5 FPGA

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Analog-to-digital converters (ADCs) are used in scientific and communications instruments on all spacecraft. As data rates get higher, and as the transition is made from parallel ADC designs to high-speed, serial, low-voltage differential signaling (LVDS) designs, the need will arise to interface these in field-programmable gate arrays (FPGAs). As Xilinx has released the radiation-hardened version of the Virtex-5, this will likely be used in future missions.

High-speed serial ADCs send data at very high rates. A de-serializer instantiated in the fabric of the FPGA could not keep up with these high data rates. The Virtex-5 contains primitives designed specifically for high-speed, source-synchronous de-serialization, but as supported by Xilinx, can only support bitwidths of 10. Supporting bitwidths of 12 or more requires the use of the primitives in an undocumented configuration, a non-trivial task.

De-serializing the bits from high-speed ADCs running at speeds of 50 Msps or more becomes a non-trivial