Gigabit Ethernet Asynchronous Clock Compensation FIFO
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Clock compensation for Gigabit Ethernet is necessary because the clock recovered from the 1.25 Gb/s serial data stream has the potential to be 200 ppm slower or faster than the system clock. The serial data is converted to 10-bit parallel data at a 125 MHz rate on a clock recovered from the serial data stream. This recovered data needs to be processed by a system clock that is also running at a nominal rate of 125 MHz, but not synchronous to the recovered clock. To cross clock domains, an asynchronous FIFO (first-in-first-out) is used, with the write pointer (wptr) in the recovered clock domain and the read pointer (rptr) in the system clock domain. Because the clocks are generated from separate sources, there is potential for FIFO overflow or underflow.

Clock compensation in Gigabit Ethernet is possible by taking advantage of the protocol data stream features. There are two distinct data streams that occur in Gigabit Ethernet where identical data is transmitted for a period of time. The first is configuration, which happens during auto-negotiation. The second is idle, which occurs at the end of auto-negotiation and between every packet. The identical data in the FIFO can be repeated by decrementing the read pointer, thus compensating for a FIFO that is draining too fast. The identical data in the FIFO can also be skipped by incrementing the read pointer, which compensates for a FIFO draining too slowly. The unique and novel features of this FIFO are that it works in both the idle stream and the configuration streams. The increment or decrement of the read pointer is different in the idle and compensation streams to preserve disparity. Another unique feature is that the read pointer to write pointer difference range changes between compensation and idle to minimize FIFO latency during packet transmission.

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High-Speed, Multi-Channel Serial ADC LVDS Interface for Xilinx Virtex-5 FPGA
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Analog-to-digital converters (ADCs) are used in scientific and communications instruments on all spacecraft. As data rates get higher, and as the transition is made from parallel ADC designs to high-speed, serial, low-voltage differential signaling (LVDS) designs, the need will arise to interface these in field-programmable gate arrays (FPGAs). As Xilinx has released the radiation-hardened version of the Virtex-5, this will likely be used in future missions.

High-speed serial ADCs send data at very high rates. A de-serializer instantiated in the fabric of the FPGA could not keep up with these high data rates. The Virtex-5 contains primitives designed specifically for high-speed, source-synchronous de serialization, but as supported by Xilinx, can only support bit-widths of 10. Supporting bit-widths of 12 or more requires the use of the primitives in an undocumented configuration, a non-trivial task.

De-serializing the bits from high-speed ADCs running at speeds of 50 Msp/s or more becomes a non-trivial