dust barriers, contactless connector systems, and smooth connector systems. The conventional connector with protective dust barrier mitigates dust by incorporating a physical dust shield. These dust barriers may be retrofitted to existing military or International Space Station connectors. Alternatively, it is possible to utilize existing connectors that can be incorporated into a universal connector housing. Contactless connectors have advantages over conventional connectors where environment integrity poses a design constraint.

The dust-tolerant intelligent electrical connection system has several novel concepts and unique features. It combines intelligent cable diagnostics (health monitoring) and automatic circuit routing capabilities into a dust-tolerant electrical umbilical. It retrofits a clamshell protective dust cover to an existing connector for reduced gravity operation, and features a universal connector housing with three styles of dust protection: inverted cap, rotating cap, and clamshell. It uses a self-healing membrane as a dust barrier for electrical connectors where required, while also combining lotus leaf technology for applications where a dust-resistant coating providing low surface tension is needed to mitigate Van der Waals forces, thereby disallowing dust particle adhesion to connector surfaces. It also permits using a ruggedized iris mechanism with an embedded electrodynamic dust shield as a dust barrier for electrical connectors where required.

The system also can use a coating to repel lunar dust and self-clean the surface, and incorporates cable health monitoring and automatic routing capabilities into an inductively coupled or capacitively coupled contactless electrical connector. An innovative knob and donut type connector is also included to mitigate lunar dust challenges. Adding electrodynamic dust shields is also possible where needed to combine active dust mitigation with EMI (electromagnetic interference) shielding capability.

This work was done by Mark Lewis, Adam Dokos, Jose Perotti, Carlos Calle, and Robert Mueller of Kennedy Space Center; and Gary Bastin, Jeffrey Carlson, Ivan Townsend III, Christopher Immer, and Pedro Modelius of ASRC Aerospace Corporation. For more information, contact the Kennedy Space Center Innovative Partnerships Office at (321) 867-5033. KSC-13578

Gigabit Ethernet Asynchronous Clock Compensation FIFO

Lyndon B. Johnson Space Center, Houston, Texas

Clock compensation for Gigabit Ethernet is necessary because the clock recovered from the 1.25 Gb/s serial data stream has the potential to be 200 ppm slower or faster than the system clock. The serial data is converted to 10-bit parallel data at a 125 MHz rate on a clock recovered from the serial data stream. This recovered data needs to be processed by a system clock that is also running at a nominal rate of 125 MHz, but not synchronous to the recovered clock. To cross clock domains, an asynchronous FIFO (first-in-first-out) is used, with the write pointer (wprt) in the recovered clock domain and the read pointer (rprt) in the system clock domain. Because the clocks are generated from separate sources, there is potential for FIFO overflow or underflow.

This work was done by Jeff Duhachek of Honeywell Aerospace for Johnson Space Center. For further information, contact the JSC Innovation Partnerships Office at (281) 483-3809. MSC-24853-1

High-Speed, Multi-Channel Serial ADC LVDS Interface for Xilinx Virtex-5 FPGA

NASA’s Jet Propulsion Laboratory, Pasadena, California

Analog-to-digital converters (ADCs) are used in scientific and communications instruments on all spacecraft. As data rates get higher, and as the transition is made from parallel ADC designs to high-speed, serial, low-voltage differential signaling (LVDS) designs, the need will arise to interface these in field-programmable gate arrays (FPGAs). As Xilinx has released the radiation-hardened version of the Virtex-5, this will likely be used in future missions.

High-speed serial ADCs send data at very high rates. A de-serializer instantiated in the fabric of the FPGA could not keep up with these high data rates. The Virtex-5 contains primitives designed specifically for high-speed, source-synchronous de-serialization, but as supported by Xilinx, can only support bit-widths of 10. Supporting bit-widths of 12 or more requires the use of the primitives in an undocumented configuration, a non-trivial task.

De-serializing the bits from high-speed ADCs running at speeds of 50 Msps or more becomes a non-trivial