

Iridium Interfacial Stack — IrIS

A bondable metallization stack prevents diffusion of oxygen and gold into silicon carbide monolithically integrated circuits operating above 500 °C.

John H. Glenn Research Center, Cleveland, Ohio

Iridium Interfacial Stack (IrIS) is the sputter deposition of high-purity tantalum silicide (TaSi₂-400 nm) / platinum (Pt-200 nm) / iridium (Ir-200 nm) / platinum (Pt-200 nm) in an ultra-high vacuum system followed by a 600 °C anneal in nitrogen for 30 minutes. IrIS simultaneously acts as both a bond metal and a diffusion barrier. This bondable metallization that also acts as a diffusion barrier can prevent oxygen from air and gold from the wire-bond from infiltrating silicon carbide (SiC) monolithically integrated circuits (ICs) operating above 500 °C in air for over 1,000 hours. This TaSi₂/Pt/Ir/Pt metallization is easily bonded for electrical connection to off-chip circuitry and does not require extra anneals or masking steps.

There are two ways that IrIS can be used in SiC ICs for applications above

500 °C: it can be put directly on a SiC ohmic contact metal, such as Ti, or be used as a bond metal residing on top of an interconnect metal. For simplicity, only the use as a bond metal is discussed. The layer thickness ratio of TaSi₂ to the first Pt layer deposited thereon should be 2:1. This will allow Si from the TaSi₂ to react with the Pt to form Pt₂Si during the 600 °C anneal carried out after all layers have been deposited. The Ir layer does not readily form a silicide at 600 °C, and thereby prevents the Si from migrating into the top-most Pt layer during future anneals and high-temperature IC operation. The second (i.e., top-most) deposited Pt layer needs to be about 200 nm to enable easy wire bonding. The thickness of 200 nm for Ir was chosen for initial experiments; further optimization

of the Ir layer thickness may be possible via further experimentation. Ir itself is not easily wire-bonded because of its hardness and much higher melting point than Pt. Below the iridium layer, the TaSi₂ and Pt react and form desired Pt₂Si during the post-deposition anneal while above the iridium layer remains pure Pt as desired to facilitate easy and strong wire-bonding to the SiC chip circuitry.

This work was done by David Spry of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18736-1.

Downsampling Photodetector Array With Windowing

Applications include laser ranging for commercial surveys, and building-to-building optical data links.

NASA's Jet Propulsion Laboratory, Pasadena, California

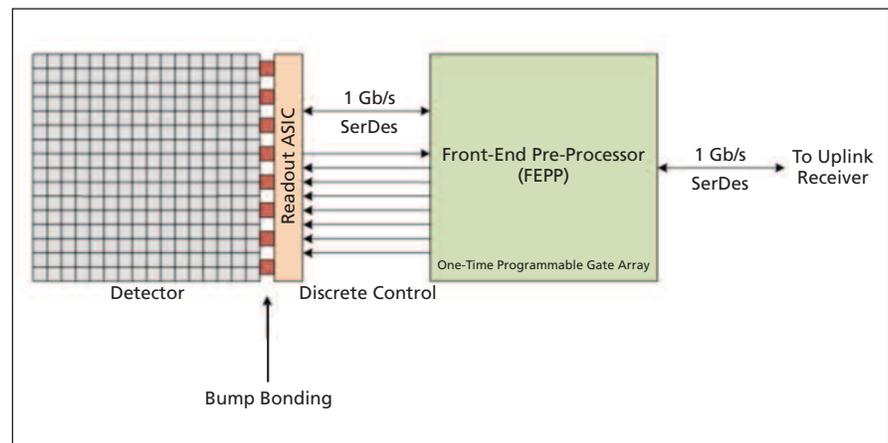
In a photon counting detector array, each pixel in the array produces an electrical pulse when an incident photon on that pixel is detected. Detection and demodulation of an optical communication signal that modulated the intensity of the optical signal requires counting the number of photon arrivals over a given interval. As the size of photon counting photodetector arrays increases, parallel processing of all the pixels exceeds the resources available in current application-specific integrated circuit (ASIC) and gate array (GA) technology; the desire for a high fill factor in avalanche photodiode (APD) detector arrays also precludes this.

Through the use of downsampling and windowing portions of the detector array, the processing is distributed between the ASIC and GA. This allows demodulation of the optical communication signal incident on a large photon counting detector array, as well as providing architecture amenable to algorithmic changes.

The detector array readout ASIC functions as a parallel-to-serial con-

verter, serializing the photodetector array output for subsequent processing. Additional downsampling functionality for each pixel is added to this ASIC. Due to the large number of pixels in the array, the readout time of the entire photodetector is greater than the time between photon arrivals; therefore, a downsampling pre-pro-

cessing step is done in order to increase the time allowed for the readout to occur. Each pixel drives a small counter that is incremented at every detected photon arrival or, equivalently, the charge in a storage capacitor is incremented. At the end of a user-configurable counting period (calculated independently from the ASIC),



Processing can be distributed across an ASIC and GA through downsampling and windowing portions of the **Detector Array**.