



Radiation-Hard SpaceWire/Gigabit Ethernet-Compatible Transponder

Transponder features low power and low fabrication cost.

Goddard Space Flight Center, Greenbelt, Maryland

A radiation-hard transponder was developed utilizing submicron/nano-technology from IBM. The device consumes low power and has a low fabrication cost. This device utilizes a Plug-and-Play concept, and can be integrated into intra-satellite networks, supporting SpaceWire and Gigabit Ethernet I/O. A space-qualified, 100-pin package also was developed, allowing space-qualified (class K) transponders to be delivered within a six-month time frame.

The novel, optical, radiation-tolerant transponder was implemented as a standalone board, containing the transponder ASIC (application specific integrated circuit) and optical module, with an FPGA (field-programmable gate array) friendly parallel interface. It features improved radiation tolerance; high-data-rate, low-power consumption; and advanced functionality. The transponder utilizes a patented current-mode logic library of radiation-hardened-by-architecture cells. The transpon-

der was developed, fabricated, and radiation tested up to 1 MRad. It was fabricated using 90-nm CMOS (complementary metal oxide semiconductor) 9 SF process from IBM, and incorporates full BIT circuitry, allowing a loop back test.

The low-speed parallel LVCMOS (low-voltage complementary metal oxide semiconductor) bus is compatible with Actel FPGA. The output LVDS (low-voltage differential signaling) interface operates up to 1.5 Gb/s. Built-in CDR (clock-data recovery) circuitry provides robust synchronization and incorporates two alarm signals such as synch loss and signal loss. The ultra-linear peak detector scheme allows on-line control of the amplitude of the input signal. Power consumption is less than 300 mW.

The developed transponder with a 1.25 Gb/s serial data rate incorporates a 10-to-1 serializer with an internal clock multiplication unit and a 10-1 deserializer with internal clock and data recovery block, which can operate with 8B10B

encoded signals. Three loop-back test modes are provided to facilitate the built-in-test functionality. The design is based on a proprietary library of differential current switching logic cells implemented in the standard 90-nm CMOS 9SF technology from IBM. The proprietary low-power LVDS physical interface is fully compatible with the SpaceWire standard, and can be directly connected to the SFP MSA (small form factor pluggable Multiple Source Agreement) optical transponder. The low-speed parallel interfaces are fully compatible with the standard 1.8 V CMOS input/output devices. The utilized proprietary annular CMOS layout structures provide TID tolerance above 1.2 MRad. The complete chip consumes less than 150 mW of power from a single 1.8-V positive supply source.

This work was done by Vladimir Katzman of Adsantec for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16038-1

Hardware Implementation of Lossless Adaptive Compression of Data From a Hyperspectral Imager

Implementation uses a new version of the algorithm that targets pushbroom-type imagers in order to be suitable for use on satellites.

NASA's Jet Propulsion Laboratory, Pasadena, California

Efficient onboard data compression can reduce the data volume from hyperspectral imagers on NASA and DoD spacecraft in order to return as much imagery as possible through constrained downlink channels. Lossless compression is important for signature extraction, object recognition, and feature classification capabilities. To provide onboard data compression, a hardware implementation of a lossless hyperspectral compression algorithm was developed using a field programmable gate array (FPGA). The underlying algorithm is the Fast Lossless (FL) com-

pression algorithm reported in "Fast Lossless Compression of Multispectral-Image Data" (NPO-42517), *NASA Tech Briefs*, Vol. 30, No. 8 (August 2006), p. 26 with the modification reported in "Lossless, Multi-Spectral Data Compressor for Improved Compression for Pushbroom-Type Instruments" (NPO-45473), *NASA Tech Briefs*, Vol. 32, No. 7 (July 2008) p. 63, which provides improved compression performance for data from pushbroom-type imagers. An FPGA implementation of the unmodified FL algorithm was previously developed and reported in "Fast and Adaptive Lossless

Onboard Hyperspectral Data Compression System" (NPO-46867), *NASA Tech Briefs*, Vol. 36, No. 5 (May 2012) p. 42. The essence of the FL algorithm is adaptive linear predictive compression using the sign algorithm for filter adaptation. The FL compressor achieves a combination of low complexity and compression effectiveness that exceeds that of state-of-the-art techniques currently in use. The modification changes the predictor structure to tolerate differences in sensitivity of different detector elements, as occurs in pushbroom-type imagers, which are suitable for spacecraft use.

The FPGA implementation offers a low-cost, flexible solution compared to traditional ASIC (application specific integrated circuit) and can be integrated as an intellectual property (IP) for part of, e.g., a design that manages the instrument interface. The FPGA implementation was benchmarked on the Xilinx Virtex IV LX25 device, and ported to a Xilinx prototype board. The

current implementation has a critical path of 29.5 ns, which dictated a clock speed of 33 MHz. The critical path delay is end-to-end measurement between the uncompressed input data and the output compression data stream. The implementation compresses one sample every clock cycle, which results in a speed of 33 Msample/s. The implementation has a rather low device use of the

Xilinx Virtex IV LX25, making the total power consumption of the implementation about 1.27 W.

This work was done by Didier Keymeulen, Nazeeh I. Aranki, and Matthew A. Klimesh of Caltech, and Alireza Bakhshi of B&A Engineering for NASA's Jet Propulsion Laboratory. For more information, contact iaofjice@jpl.nasa.gov. NPO-47103

High-Voltage, Low-Power BNC Feedthrough Terminator

John F. Kennedy Space Center, Florida

This innovation is a high-voltage, low-power BNC (Bayonet Neill–Concelman) feedthrough that enables the user to terminate an instrumentation cable properly while connected to a high voltage, without the use of a voltage divider. This feedthrough is low power, which will not load the source, and will properly terminate the instrumentation cable to the instrumentation, even if the cable impedance is not constant.

The Space Shuttle Program had a requirement to measure voltage transients on the orbiter bus through the Ground Lightning Measurement System (GLMS). This measurement has a bandwidth requirement of 1 MHz. The GLMS voltage measurement is connected to the or-

biter through a DC panel. The DC panel is connected to the bus through a non-uniform cable that is approximately 75 ft (≈ 23 m) long. A 15-ft (≈ 5 -m), 50-ohm triaxial cable is connected between the DC panel and the digitizer. Based on calculations and simulations, cable resonances and reflections due to mismatched impedances of the cable connecting the orbiter bus and the digitizer causes the output not to reflect accurately what is on the bus. A voltage divider at the DC panel, and terminating the 50-ohm cable properly, would eliminate this issue. Due to implementation issues, an alternative design was needed to terminate the cable properly without the use of a voltage divider.

Analysis shows how the cable resonances and reflections due to the mismatched impedances of the cable connecting the orbiter bus and the digitizer causes the output not to reflect accurately what is on the bus. After simulating a dampening circuit located at the digitizer, simulations were performed to show how the cable resonances were dampened and the accuracy was improved significantly. Test cables built to verify simulations were accurate. Since the dampening circuit is low power, it can be packaged in a BNC feedthrough.

This work was done by Douglas (Doug) Bearden of Kennedy Space Center. Further information is contained in a TSP (see page 1). KSC-13560

SpaceCube Mini

A unit that is being designed will be a very compact and low-power system.

Goddard Space Flight Center, Greenbelt, Maryland

This version of the SpaceCube will be a full-fledged, onboard space processing system capable of 2500+ MIPS, and featuring a number of plug-and-play gigabit and standard interfaces, all in a condensed 3×3×3 form factor [<10 watts and < 3 lb (≈ 1.4 kg)]. The main processing engine is the Xilinx SIRF radiation-hardened-by-design Virtex-5 FX-130T field-programmable gate array (FPGA).

Even as the SpaceCube 2.0 version (currently under test) is being targeted as the platform of choice for a number of the upcoming Earth Science Decadal Survey missions, GSFC has been contacted by customers who wish to see a system that incorporates key features of the version 2.0 architecture in an even smaller form factor. In order to fulfill

that need, the SpaceCube Mini is being designed, and will be a very compact and low-power system. A similar flight system with this combination of small size, low power, low cost, adaptability, and extremely high processing power does not otherwise exist, and the SpaceCube Mini will be of tremendous benefit to GSFC and its partners.

The SpaceCube Mini will utilize space-grade components. The primary processing engine of the Mini is the Xilinx Virtex-5 SIRF FX-130T radiation-hardened-by-design FPGA for critical flight applications in high-radiation environments. The Mini can also be equipped with a commercial Xilinx Virtex-5 FPGA with integrated PowerPCs for a low-cost, high-power computing platform for use in the relatively radia-

tion-benign LEOs (low-Earth orbits). In either case, this version of the SpaceCube will weigh less than 3 pounds (≈ 1.4 kg), conform to the CubeSat form-factor (10×10×10 cm), and will be low power (<10 watts for typical applications). The SpaceCube Mini will have a radiation-hardened Aeroflex FPGA for configuring and scrubbing the Xilinx FPGA by utilizing the onboard FLASH memory to store the configuration files. The FLASH memory will also be used for storing algorithm and application code for the PowerPCs and the Xilinx FPGA. In addition, it will feature high-speed DDR SDRAM (double data rate synchronous dynamic random-access memory) to store the instructions and data of active applications. This version will also feature SATA-II and Gigabit