

# Packaging Technologies for High Temperature Electronics and Sensors

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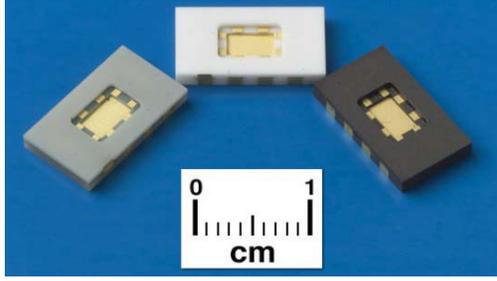
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## Abstract

This paper reviews ceramic substrates and thick-film metallization based packaging technologies in development for 500°C silicon carbide (SiC) electronics and sensors. Prototype high temperature ceramic chip-level packages and printed circuit boards (PCBs) based on ceramic substrates of aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) and aluminum nitride (AlN) have been designed and fabricated. These ceramic substrate-based chip-level packages with gold (Au) thick-film metallization have been electrically characterized at temperatures up to 550°C. A 96% alumina based edge connector for a PCB level subsystem interconnection has also been demonstrated recently. The 96% alumina packaging system composed of chip-level packages and PCBs has been tested with high temperature SiC devices at 500°C for over 10,000 hours. In addition to tests in a laboratory environment, a SiC JFET with a packaging system composed of a 96% alumina chip-level package and an alumina printed circuit board mounted on a data acquisition circuit board was launched as a part of the MISSE-7 suite to the International Space Station via a Shuttle mission. This packaged SiC transistor was successfully tested in orbit for eighteen months. A spark-plug type sensor package designed for high temperature SiC capacitive pressure sensors was developed. This sensor package combines the high temperature interconnection system with a commercial high temperature high pressure stainless steel seal gland (electrical feed-through). Test results of a packaged high temperature capacitive pressure sensor at 500°C are also discussed. In addition to the pressure sensor package, efforts for packaging high temperature SiC diode-based gas chemical sensors are in process.

## Introduction

Various SiC electronics and sensors are currently under development for applications in 500°C high temperature environments such as hot sections of aerospace engines and the surface of Venus. In order to conduct long-term tests and eventually commercialize these SiC devices, compatible packaging technologies for the SiC electronics and sensors are required. This article reviews packaging technologies developed for 500°C SiC electronics and sensors to address both component and subsystem level packaging needs for instrumentation for high temperature environments. The packaging system for high temperature SiC electronics includes ceramic chip-level packages, ceramic PCBs, and edge-connectors. High temperature durable die-attach and precious metal wire-bonding are used in the chip-level packaging process. A high temperature sensor package is specifically designed to address high temperature micro-fabricated capacitive pressure sensors for high pressure environments. This paper reviews development of these electronics and sensor packaging technologies, including some test results of SiC electronics and capacitive pressure sensors using these packaging technologies in laboratory as well as in space and flight environments.



**Figure 1:** Prototype high temperature chip-level packages based on aluminum nitride (left), 96% alumina (center), and 90% alumina (right) [4]. These packages have 8 I/Os.

## Electronics Packaging

Compared with other ceramic substrate materials, 96% alumina substrates have better dielectric performance at high temperature [1] while aluminum nitride has a relatively low coefficient of thermal expansion (CTE, 4.5 ppm/K) that is close to that of SiC (4.0 ppm/K). So aluminum nitride substrate based packages provide better thermal-mechanical reliability (compared to alumina with CTE of 7.4 ppm/°K). Selected thick-film materials designed for alumina and aluminum nitride substrates have been tested as substrate metallization for 500°C packaging applications [2,3]. Prototype high temperature ceramic chip-level packages based on ceramic substrates of

aluminum oxides and aluminum nitride have been developed to address packaging needs for small scale 500°C SiC micro-electronics. These ceramic substrates and Au thick-film metallization based packages have been electrically characterized at temperatures up to 550°C [4]. Figure 1 shows prototype high temperature, low power 8-I/O (Input / Output) chip-level packages based on 96% alumina, 90% alumina, and aluminum nitride. Table 1 shows parasitic capacitance and parallel conductance of two neighboring I/Os (one of two I/Os is the ground with relatively larger metallization area) of high temperature low power 8-I/O surface-mount packages of 96% alumina (shown in Figure 1) in a temperature range from room temperature to 550°C, at 100Hz, 120 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz [4]. The upper numbers in each table entry are capacitances in unit of pF (or as indicated in nF), while the lower numbers are parasitic conductances in unit of  $\mu$ S. The package parasitic parameters increase with temperature because of the changes of the dielectric properties of the substrate material with temperature. The data in the table indicate that parasitic effects between two neighboring I/Os basically increase with temperature, but they are satisfactorily low in the entire temperature and frequency ranges. This 96% alumina prototype package meets the basic requirements for packaging many (currently) envisioned high temperature low power and low frequency SiC electronics.

A 96% alumina high temperature circuit board [5] with four SiC devices is shown in Figure 2 [6]. This packaging system has been successfully tested with high temperature SiC JFET (junction gate field-effect transistor) circuits at 500°C for over 10,000 hours. Figure 3 shows I-V curves of a SiC JFET with this packaging system measured at 1, 10, 100, 1,000, and 10,000 hours at 500°C [6]. Without an appropriate packaging, such a long term test of

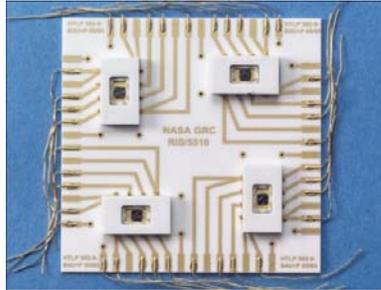
**Table 1:** Parasitic capacitance (upper numbers, in pF or as indicated in nF) and conductance (lower numbers, in  $\mu$ S) of two neighboring I/Os of 96% alumina packages [4]. Those results not measurable are indicated by -.

f (Hz)	T (°C)											
	T <sub>r</sub>	100	150	200	250	300	350	400	450	500	550	
100	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	1.5	-	1	1	1.5	2	2.0	2.0	2.5	4	4	4
	0.000	0.000	0.000	0.000	0.00	0.00	0.000	0.000	0.0015	0.002	0.0025	0.0025
1K	1.5	1.3	1.3	1.4	1.35	1.5	1.6	1.75	1.85	2.15	2.35	2.35
	0.001	0.000	0.00	0.000	0.000	0.001	0.001	0.002	0.0025	0.004	0.0055	0.0055
10K	1.36	1.33	1.3	1.36	1.35	1.46	1.43	1.56	1.54	1.63	1.74	1.74
	0.003	0.000	0.000	0.001	0.001	0.002	0.004	0.006	0.010	0.015	0.020	0.020
100K	1.33	1.38	1.28	1.36	1.36	1.44	1.36	1.427	1.42	1.53	1.47	1.47
	0.015	0.006	0.006	0.007	0.009	0.0135	0.018	0.0255	0.036	0.052	0.071	0.071
1M	1.29	1.30	1.29	1.40	1.35	1.45	1.33	1.39	1.42	1.45	1.47	1.47
	-	-	-	-	-	-	-	-	-	0.043	0.12	0.12

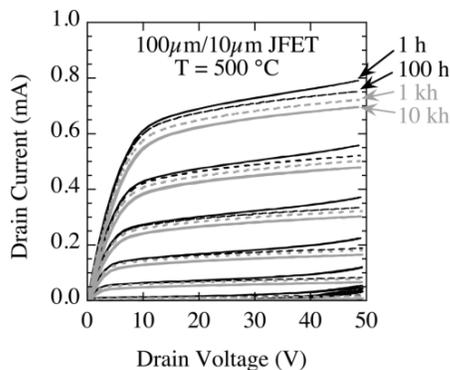
SiC electronics at 500°C would not be possible due to fast degradation of probes. For more detailed analysis of long-term high temperature test results of SiC JFETs see Reference 6. As shown in Figure 2, Au wires were directly and permanently attached to the board for electrical inter-connection to the instruments outside of

the oven for test. A prototype edge-connector socket, consisting of a 96% alumina box and Inconel contact pins/springs mounted on two plug-in units (not shown) for PCB level interconnection, has been initially demonstrated at 500°C. It is still under development for subsystem level integration, as well as more efficient testing of SiC electronics in high temperature environments.

In addition to these high temperature tests in a laboratory environment, a SiC JFET with 96% alumina based packaging system including a chip-level package and a PCB was tested in NASA Space Shuttle flight and Space Station orbit environments.



**Figure 2:** High temperature 96% alumina PCB with four packaged SiC devices [5]. PCB measures 2 inches by 2 inches.



**Figure 3:** Drain I-V curves of a packaged SiC JFET measured at 500°C at 1, 100, 1k, and 10k hours, Gate bias steps -2V from 0V as top curves [6].

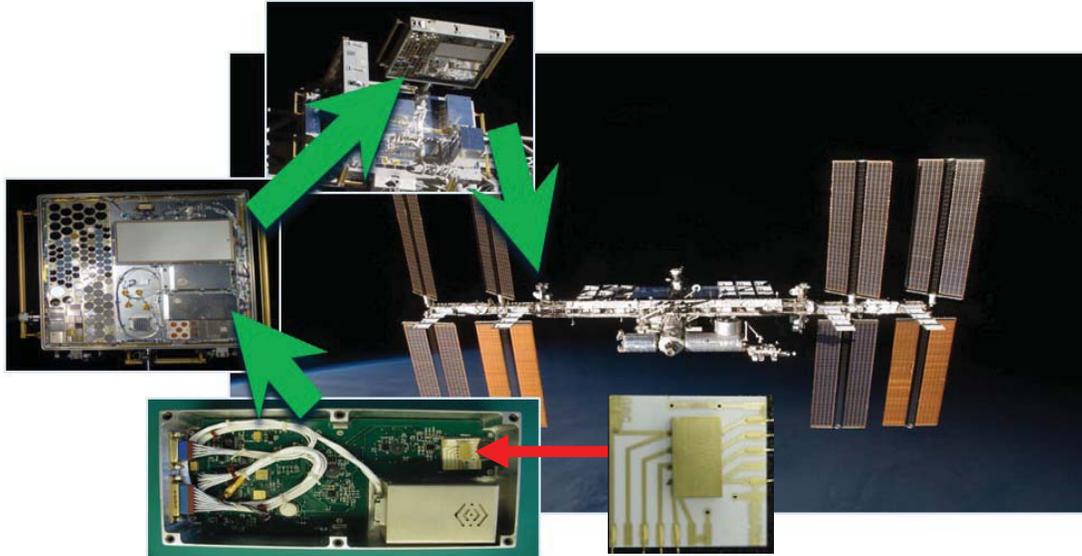
The data acquisition circuit board with a SiC JFET packaged using 96% alumina packaging system is shown in Figure 4 [7]. The 96% alumina packaging system (with a SiC JFET) is shown in the inset of Figure 4. The circuit board was enclosed in an aluminum box. The circuit box was further integrated into one of two Passive Experiment Containers (PEC) of MISSE-7 (Materials International Space Station Experiment 7). The MISSE-7 suite was mounted outside of the Space Station via an astronaut extra vehicular activity (EVA). The packaged SiC JFET was electrically characterized every hour with temperature monitoring on the orbit for a total of eighteen months.

The MISSE-7 suite was exposed to Shuttle launching, atomic oxygen, limited thermal cycling, space radiation, and Shuttle reentry. Figure 5 shows the I-V curves of the packaged SiC JFET measured *in situ* in orbit at 0 hours (the first data acquisition in orbit at this temperature) and 9778 hours (407 days after the first data acquisition). Both in-orbit test results [8] and post-flight examination and test indicate no packaging failure or degradation.

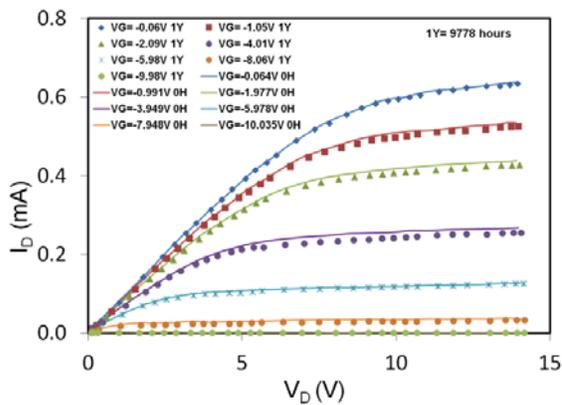
The 96% alumina chip-level packages of this prototype system were not completely fabricated via a commercial co-fire process that is more suitable for large scale low cost commercial production. The co-fired alumina materials adopted by the packaging industry today usually contain glass constituents to provide better adhesion and sealing at interfaces formed during a co-firing process. This co-firing process is performed at temperatures that are typically

lower than the regular sintering temperature for alumina. In order to explore the possibility of using co-fired alumina material systems for high temperature electronics packaging, the dielectric performance of selected high temperature co-fired ceramic (HTCC) alumina (polycrystalline aluminum oxides with glass constituents) substrates were tested at low frequencies ( $\leq 1\text{MHz}$ ) at temperatures up to 550°C. The test results demonstrated better or comparable dielectric performance to that of the 96% alumina indicating a possible future direction of high temperature packaging material systems [9] for commercial production.

A similar aluminum nitride based packaging system is also in parallel development for 500°C applications. However, some commercial aluminum nitride materials demonstrate high dielectric constant and high dielectric loss at elevated temperatures resulting in high parasitic parameters of aluminum nitride substrate based packages. An approach with a glass coating on aluminum nitride surface prior to thick-film metallization was proposed and successfully tested to significantly reduce the parasitic effects of aluminum nitride based packages at temperatures up to 500°C [10].



**Figure 4:** Test of SiC JFET with 96% alumina high temperature packaging system on International Space Station (ISS) orbit via MISSE7 [7].



**Figure 5:** I-V data of SiC JFET with 96% alumina packaging system acquired at 0 hour and 9778 hours on ISS orbit, at temperature of 296 °K.

### Pressure Sensor Packaging

A spark-plug type package designed for high temperature SiC capacitive pressure sensors is shown in Figure 6. An electrical interconnection system composed of a miniaturized ceramic substrate with Au thick-film metallization and attached precious metal wires is sealed in a commercial high temperature, high pressure stainless steel gland [11]. The sensor die is electrically connected to the substrate with Au wire-bonds. Figure 7a and 7b show the parasitic capacitance and parallel conductance, respectively, of the sensor package with four interconnections (wires) designed for sensor chips with dimensions up to 2 mm x 2 mm using Lava [12] as the high temperature sealant.

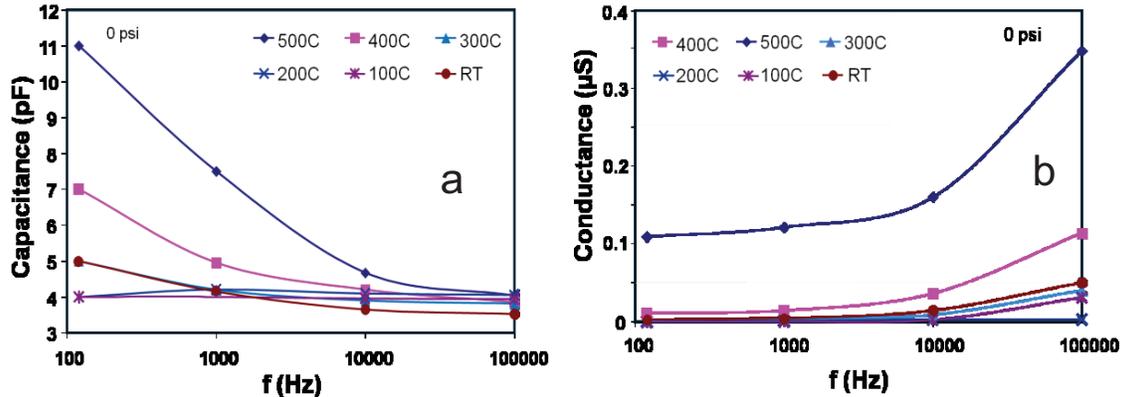
The parasitic capacitance and conductance are measured between two signal wires with a third wire connected to the shield of an LCZ impedance meter. This sensor package provides very low parasitic effects, as shown in Figure 7a and 7b [11]. Since the sealant is under very high compressive stress, this sensor packaging can be used in very high differential pressure environments. A high temperature SiC capacitive pressure sensor with this package has been tested at temperatures up to 500°C. Figure 8 shows test data of capacitance vs. pressure at room temperature and 500°C. The packaging parasitic effects shown in Figure 7a and 7b have been corrected for (subtracted). A low thermal stress die-attach method for high temperature MEMS sensor packaging is discussed in Reference 3. In addition to pressure sensor packaging, packaging efforts for SiC diode based high temperature gas chemical sensors are also in process [12].

## Summary

Ceramic substrates and thick-film metallization based prototype packaging systems including chip-level packages and compatible printed circuit board were demonstrated for 500°C SiC electronics. A compatible alumina edge-connector socket is under

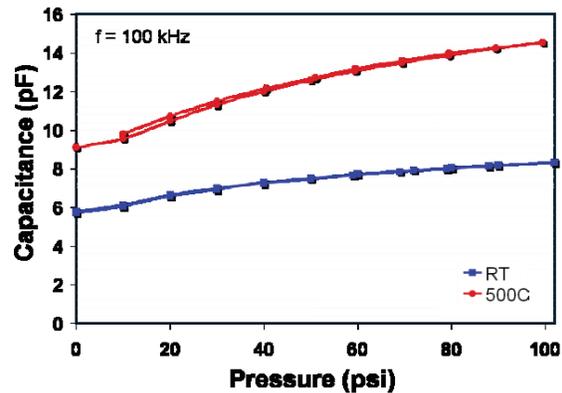


**Figure 6:** Spark-plug type package for high temperature SiC capacitive pressure sensor [11].



**Figure 7:** The parasitic capacitance (a) and parallel conductance (b) of the sensor package with Lava sealant [11]. The package was characterized at 1 atm.

development. The 96% alumina based packaging system has been used to facilitate long-term tests of SiC JFET circuits over 10,000 hours at 500°C. In addition to the tests in the laboratory environment, the 96% alumina packaging system composed of a chip-level package and a PCB has also been tested in Space Shuttle flight and continuous Space Station orbit environments for over eighteen months. Initial test results of selected co-fired alumina material systems show the possibility of using HTCC alumina for future commercialization of high temperature alumina packaging systems. More tests are currently underway to establish an optimal co-fired material system that has improved technical advantages for application at high temperatures, yet is suitable for low cost and large - scale commercial production. A spark-plug type sensor package with low parasitic effects for high temperature capacitive pressure sensors has been developed and tested with SiC sensors at temperatures up to 500°C. This sensor package may be applied to other micro-fabricated solid state sensors for high temperature and high differential pressure environments.



**Figure 8:** The test results of the packaged high temperature SiC capacitive pressure sensor at room temperature and 500°C after overnight heat treatment at 500°C. Lava sealant is used for packaging. The packaging parasitic capacitances have been subtracted [11].

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