



## Ultra-Wideband, Dual-Polarized, Beam-Steering P-Band Array Antenna

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A dual-polarized, wide-bandwidth (200 MHz for one polarization, 100 MHz for the orthogonal polarization) antenna array at P-band was designed to be driven by NASA's EcoSAR digital beam former. EcoSAR requires two wide P-band antenna arrays mounted on the wings of an aircraft, each capable of steering its main beam up to 35° off-boresight, allowing the twin radar beams to be steered at angles to the flight path. The science requirements are mainly for dual-polarization capability and a wide bandwidth of operation of up to 200 MHz if possible, but at least 100 MHz with high polarization port isolation and low cross-polarization. The novel design geometry can be scaled with minor modifications up to about four times higher or down to about half the current design frequencies for any application requiring a dual-polarized, wide-bandwidth steerable antenna array.

EcoSAR is an airborne interferometric P-band synthetic aperture radar (SAR) research application for studying two- and three-dimensional fine-scale measurements of terrestrial ecosystem structure and biomass, which will ulti-

mately aid in the broader study of the carbon cycle and climate change. The two 2×8 element P-band antenna arrays required by the system will be separated by a baseline of about 25 m, allowing for interferometry measurements. The wide 100-to-200-MHz bandwidth dual-polarized beams employed will allow the determination of the amount of biomass and even tree height on the ground.

To reduce the size of the patches along the boresight dimension in order to fit them into the available space, two techniques were employed. One technique is to add slots along the edges of each patch where the main electric currents are expected to flow, and the other technique is to bend the central part of the patch away from the ground plane. The latter also facilitates higher mechanical rigidity.

The high port isolation of more than 40 dB was achieved by employing a highly symmetrical feed mechanism for each pair of elements: three apertures coupling to the patch elements were placed along the two symmetry lines of the antenna element pair. Two apertures were used in tandem to excite two

of the stacked patch elements for one polarization; the other was used to excite one element from one side and the other element from the other side, opposite in phase, taking care of the remaining polarization. The apertures narrow down to a small gap where they are excited by a crossing microstrip line to prevent any asymmetrical excitation of the two sides of the aperture gap, minimizing port-to-port coupling.

Using patches that are non-planar leads to higher mechanical rigidity and smaller patch sizes to fit into the available space. Aperture coupling minimizes direct metal-to-metal connections. Using an aperture coupling feed mechanism results in a feed network for two antenna elements with a total of three feed points, plus one simple in-phase combiner to reduce it to two ports. It greatly reduces the complexity of the alternative, but more conventional, way of feeding a pair of two dual-polarized elements with high port isolation.

*This work was done by Cornelis du Toit of DSFG for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16778-1*

## Centering a DDR Strobe in the Middle of a Data Packet

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The Orion CEV Northstar ASIC (application-specific integrated circuit) project required a DDR (double data rate) memory bus driver/receiver (DDR PHY block) to interface with external DDR memory. The DDR interface (JESD79C) is based on a source synchronous strobe (DQS) that is sent along with each packet of data (DQ). New data is provided concurrently with each edge of strobe and is sent irregularly. In order to capture this data, the strobe needs to be delayed and used to latch the data into a register.

A circuit solves the need for training a DDR PRY block by incorporating a PVT-compensated delay element in the strobe path. This circuit takes an external reference clock signal and uses the regular clock to calibrate a known delay through a data path. The compensated delay DQS signal is then used to capture the DQ data in a normal register. This register structure can be configured as a FIFO (first in first out), in order to transfer data from the DDR domain to the system clock domain. This design is different in that it does

not rely upon the need for training the system response, nor does it use a PLL (phase locked loop) or a DLL (delay locked loop) to provide an offset of the strobe signal.

The circuit is created using standard ASIC building blocks, plus the PVT (process, voltage, and temperature) compensated delay line. The design uses a globally available system clock as a reference, alleviating the need to operate synchronously with the remote memory. The reference clock conditions the PVT compensated delay line to provide a pre-