Rad-Hard Structured ASIC
Body of Knowledge

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Body of Knowledge

NASA Electronic Parts and Packaging (NEPP) Program
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1.0 INTRODUCTION

Structured Application-Specific Integrated Circuit (ASIC) technology is a platform between traditional ASICS and Field-Programmable Gate Arrays (FPGA). The motivation behind structured ASICs is to combine the low non-recurring engineering costs (NRE) costs of FPGAs with the high performance of ASICs.

FPGA technology is designed and fabricated in a process that is completely independent of end-user applications. It is a “one size fits all” approach to providing a programmable circuit that can support many applications. Because the customer has no involvement in FPGA development, there is no NRE cost to the customer. Moreover, because FPGAs are programmable (and some reprogrammable) by the end-user, FPGAs offer maximum flexibility in terms of programming, debugging, and prototyping. However, the routing complexity required to facilitate this flexibility comes at a large price in terms of the speed and performance achievable with an FPGA.

ASICs, on the other hand, are designed and developed with the end user’s application fully in mind. The ASIC is built to support only a single application, and is therefore a one-off development activity for the manufacturer. NRE costs are very high, as entirely new mask sets must be developed to support just a single customer’s needs. In contrast, with the FPGA, every chip is identical. However, because back-end development of an ASIC is done with a single customer’s application in mind, much higher speed and performance is achievable, as routing can be fully optimized for the customer’s specific application.

Structured ASICs aim to offer an intermediate solution. Structured ASICs have essentially the same structure as an FPGA, but they are mask-programmable instead of field-programmable. The manufacturer, therefore, goes through a single design and development activity to produce a structured ASIC platform, then finalizes the chip for each customer through a relatively simple programming step at the end. It follows that some interaction between the manufacturer and customer is required to produce the final circuit, which means more NRE than an FPGA but much less than an ASIC. Structured ASIC programming involves actual fabrication process steps that configure via layers between metal layers to produce the desired circuit. The routing complexity needed is much less than what is required for full field-programmability, so much greater speeds and performance are possible.

This report provides an overview of the structured ASIC platforms that are radiation-hardened and intended for space application.
2.0 SANDIA NATIONAL LABORATORIES: VIARRAY

Sandia’s structured ASIC product line, known as “ViArray,” debuted in 2005 with the VA260 digital platform. The ViArray process was originally developed for nuclear weapon applications in a harsh radiation environment, making it ideal for space applications. The VA260 was implemented in Sandia’s 0.35 µm radiation-hardened SOI CMOS, 3.3 V technology. The platform offered 260K logic gates, 354 Kb of SRAM, 352 Kb of ROM, an on-chip oscillator, and 170 configurable I/Os.

The ViArray product line quickly moved away from VA260 in 2007 with the announcement of the Eiger (digital) and Whistler (mixed-signal, 2009) platforms (see Figure 2.0-1). The baseline process behind these platforms is also the radiation-hardened 3.3 V, 0.35 µm SOI CMOS. It has advanced significantly since the VA260 days and now supports 24 mask levels, SOI substrate, STI hardened field oxide, nitride trench capacitors, LDD implants, 7 nm tunnel oxide thickness, poly SEU transistors, titanium silicide, tungsten via fills, metal/metal capacitors, and L_EFF of 0.28 µm (V_T ~0.7 V and 1.0 V).

In addition to the Eiger and Whistler platforms, Sandia also offers ViArray embedded in custom ASICs. Beginning in 2012, 3D-ViArray (stacked chips) went into development to bring more performance in a smaller package/footprint. So far, all ViArray chips have been in plastic BGA packages. However, Sandia has started development on ceramic column grid arrays, flip-chip PBGA, and flip-chip on-board technologies.

2.1.1 Performance Specs and Radiation Characterization

A comparison of the Eiger and Whistler platforms, including radiation performance, is given in Table 2.1.1-1.

<table>
<thead>
<tr>
<th></th>
<th>Eiger Digital Rad-Hard ViArray</th>
<th>Whistler Mixed-Signal Rad-Hard ViArray</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35 µm SOI CMOS</td>
<td>0.35 µm SOI CMOS</td>
</tr>
<tr>
<td>VDD</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>−55°C to 125°C</td>
<td>−55°C to 125°C</td>
</tr>
<tr>
<td>ASIC gate-equivalent</td>
<td>276K</td>
<td>138K</td>
</tr>
<tr>
<td>Dual-Port SRAM</td>
<td>368 Kb</td>
<td>184 Kb</td>
</tr>
<tr>
<td>Configurable ROM</td>
<td>384 Kb</td>
<td>192 Kb</td>
</tr>
<tr>
<td>Volatile Memory</td>
<td>2 Kb</td>
<td>–</td>
</tr>
<tr>
<td>Oscillators</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Phase Lock Loops</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 2.0-1. Sample chips of Sandia’s Eiger (digital) and Whistler (mixed-signal) structured ASIC platforms [1].
### 2.1.2 Flight Heritage

NASA JPL/Caltech and Sandia worked closely together while the ViArray platform was a candidate to provide rad-hard integrated circuits for the Europa Jupiter System Mission (EJSM) before the project was canceled [2].

Currently, NASA Goddard is building a prototype proof of concept system-on-a-chip utilizing the Whistler platform [2].

### 2.1.3 Design Tools

The ViArray design flow is based on standard ASIC design tools, but heavily augmented with Sandia-produced intellectual property and scripts to automate recurring design tasks that are specific to the ViArray platforms. A list of the electronic design automation (EDA) tools used in ViArray design is given in Table 2.1.3-1.

<table>
<thead>
<tr>
<th>Design Step</th>
<th>Design Tool</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTL/gate-level simulation</td>
<td>Mentor ModelSim</td>
</tr>
<tr>
<td>Mixed-signal spice/RTL simulation (optional)</td>
<td>Cadence AMS</td>
</tr>
<tr>
<td>Pad-frame generation, vector generation, testbench generation, ASIC tester definitions</td>
<td>Sandia scripts</td>
</tr>
<tr>
<td>Logic synthesis, scan insertion, STA, ATPG</td>
<td>Synopsys tools</td>
</tr>
<tr>
<td>Auto Place &amp; Route</td>
<td>ViASIC ViaPath</td>
</tr>
<tr>
<td>Parasitic extraction, power analysis, LVS, DRC, mask generation</td>
<td>Cadence &amp; Mentor tools</td>
</tr>
</tbody>
</table>

#### Table 2.1.3-1. ViArray Design Tools.
2.1.4 **Design Security**

FPGAs have a distinct advantage over ASICs (and structured ASICs) in terms of design security. Since FPGAs are field-programmable by the end-user, the application design does not need to be shared with a third party (the manufacturer). However, by using a trusted vendor, security risks can be mitigated.

Sandia is a DoD Category 1A Accredited Supplier of both “trusted design and foundry services” with ISO 9001 certified process optimized for custom radiation-hardened, digital, analog, and mixed-signal ASICs.

2.1.5 **Contact**

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Manager – Mixed Signal ASIC/SoC Products  
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1515 Eubank Blvd. SE  
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3.0 HONEYWELL: HX5000

The HX5000 standard cell, structured ASIC platform went into production in 2007 and received QML Class Q qualification in 2008 [3].

HX5000 is a digital platform built on Honeywell’s S150 process, a 1.8 V, 0.15 μm SOI CMOS technology. HX5000 provides more than 15M usable gates and supports up to 1000 signal I/Os.

3.1.1 Performance Specs and Radiation Characterization

Table 3.1.1-1. Honeywell HX5000 Performance Specs and Radiation Characterization.

<table>
<thead>
<tr>
<th></th>
<th>HX5000 (Digital)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.15 μm SOI CMOS</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55°C to 125°C</td>
</tr>
<tr>
<td>VDD</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Signal I/O</td>
<td>1000</td>
</tr>
<tr>
<td>ASIC gate-equivalent</td>
<td>15M</td>
</tr>
<tr>
<td>Package</td>
<td>Ceramic LGA or QFP</td>
</tr>
<tr>
<td>TID</td>
<td>&gt;1 Mrad (Si)</td>
</tr>
<tr>
<td>SEL</td>
<td>Immune</td>
</tr>
<tr>
<td>QML Status</td>
<td>Class Q</td>
</tr>
</tbody>
</table>

3.1.2 Flight Heritage

Honeywell has delivered over 700 ASIC designs on their HX2000, HX3000, and HX5000 process lines. The percentage of these designs that are on the HX5000 standard cell/structured array process is unknown.

3.1.3 Design Tools

Honeywell utilizes the Synopsys Pilot design flow/environment and Mentor tool set, including:

- Design Compiler
- PrimeTime SI
- PrimeTime PX
- Formality
- TetraMAX
- IC Compiler
- StarRCXT
- VCS
- Mentor ModelSim
- Mentor Tessent M-BIST

Honeywell-provided VDS-VI tools:

- IOGen
- Verify
- SpecBuilder/TestSpec
- Test Collar
3.1.4 **Design Security**
Honeywell Aerospace Plymouth is a Category 1A trusted source with accreditation of trust from the Defense Microelectronics Activity (DMEA) as defined by Instruction 8500.2 of the Department of Defense Directives.

3.1.5 **Contact**
Thomas Romanko, Microelectronics Application Engineer
Honeywell Microelectronics
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Plymouth, MN 55441
Office: 763-954-2103
4.0 TRIAD: VCA

Triad is currently in development on radiation-hardened mixed-signal structured ASICs using their patented via-configurable array (VCA) technology, which is based on ViASIC (acquired by Triad in 2011) ViaMask technology [4]. ViASIC used the base technology in high volume commercial applications since 2000. Now Triad is working on using radiation-hardened-by-design (RHBD) techniques to take the product to the military/space market.

Similar to Sandia, Triad offers two platforms: mixed signal and purely digital. The mixed-signal platform is known as “VCA-301” and the six digital platforms are numbered from “VCA-501” thru “VCA-506.”

4.1.1 Performance Specs and Radiation Characterization

Table 4.1.1-1 gives a comparison between the VCA-201 mixed signal platform and the VCA-501 digital platform from Triad. The differences among the six digital platforms are given in Table 4.1.1-2.

<table>
<thead>
<tr>
<th></th>
<th>VCA-301 Mixed Signal</th>
<th>VCA-501 Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18 μm CMOS</td>
<td>IBM 9LP 90 nm CMOS</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>–55°C to 125°C</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>Voltage</td>
<td>1.8 or 3.3 V</td>
<td>1.2 V, 1.2–2.5 V I/O</td>
</tr>
<tr>
<td>TID</td>
<td>&gt;300 krad (Si)</td>
<td>&gt;1 Mrad (Si)</td>
</tr>
<tr>
<td>Gates</td>
<td>28K</td>
<td>&gt;1M</td>
</tr>
<tr>
<td>SEU</td>
<td>&lt;1e–5 errors/day</td>
<td>&lt;1e–5 errors/day</td>
</tr>
<tr>
<td>SEL</td>
<td>Immune</td>
<td>Immune</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Array</th>
<th>Gates</th>
<th>Distributed RAM</th>
<th>Block RAM</th>
<th>VROM</th>
<th>SERDES</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCA-501</td>
<td>107k</td>
<td>78 kb</td>
<td>–</td>
<td>288 kb</td>
<td>–</td>
</tr>
<tr>
<td>VCA-502</td>
<td>177k</td>
<td>129 kb</td>
<td>5× 8k×8</td>
<td>288 kb</td>
<td>4 ch</td>
</tr>
<tr>
<td>VCA-503</td>
<td>239k</td>
<td>213 kb</td>
<td>–</td>
<td>288 kb</td>
<td>–</td>
</tr>
<tr>
<td>VCA-504</td>
<td>490k</td>
<td>356 kb</td>
<td>8× 8k×8</td>
<td>288 kb</td>
<td>8 ch</td>
</tr>
<tr>
<td>VCA-505</td>
<td>225k</td>
<td>164 kb</td>
<td>32× 8k×8</td>
<td>288 kb</td>
<td>–</td>
</tr>
<tr>
<td>VCA-506</td>
<td>1.17M</td>
<td>848 kb</td>
<td>12× 8k×8</td>
<td>288 kb</td>
<td>16 ch</td>
</tr>
</tbody>
</table>

4.1.2 Flight Heritage

None yet. Technology is still under development although prototype chips have undergone TID and SEE testing. Production/flight products are expected late 2013.

4.1.3 Design Tools

One of the biggest selling points for Triad is their ViaDesigner and ViaPath design tools, which promises very rapid ASIC development. With ViaDesigner, you design and simulate your design using high-level resources. ViaPath is then the automatic place and route software that maps your design to a VCA.
4.1.4 Design Security

Triad’s foundry partner is austriamicrosystems (ams), headquartered in Graz, Austria. This is also where their foundry is located, so space programs with requirements for US-trusted foundries may have an issue with this. ams also partners with UMC (Taiwan), TSMC (Taiwan), IBM (US), OKINS (Philippines), FCI (Singapore), Amkor (US/Japan/Philippines), and Carsem (Malaysia) for foundry, test, and assembly services. With so many entities involved in the design, production, and test of the structured ASIC chip, maintaining design security could be an issue.

4.1.5 Contact

Jim Kemerling, CTO
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Office: 336-774-2150
5.0 AEROFLEX

Aeroflex offers a variety of digital and mixed-signal radiation-hardened ASICs for space application, but currently does not offer any structured or standard array technologies; nor do they currently have any on their product roadmap.

A datasheet for “UT0.25µHBD Hardened-by-Design Structured Array” was once available, but Aeroflex did not identify a sufficient market to justify the development effort.
6.0 CONCLUSION

Sandia, Honeywell, and Triad are the three options space programs have when considering radiation-hardened structured-ASIC platforms.

For most programs, Honeywell is probably the best choice. HX5000 is a mature and proven process with the most performance and capability. Honeywell also has MIL-PRF-38535 Class Q qualification and certification.

From the design perspective, Triad is probably the best option since they provide their own design tools. Controlling both the software and hardware makes for a well-integrated design environment. However, Triad’s manufacturing process, which involves many international partners, could be an issue for space projects with strict security requirements.

Sandia’s platforms, although also based on mature and well-established processes, are several generations behind Honeywell in terms of performance and capability. In addition, Sandia’s devices are packaged in non-hermetic plastic LGAs, which is a less desirable format than hermetic ceramic packaging.

<table>
<thead>
<tr>
<th>Table 6.0-1. Rad-Hard Structured ASIC Technology Comparison (Digital).</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
</tr>
<tr>
<td>Process</td>
</tr>
<tr>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>Gates</td>
</tr>
<tr>
<td>TID</td>
</tr>
<tr>
<td>Package</td>
</tr>
<tr>
<td>QML</td>
</tr>
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7.0 REFERENCES

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14. ABSTRACT
Structured Application-Specific Integrated Circuit (ASIC) technology is a platform between traditional ASICs and Field-Programmable Gate Arrays (FPGA). The motivation behind structured ASICs is to combine the low non-recurring engineering costs (NRE) costs of FPGAs with the high performance of ASICs. This report provides an overview of the structured ASIC platforms that are radiation-hardened and intended for space application.

15. SUBJECT TERMS
structured asic, sandia, aeroflex, honeywell, triad

16. SECURITY CLASSIFICATION OF:

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<th>c. THIS PAGE</th>
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