Soft Decision Analyzer

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Communication System
with Open-Loop Testing

Data to Transmit → Source Coding → Channel Coding → Modulate & Transmit

Source Coding

Channel Coding

Communication Channel

Receive & Demodulate

Received Data → Source Coding → Channel Coding → Soft Decision Analyzer

Soft Decision Analyzer
High-Performance Soft Decision Block Codes

• Modern block decoders can operate at 10% SER or higher
• The decoder cannot operate on a PRBS BERT pattern
• If you break the link to change the data pattern, it reacquires with a different alignment, and you change the performance
• For testing soft-decision block codes with practical receivers and a practical channel, an instrument was needed that could
  – Analyze framed code-blocks (“live data” not just PRBS)
  – Detect and track receiver threshold effects like slips and rotations
As Modern Error Correction Approaches the Shannon Limit, Receivers Must Contend with Ultra-Low SNRs
Communication System
with Closed-Loop Testing

Data to Transmit → Source Coding → Channel Coding → Modulate & Transmit

Sending Data through Source Coding and Channel Coding to Modulate and Transmit.

Received Data → Source Coding → Channel Coding → Receive & Demodulate

Data Reception and Decoding Process.
SDA Measurable Parameters

- Acquired Clock
- Acquired Data
- Stable Carrier
- Stable Clock
- Stable Data
- Modulation Quadrant
- Symbol Error Rate
- Loss of Signal Detection, Recovery, & Rate
- Rotation Detection, Recovery, & Rate
- Slip Detection, Recovery, & Rate
- Data Run Length
- Delay
- Data Rate
- Data Distribution Histograms
- Signal-to-Noise Ratio
- LDPC Combining Ratio
- Inter-symbol Interference
- Inter-channel Interference
- Decision Threshold Imbalance
- Data Imbalance
- Channel Imbalance
Connecting Test Points

1) Receiver Test with Transmitter and Channel, no Decoder

2) Receiver Test with Transmitter and Channel, Translation for Decoder

3) Receiver Test with Transmitter and Channel, Integrated with Decoder

Clock and Data, as transmitted
Hard vs. Soft Decision

• For binary communications, hard decisions are simply the 1’s and 0’s. Soft decisions also contain the 1’s and 0’s, but also a level of confidence.

• The number of confidence levels is determined by the number of bits used for soft decisions.

• Example of 3-bit soft decision:
  – 011 (Strongest 0)
  – 010
  – 001
  – 000 (Weakest 0)
  – 100 (Weakest 1)
  – 101
  – 110
  – 111 (Strongest 1)
Input and Output Scaling

• Input and output scale tables are used to accommodate variation in bus widths, number representation, and statistical average.

• Problems with logic polarity and pin swapping can be corrected at the click of a mouse.

• The output bus allows SDA to translate between a transmitter and a receiver built to different specifications.
Correlators

- **SDA** can acquire and maintain reliable correlation between Reference and Test data streams at SERs in excess of 30%. At 17% SER, the SDA can recover from a slip in less than 600 bits.
- Alignment is continuously monitored. Each symbol interval, correlation is evaluated in each of four quadrants for each of nine alignments. The window is re-centered after each slip detection.
- A variable-width correlator (16 to 512 bits) is available, trading resolution for stability.
- Three parameters control hysteresis and squelch
  - Variable-length running totals of how many times each alignment has been best, used to select a winner
  - A variable-length lock-out following an alignment change
  - A correlation quality threshold invokes flywheeling
Maintaining Alignment

On-time correlator “Early-0” (E0) wins

Receiver slips a bit

Sequence Count (each count is one REF clock cycle in duration)
Slips, in a Real Symbol Synchronizer

- Phase jitter trend measured during a slip on the I channel
- Transition time of the slip depends on the loop bandwidth, here it took 300 bits
• QPSK rotation by one quadrant (a 90° slip of the carrier tracking loop) causes channel swapping.

• Channel swapping means symbol synchronizer swapping.

• Due to symbol staggering, the symbol synchronizers are now integrating mid-bit to mid-bit.

• A half-bit slip one direction or the other must ensue to compensate.
Es/No Estimations

- Es/No from hard decision SER and inverse $Q()$ (practical meaning and highly stable)
- Es/No from fitted bell curve (high stability but assumes Gaussian noise)
- Es/No from mean and standard deviation of **correlated** soft decisions (direct compare for many SNR estimators)
- Es/No from median and long-tail standard deviation of **correlated** soft decisions (less influenced by clipping, and no distribution assumed)
Quantified Imbalances

• Not just one, but 8 histograms are run concurrently and then analyzed for:
  – Data Imbalance
  – Logic Threshold Imbalance
  – Channel Imbalance
  – Transition Density
  – choice of Inter-Symbol Interference (ISI) or Inter-Channel Interference
Actual Receiver Performance

- Probability of Error is much higher for bits sent as a “1” following a “0” – but only for one of the two channels.
Correlated Histograms and Anomalous Behavior

Most symbols have low amplitude, but most are correct. Why?

Uncorrelated

Underlying Phenomenon
Data Logging

• Continuous Historical Record
  – Slips, rotations
  – Long runs
  – External triggers

• Publish on Demand
  – Configuration
  – BER and Es/No measurements
  – User notes
Data Reinvestigation

- Average symbol amplitude data taken from SER curves, plotted as amplitude droop
Supporting Measurements

- Run Lengths ($2^{15}$-1 pattern shown here)
- Discrete Programmable Test Points
  - Slips, rotations, long runs, clock phase lock, correlator lock, copy of data or clock...
  - General purpose test points with selectable functionality
- Channel Simulator
Sweeping Degradation FromBaseline

Test Results, Constant Jitter

Revised Model Results, Constant Degradation

Performance with Jitter
Brand A, LBW=0.114%
SQPSK, 10% SER, 2Mfps

- slips
- no slips

- Phi=11.3% rms
- Phi=7.7% rms
- Phi=5.2% rms
- Phi=3.6% rms
- FJ=0.147% peak
- FJ=0.068% peak
- FJ=0.032% peak
- FJ=0.022% peak
- FJ=0.01% peak
- FJ=0.00681% peak
- CCI=1.4E^{-5}% rms
- CCI=9.6E^{-6}% rms
- CCI=6.5E^{-6}% rms
- CCI=4.4E^{-6}% rms

Figure 16. BER degradation surface plot as a function of peak jitter and jitter rate for $\zeta = 0.4$. 
Use-Case Example

Orion Transponder – Baseband Processor Integration