Single-Event Effect Response of a Commercial ReRAM

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Acronyms

- SEE – Single-event effect
- SEU – Single-event upset
- SEFI – Single-event functional interrupt
- RAM – Random access memory
- ROM – Read-only memory
- ReRAM – Reduction-oxidation random access memory
- 1T1R – 1 transistor 1 resistor
- LET – Linear energy transfer
- CMOS – Complimentary metal-oxide-semiconductor
Motivation

• Limited availability of radiation tolerant flash memories
• Radiation performance of state-of-the-art flash is generally good but include some weaknesses
• Flash already reaching scaling limits
• Resistive random access memory has shown very good tolerance to ionizing radiation*
• Currently available radiation test results only on test chips
• A first look at the SEE performance of a commercial production-level reduction-oxidation random access memory (ReRAM)


Device Details

Panasonic MN101L
- 16 bit microcontroller with embedded ReRAM
- Industry’s first mass production-level ReRAM
- 1T1R array architecture, with CMOS transistor as access transistor to each ReRAM stack
- TaO\textsubscript{x} as switching layer
- Minimum device width ~ 0.5 μm
- Fabricated back-end-of-line in a 180 nm CMOS process

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Size</td>
<td>64 KB</td>
</tr>
<tr>
<td>Program Endurance</td>
<td>Program area (62 KB): ( \geq 10^3 )</td>
</tr>
<tr>
<td></td>
<td>Data area (2 KB): ( \geq 10^5 )</td>
</tr>
<tr>
<td>Programming Voltage</td>
<td>1.8 to 3.6 V</td>
</tr>
<tr>
<td>Reading Voltage</td>
<td>1.1 to 3.6 V</td>
</tr>
<tr>
<td>Data Retention</td>
<td>10 years</td>
</tr>
</tbody>
</table>

Heavy Ion Testing

- Kovar lid collimator (254 µm) exposed ReRAM array and peripheral control circuits
- Used Panasonic’s evaluation card as test vehicle
- Read Only Memory (ROM) operating conditions: V<sub>cc</sub> = 3.3 V, Frequency = 8 MHz or DC
- Test modes: static, dynamic read, read/compare/write, and write
- Data patterns: 00, FF, 55, and AA
- 15 MeV/amu heavy ions at Texas A&M University
  - Ne, Ar, Kr, and Xe at normal, 30°, and 45°
  - Flux = 10<sup>3</sup> to 10<sup>4</sup> cm<sup>-2</sup>·s<sup>-1</sup>, fluence = 2 × 10<sup>6</sup> cm<sup>-2</sup> per shot
Heavy Ion Test Results

- Static tests did not result in SEU
  - 1 functional error following Xe irradiation, during read-back, recovered by a reset

- Dynamic read and write tests resulted in mostly SEFI
  - 1 event set device into locked mode
  - Reset for read mode SEFI
  - Reset or power cycle for write mode SEFI

- Similar SEFI cross sections for read and write test mode

- Angular irradiation
  - Cross section of normal incident degraded beam several factors higher than angular irradiation with same effective LET
  - Beam shadowing from the collimator
SEE Characteristics

- **Functional interrupts**
  - Most SEFIs did not result in large scale errors
  - Microcontroller stops reading/writing
  - 1 SEFI showed mass errors from the RAM

- **Bit upsets**
  - Included single-bit and multiple-bit upsets
  - Error address locations distributed throughout the microcontroller memory bank
  - 8 SEUs in the ROM
  - Could not rule out array errors

Pulsed-Laser Testing

- Pulsed-laser testing was carried out at the Naval Research Laboratory
- Laser characteristics
  - Wavelength = 590 nm
  - 1/e penetration range = 2 μm in silicon
  - Beam diameter = 1.7 μm for 20× lens, 0.9 μm for 100× lens
- We probed the ReRAM array and surrounding peripheral circuits with a 20× lens to identify the sensitive regions
- Sensitive areas were further investigated with a 100× lens, and the energy was fine-tuned to determine the upset energy threshold
- Equivalent LET values are based on empirical data from previous studies on other device types
Sensitive Locations

- Bit upsets
  - Did not originate from the ReRAM array
  - Location sensitive to SEUs also susceptible to SEFI

- Functional interrupt
  - Stops reading/writing
  - Continuously reading out errors from the ROM
  - Stuck reading at end of Bank0 (FFFF)
  - Continuously reading errors from other address locations beside the ROM
Upset Sensitivity in the Most Sensitive Location

- SEFI energy threshold
- Location 1:
  - Read mode: 5.5 pJ (17 MeV·cm²/mg)
  - Write mode: 8.6 pJ (26.5 MeV·cm²/mg)
- Location 2:
  - Read mode: 71 pJ (220 MeV·cm²/mg)
- Location 3:
  - Read mode: 105 pJ (320 MeV·cm²/mg)
SEE Characteristics

- Compare SEE from location 1 with heavy ion results
- Memory address of errors from laser test are similar to those from heavy ion test
- SEFI modes from laser and heavy ion test are also similar
  - Although limited information was gained from SEFIs that caused immediate cease of operation
- Sensitive region consists of sense amplifier circuit
  - Similar characteristics to SEFI caused by SEU from sensing circuit in flash*

SF Register – Special function register
IO Register – Input/Output register

Conclusion

- ReRAM array is hardened against heavy ions with LET as high as 70 MeV·cm²/mg
  - SEU in CMOS access transistor not enough to cause bit flip

- SEFI is the dominant error mode
  - Sensitivity of peripheral circuits critical to SEE response of ReRAM
  - Sense amplifier vulnerable to upsets leading to SEFI

- Lack of charge pump reduces sensitivity to radiation-induced erase/program failure
  - Eliminates block erase failures (issue for flash)