



Single Event Gate Rupture Characterization of the Fuji MOSFETs: 2SJ1A03 (A08P10), 2SJ1A09 (A08P20), and NSD1A01

Leif Scheick
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 14-6 01/14



Single-event Gate Rupture Characterization of the Fuji MOSFETs: 2SJ1A03 (A08P10), 2SJ1A09 (A08P20), and NSD1A01

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Leif Scheick
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 939904.01.11.30
JPL Project Number: 102197
Task Number: 3.23.5

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

<http://nepp.nasa.gov>

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

©2014 California Institute of Technology. Government sponsorship acknowledged.

TABLE OF CONTENTS

1.0 Purpose.....	1
2.0 Test Samples	2
3.0 General	3
4.0 Electrical Tests.....	4
5.0 Failure Criteria.....	24
6.0 Schedule	25
7.0 Bias Condition/Fixtures	26
7.1 Setup.....	26
8.0 Procedure	27
9.0 Results	28
10.0 Conclusion and Recommendation	36

1.0 PURPOSE

This testing is to characterize the power MOSFETs listed in Table 1.0-1 for single-event gate rupture (SEGR) and single-event burnout (SEB) response. Test results were compared against comparable voltage rated devices.

Table 1.0-1. List of power MOSFET devices that will be tested for SEE characterization.

Manufacturer	Part Number	Voltage rating (V)	Channel	Number provided	Package
FUJI	2SJ1A03 (11P10)	-100	P	50	TO-254
FUJI	2SJ1A09 (08P20)	-200	P	50	TO-254
FUJI	NSD1A01	600	N	50	24 DIP

2.0 TEST SAMPLES

The test samples are outlined in Table 1.0-1. Parts were handled in accordance with all ESD precautions. All parts had the following parameters measure before SEE testing: transconductance, voltage threshold, gate leakage. The following stress tests were applied to all devices: full off gate bias and 80% drain bias. All devices passed these tests and were approved for testing. Table 2.0-1 lists the steps required in preparing and vetting the parts in this test.

Table 2.0-1. List of power MOSFET devices that will be tested for SEE characterization.

Step	Part Numbers	Action	ATE	Serial Number and Calibration end date	Compliance
Check in	All	Verify part number, visually inspect for damage and assign SEE test serial number	NA	NA	Yes
Initial parametric test	All	Measure gm, Vth and Igss @ ± 20 V	HP4156		Yes
Initial stress test	All	Apply absolute maximum Vgs (off) and absolute maximum Vds	HP4142		Yes
De-lid and die photo	All	De-lid and die photo	NA	NA	Yes

3.0 GENERAL

Eighteen (18) of the fifty (50) available NSD1A01 have been tested. Thirty six (36) of the fifty (50) available 2SJ1A09 have been tested. Twenty four (24) of the fifty (50) available 2SJ1A03 have been tested. Parts were tested at Brookhaven National Laboratory (BNL) and the Texas A&M University Radiation Effect Facility (TAMU-REF). See Table 3.0-1 for a list of tested parts and ions.

Table 3.0-1. Selected ion beam energy (15 MeV/amu).

Group	Qty	Part Number	Gate to Source Bias [V]	Site	Surface LET [MeV mg/cm ²]	Ion-Energy [MeV]	Ion (range in Si [μm])
A1	6	2SJ1A03	Vgs= 0, 5, 10, 15, 20	TAM	36	Kr-300	60
A2	6	2SJ1A03	Vgs= 0, 5, 10, 15	BNL	36.1	Br-279	37.45
A3	6	2SJ1A03	Vgs= 0, 5, 10, 15, 20	TAM	61	Xe-648	52.3
A4	6	2SJ1A03	Vgs= 0, 5, 10, 15, 20	TAM	27.1	Kr-1097	144.2
A5	6	2SJ1A03	Vgs= 0, 5, 10, 15, 20	TAM	50.2	Xe-1632	129
B1	6	2SJ1A09	Vgs= 0, 5, 10, 15	TAM	94.4	Au-1768	88.1
B2	6	2SJ1A09	Vgs= 0, 5, 10, 15	TAM	31.5	Xe-333	63.4
B3	6	2SJ1A09	Vgs= 0, 5, 10, 15	TAM	50.9	Xe-1569	124.5
B4	6	2SJ1A09	Vgs= 0, 5, 10, 15	TAM	36	Kr-300	60
B4	6	2SJ1A09	Vgs= 0, 5, 10, 15	BNL	36.1	Br-279	37.45
B5	6	2SJ1A09	Vgs= 0, 5, 10, 15	TAM	27.1	Kr-1097	144.2
C1	3	NSD1A01	Vgs= 0, -5	TAM	84.7	Au-2342	123
C2	3	NSD1A01	Vgs= 0, -5	TAM	94.4	Au-1768	88.1
C3	6	NSD1A01	Vgs= 0, -5, -10, -15	TAM	50.9	Xe-1569	124.5
C4	3	NSD1A01	Vgs= 0, -5, -10	TAM	34.8	Kr-533	64.6
C5	3	NSD1A01	Vgs= 0, -5, -10	TAM	31	Kr-733	96.1
C6	3	NSD1A01	Vgs= 0, -5, -10	TAM	50.2	Xe-1632	129

4.0 ELECTRICAL TESTS

Electrical tests were performed in accordance with “The Test Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs” [JPL Publication 08-10 2/08]. The threshold voltage (V_{th}) and transconductance (g_m) were measured on all parts prior to irradiation. All parts were in specification. However, the 2SJ1A03 (A08P10) exhibited forward breakdown when the full off-gate-to-source bias (V_{gs-off}) and full drain-to-source bias (V_{ds}) were simultaneously applied to these devices. Figure 4.0-1 through Figure 4.0-38 present the effect. This phenomenon prevented the post irradiation test of simultaneous full gate and drain stress, which altered the failure criteria in section 5.0. However, this condition did not prevent the biasing conditions required for SEE testing.

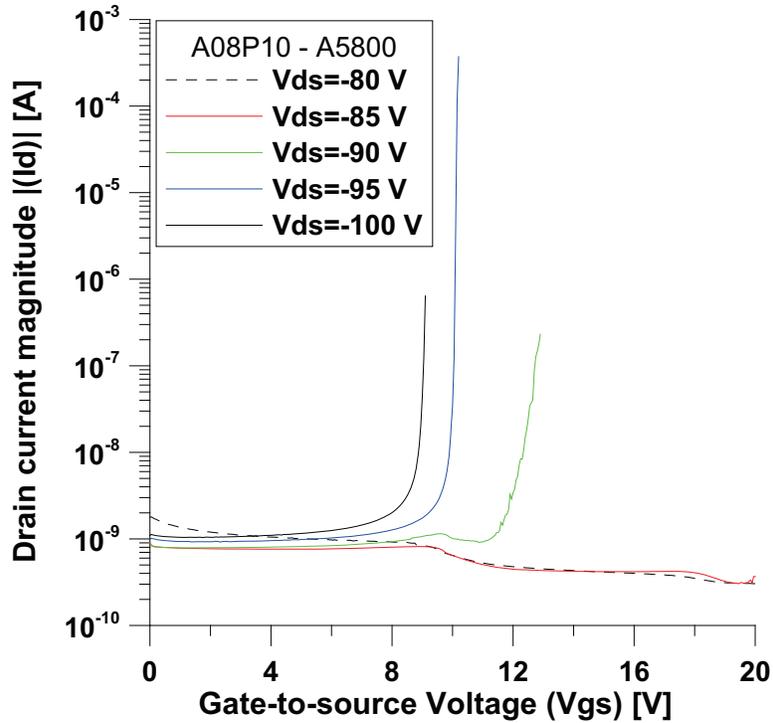


Figure 4.0-1

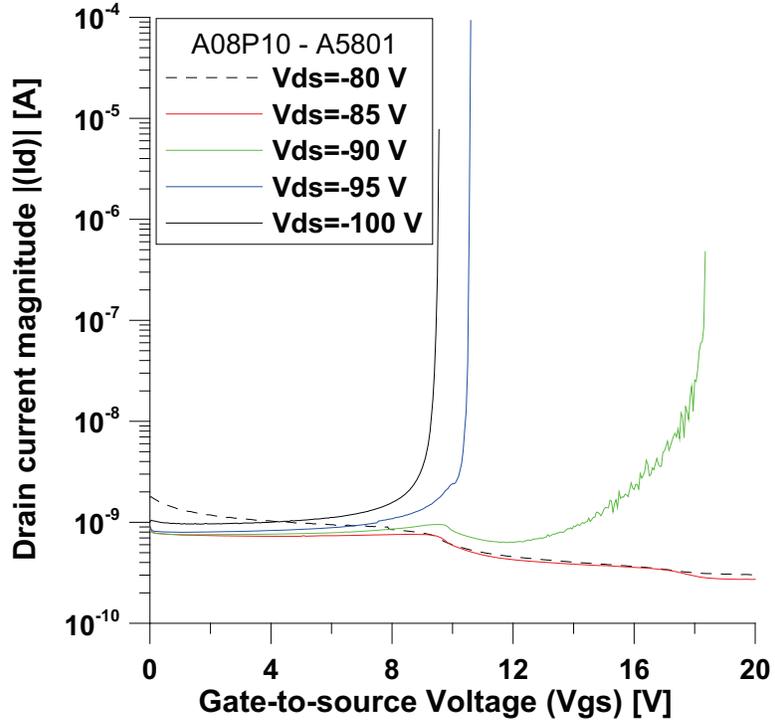


Figure 4.0-2

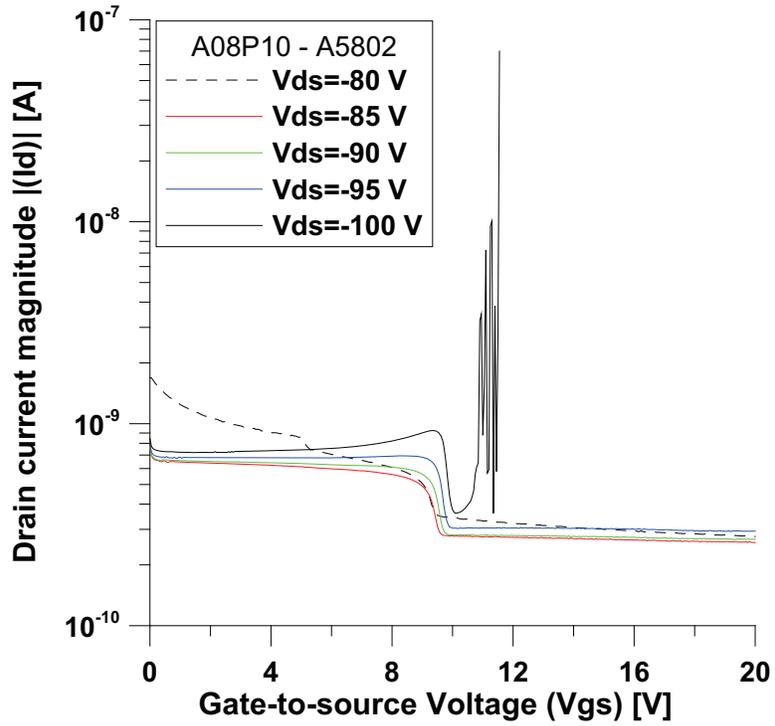


Figure 4.0-3

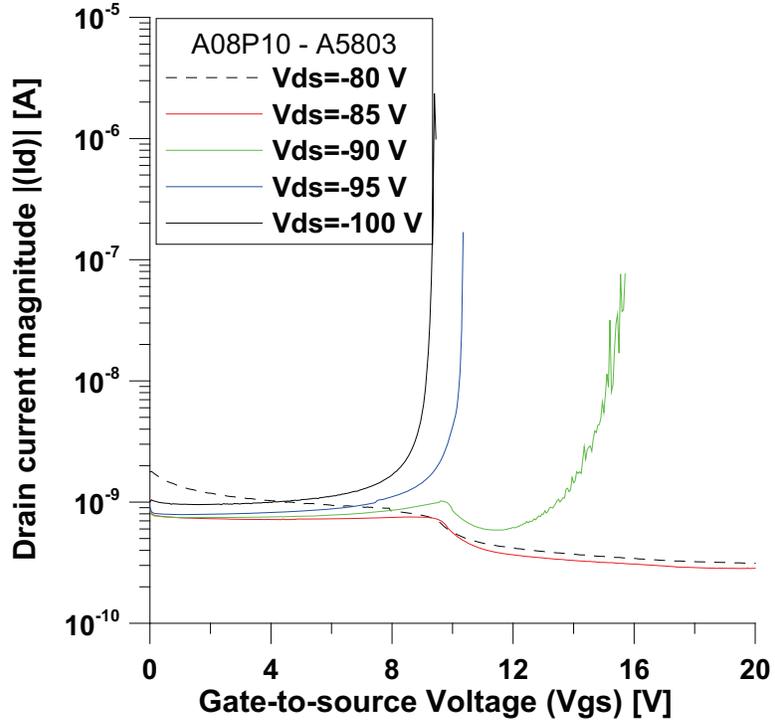


Figure 4.0-4

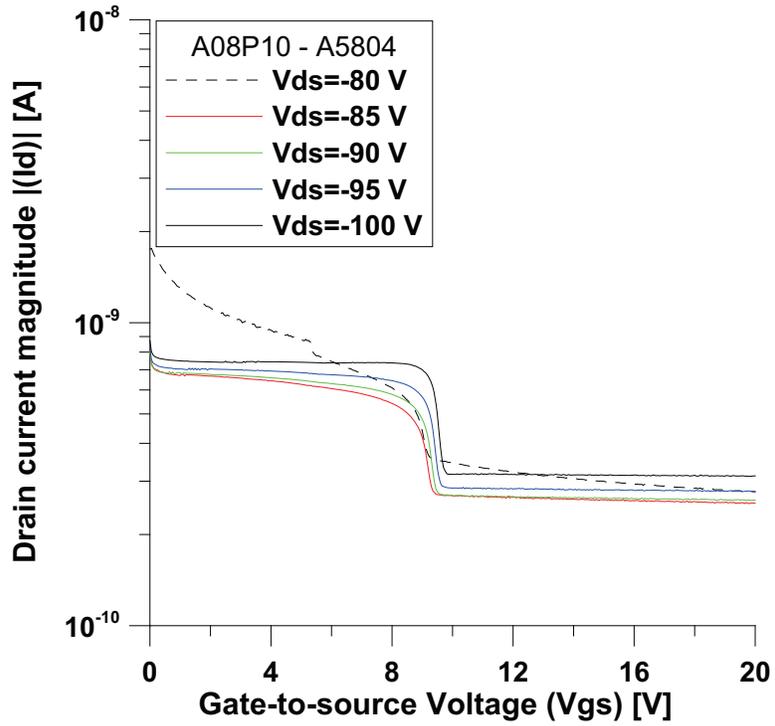


Figure 4.0-5

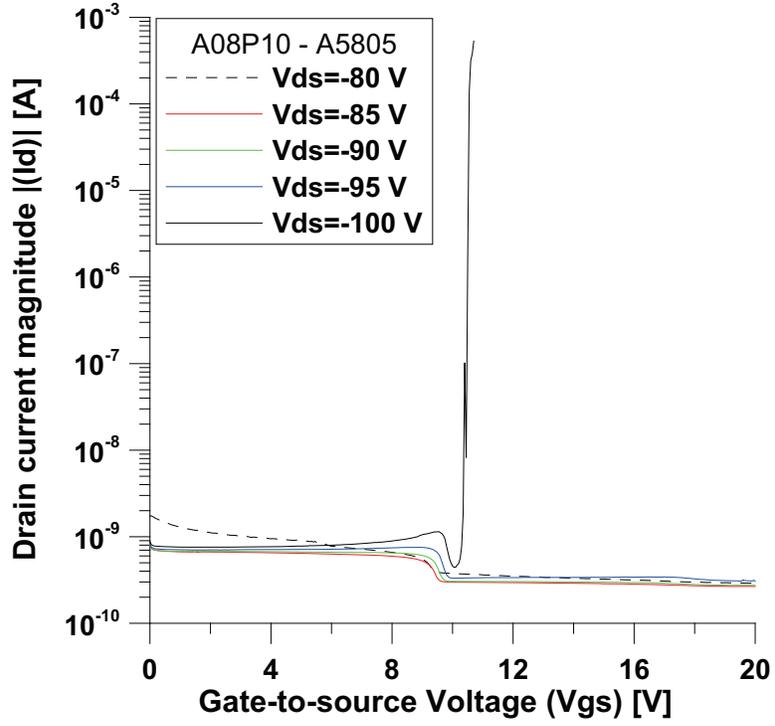


Figure 4.0-6

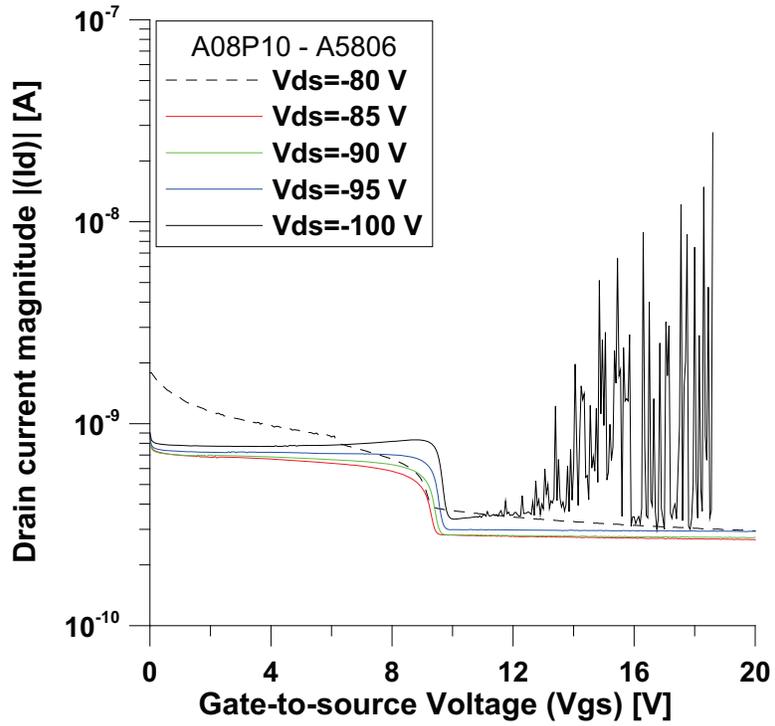


Figure 4.0-7

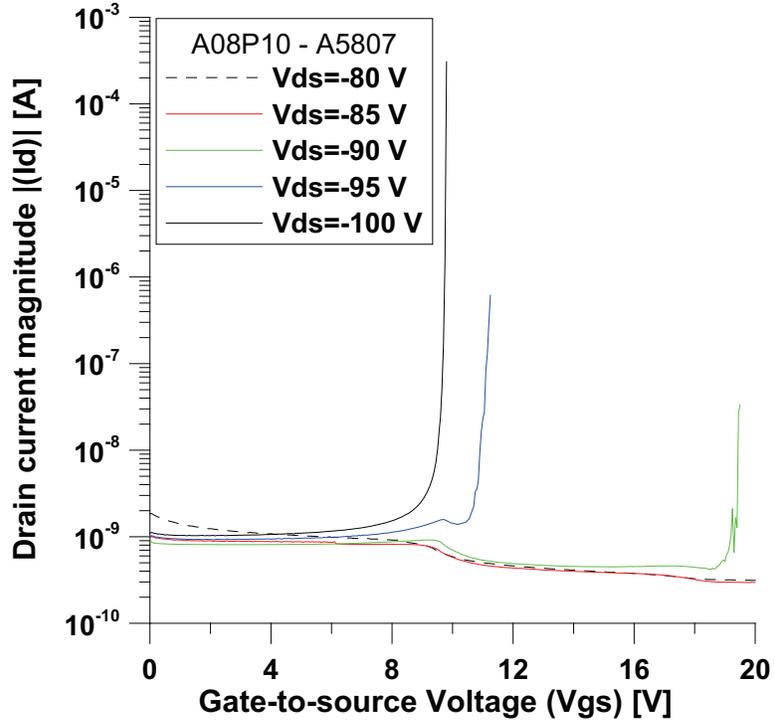


Figure 4.0-8

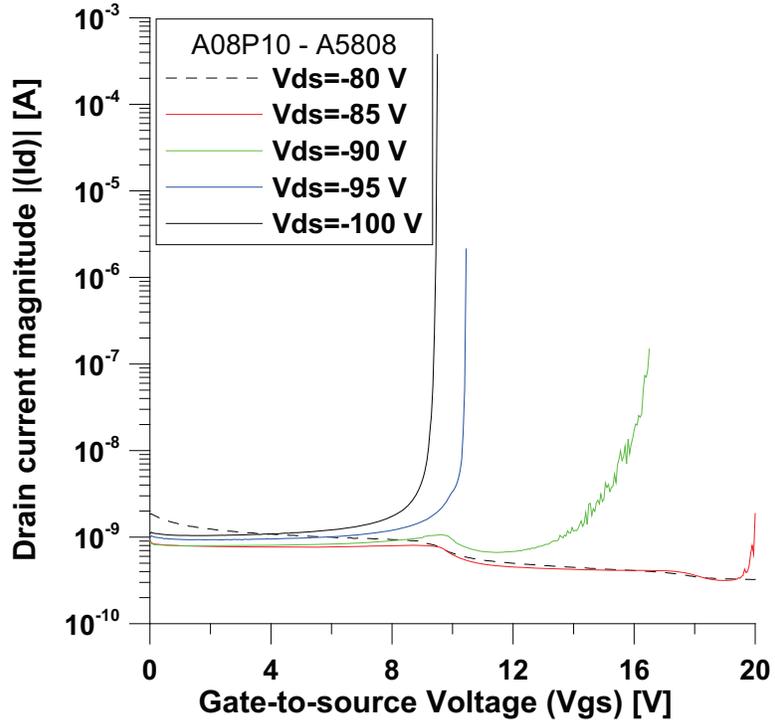


Figure 4.0-9

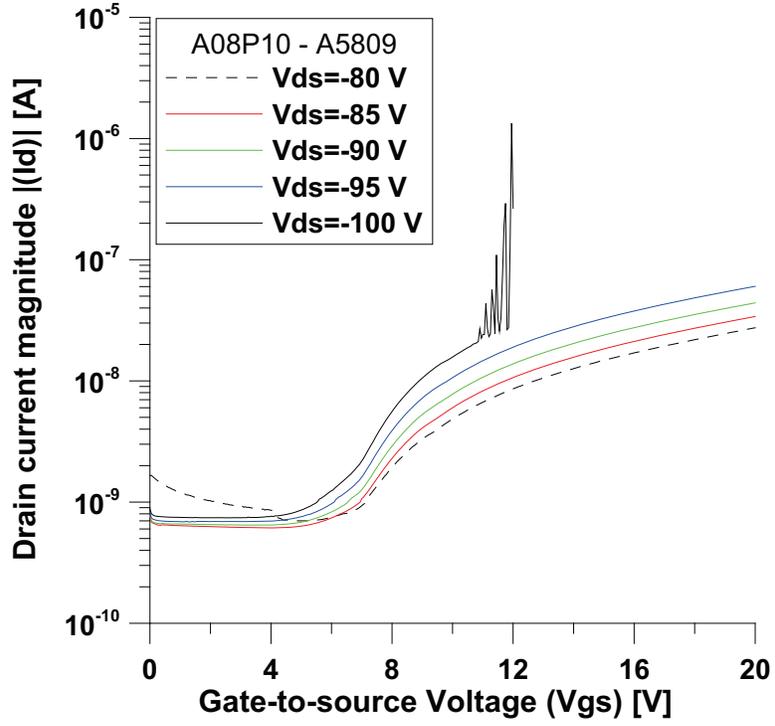


Figure 4.0-10

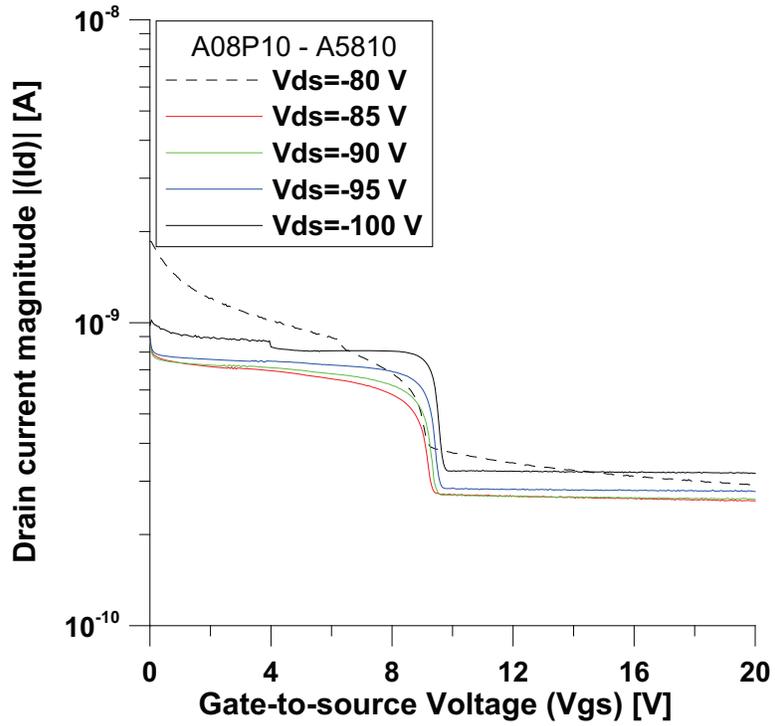


Figure 4.0-11

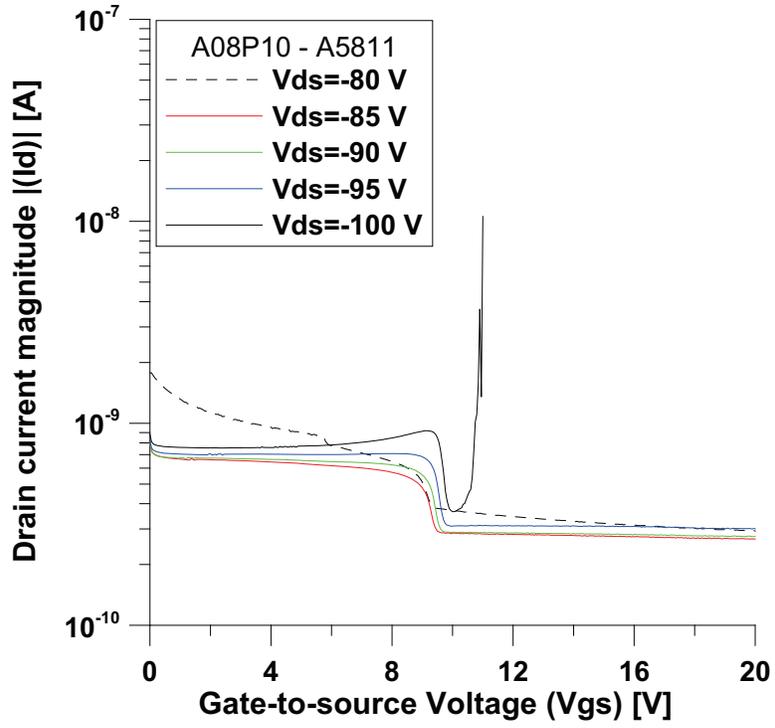


Figure 4.0-12

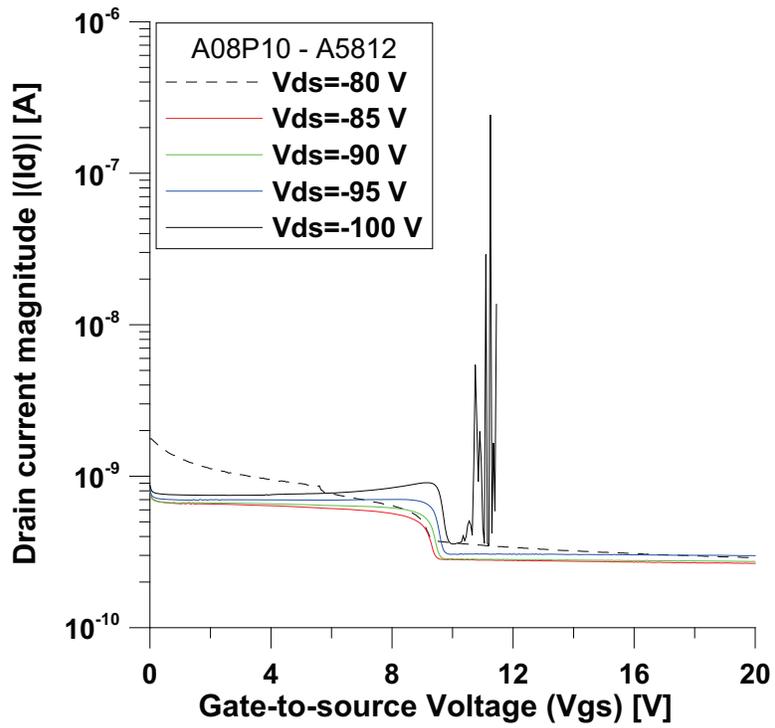


Figure 4.0-13

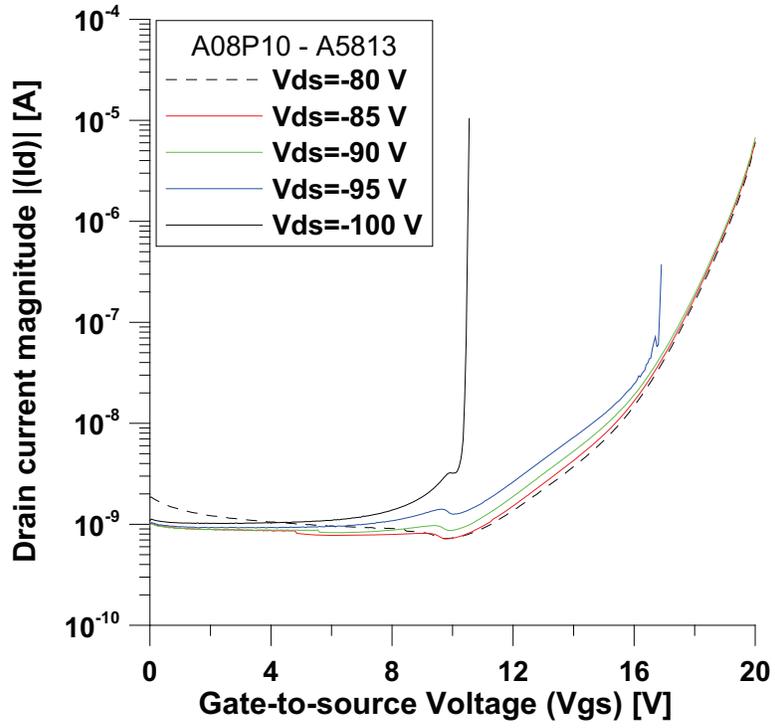


Figure 4.0-14

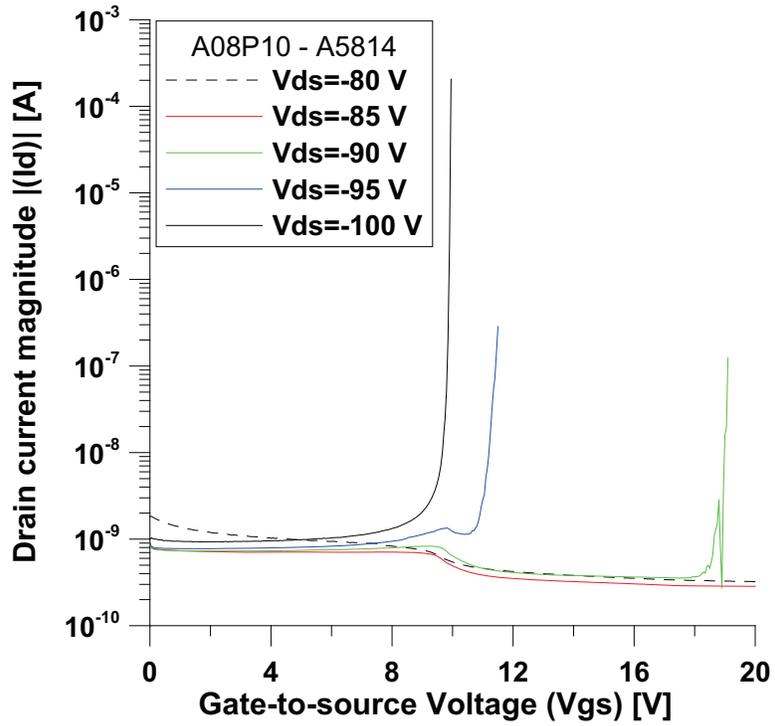


Figure 4.0-15

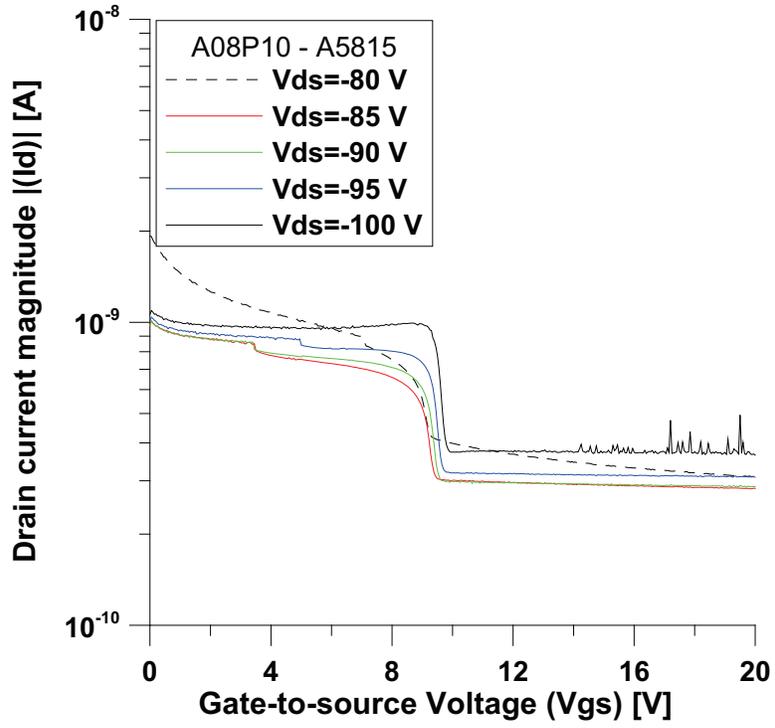


Figure 4.0-16

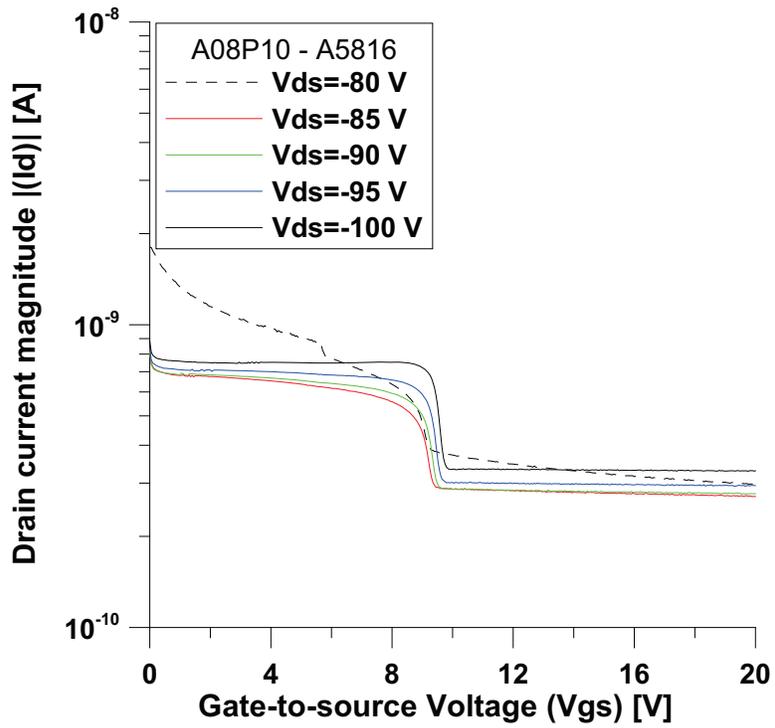


Figure 4.0-17

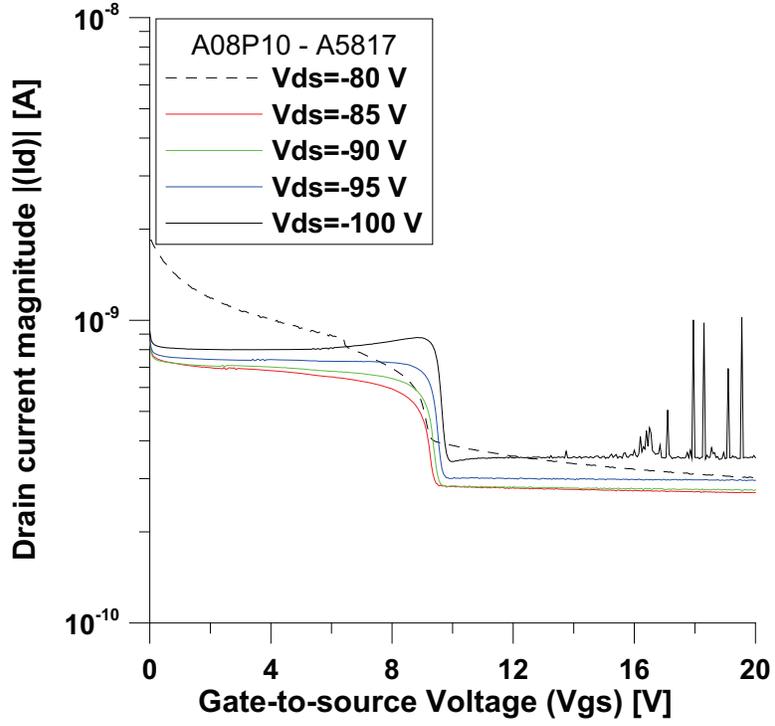


Figure 4.0-18

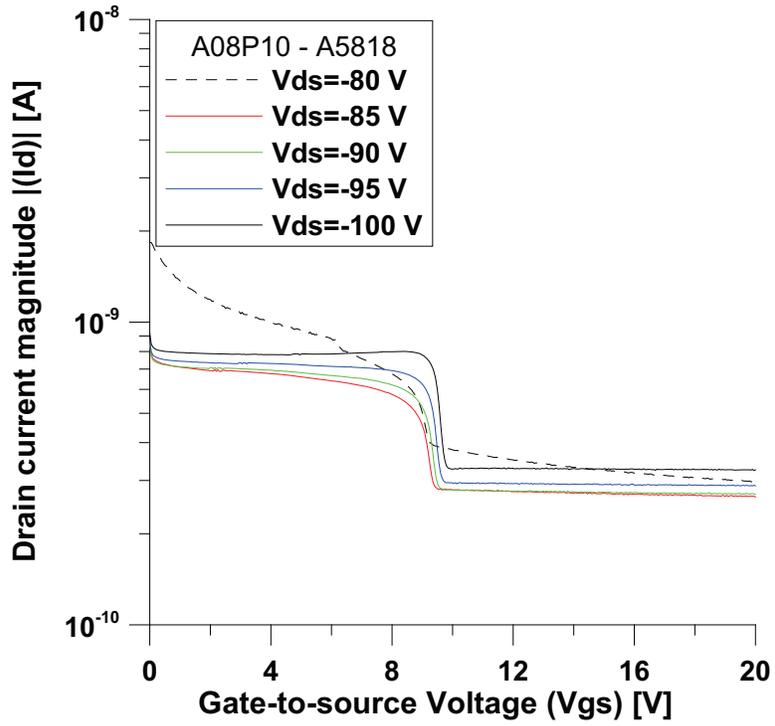


Figure 4.0-19

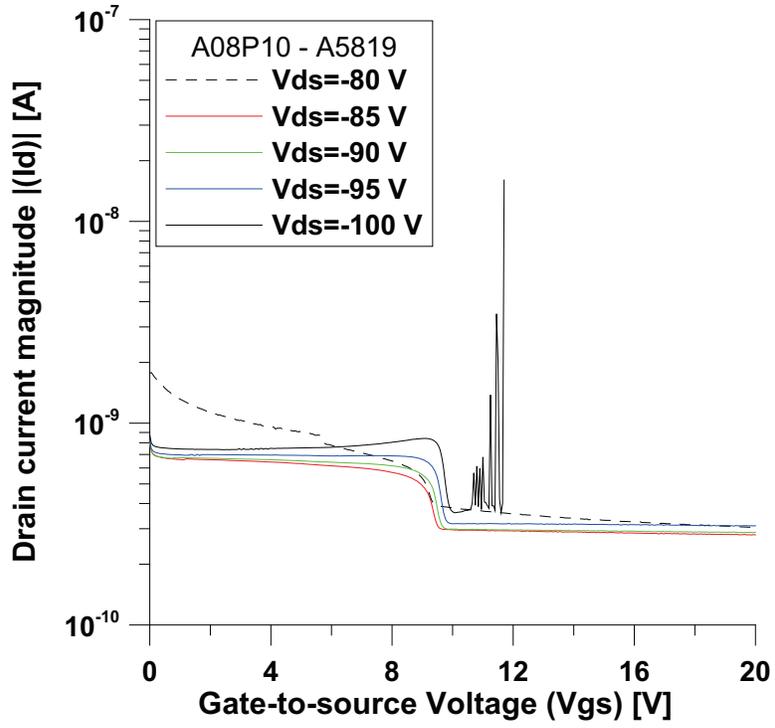


Figure 4.0-20

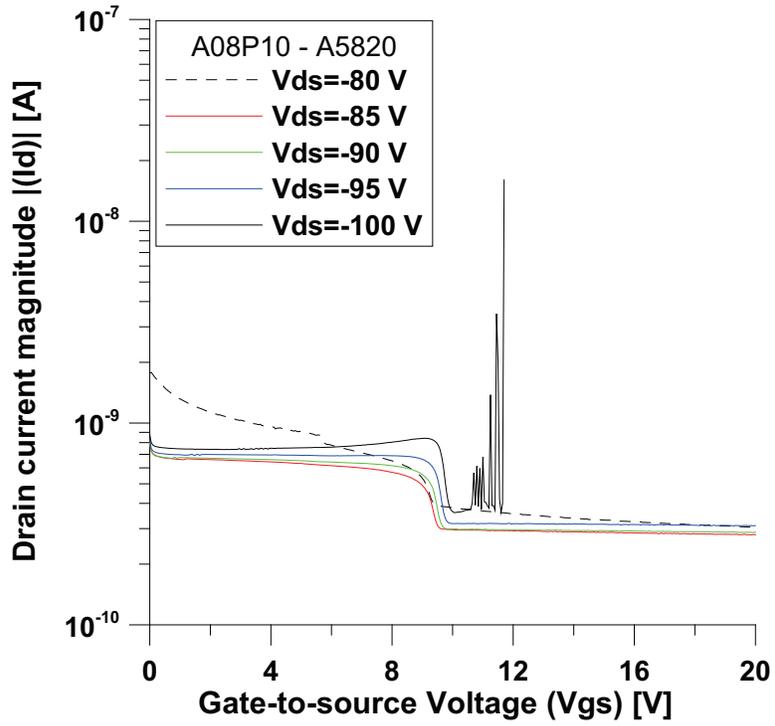


Figure 4.0-21

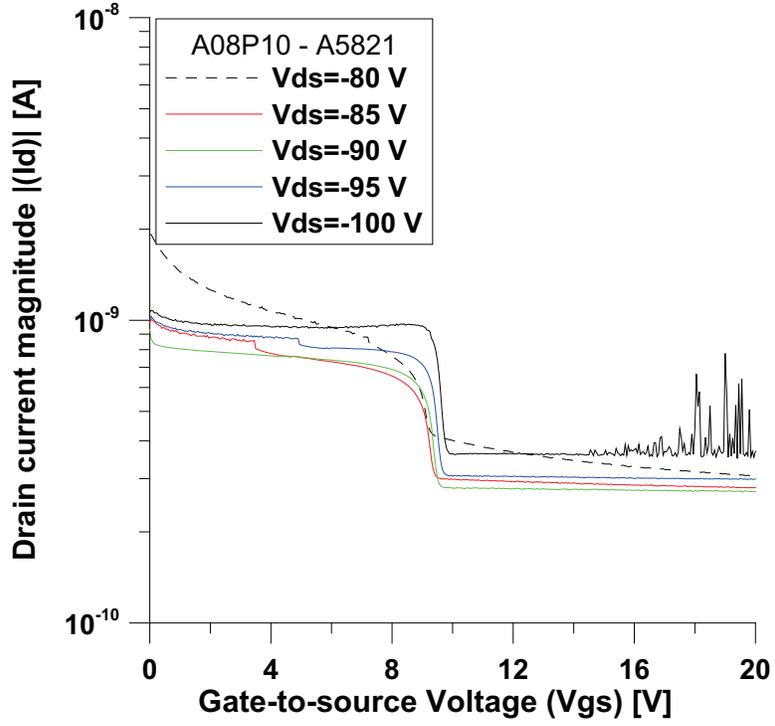


Figure 4.0-22

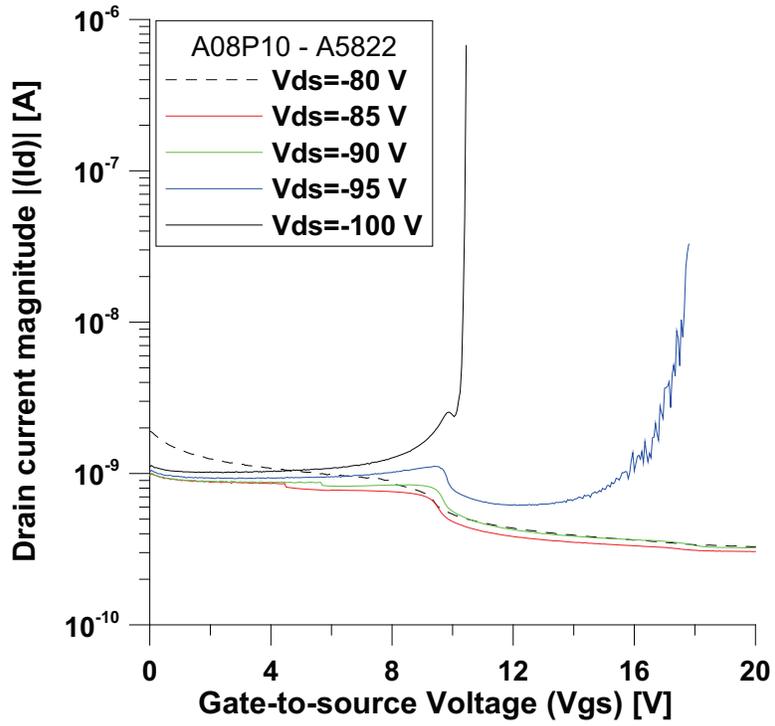


Figure 4.0-23

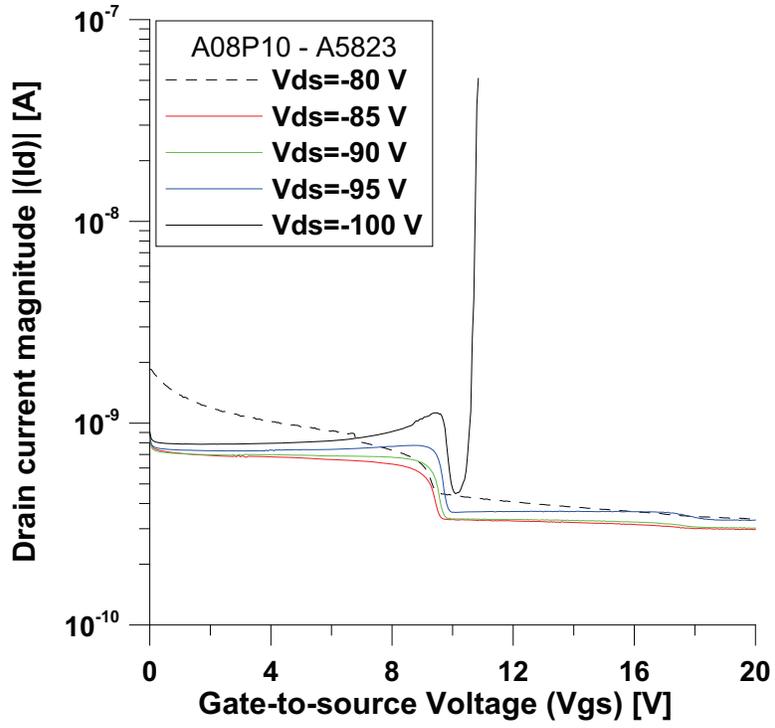


Figure 4.0-24

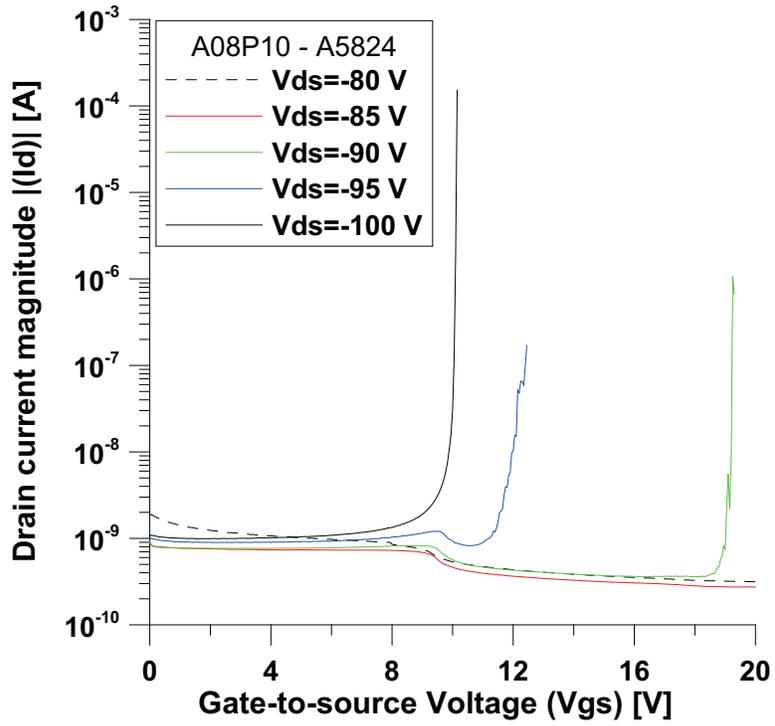


Figure 4.0-25

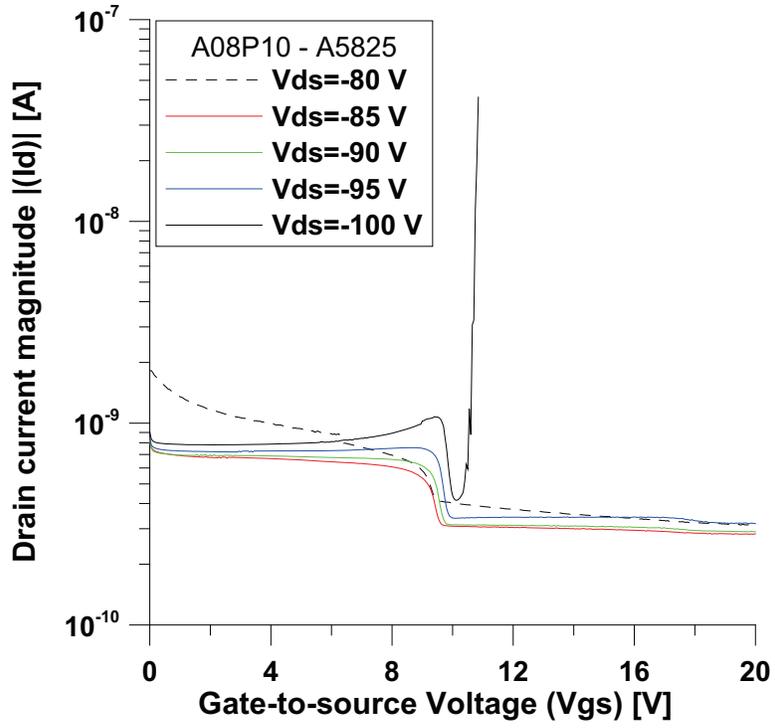


Figure 4.0-26

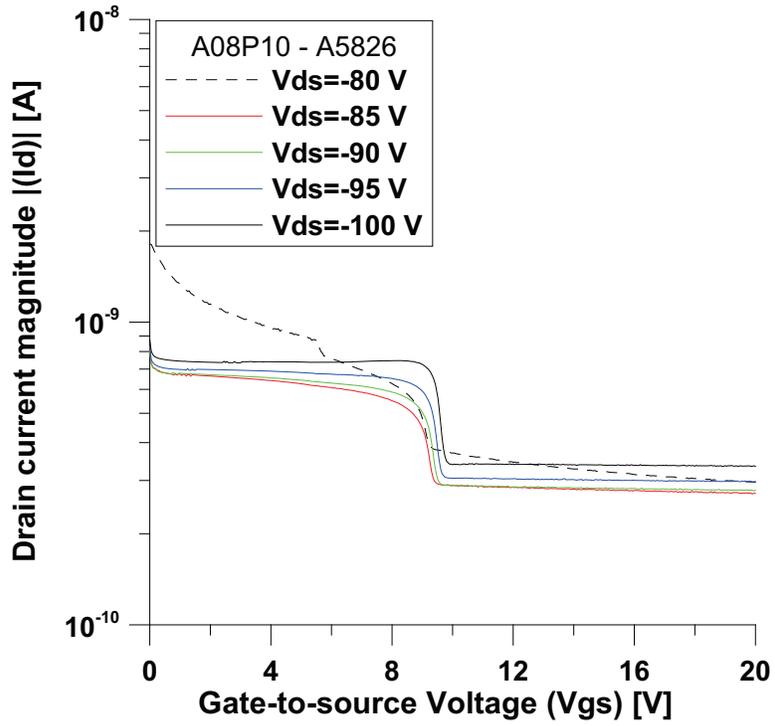


Figure 4.0-27

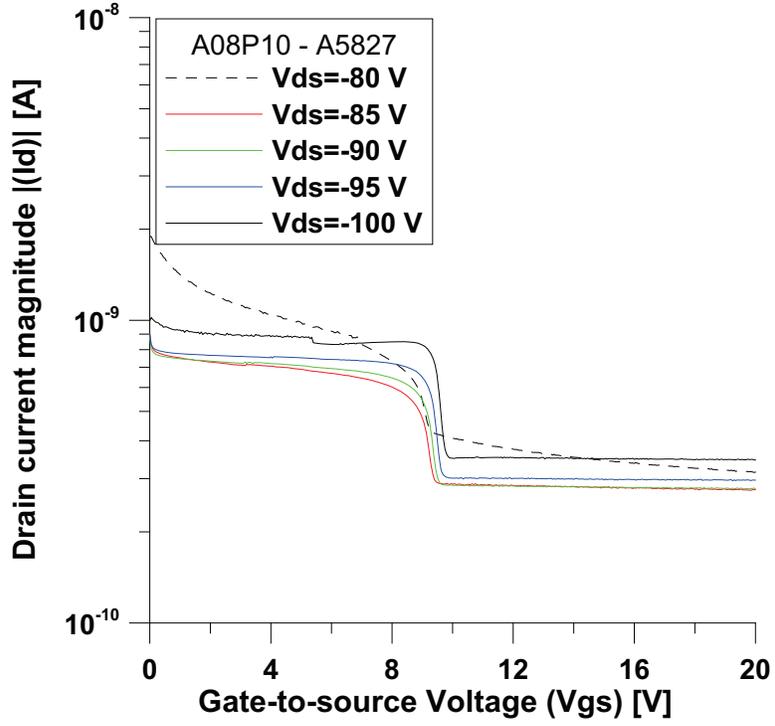


Figure 4.0-28

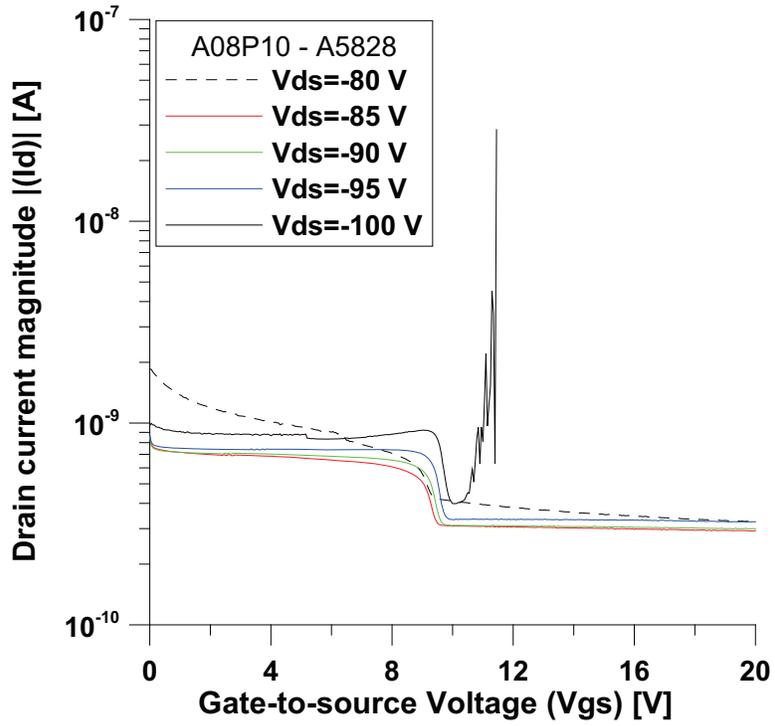


Figure 4.0-29

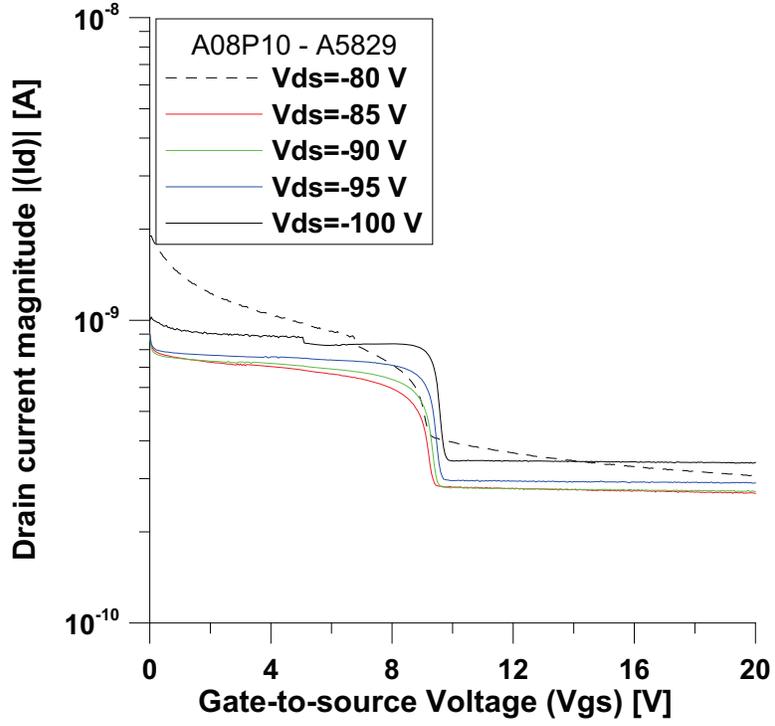


Figure 4.0-30

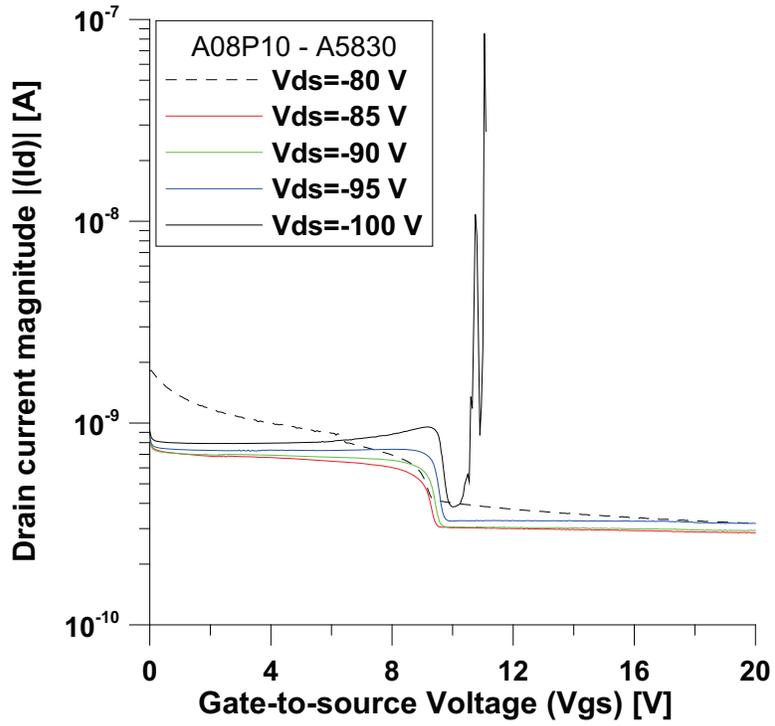


Figure 4.0-31

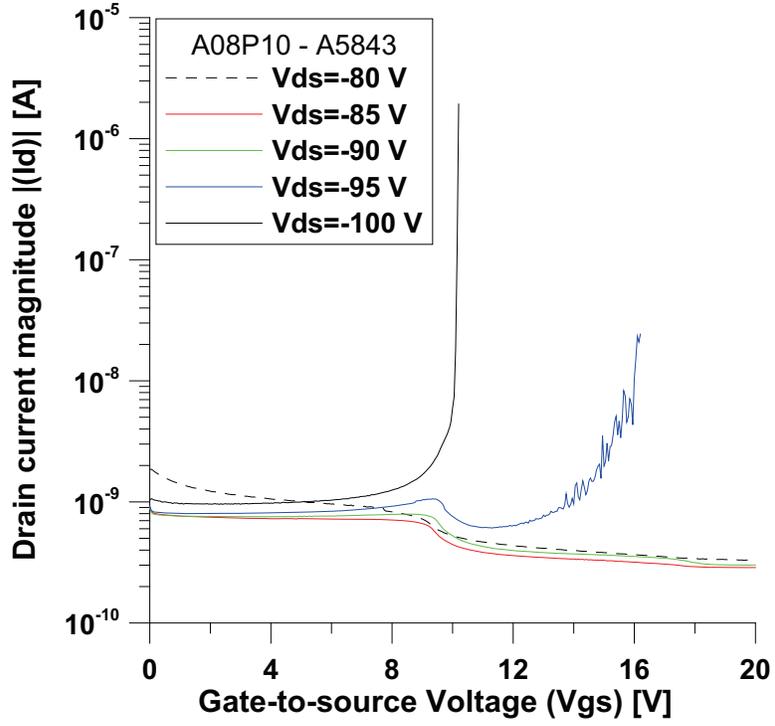


Figure 4.0-32

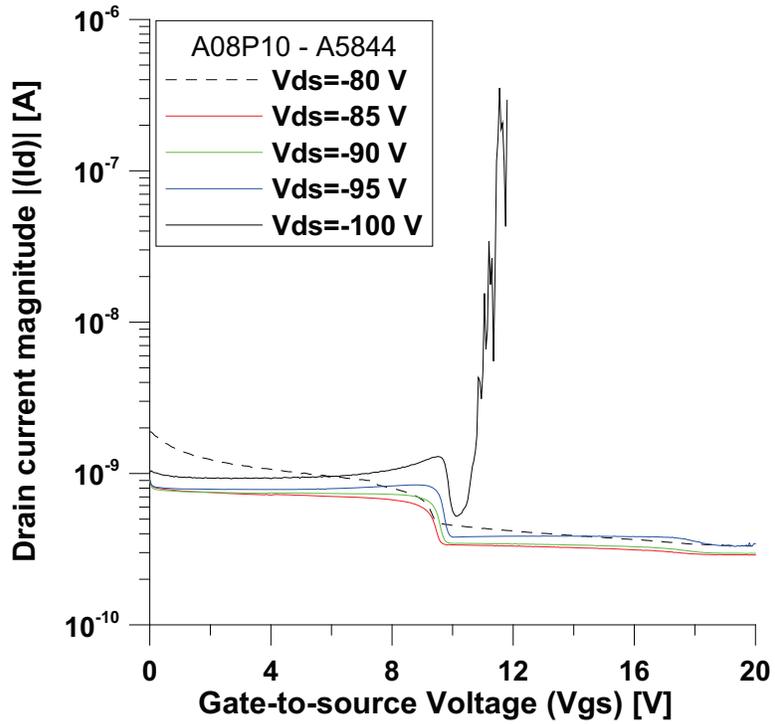


Figure 4.0-33

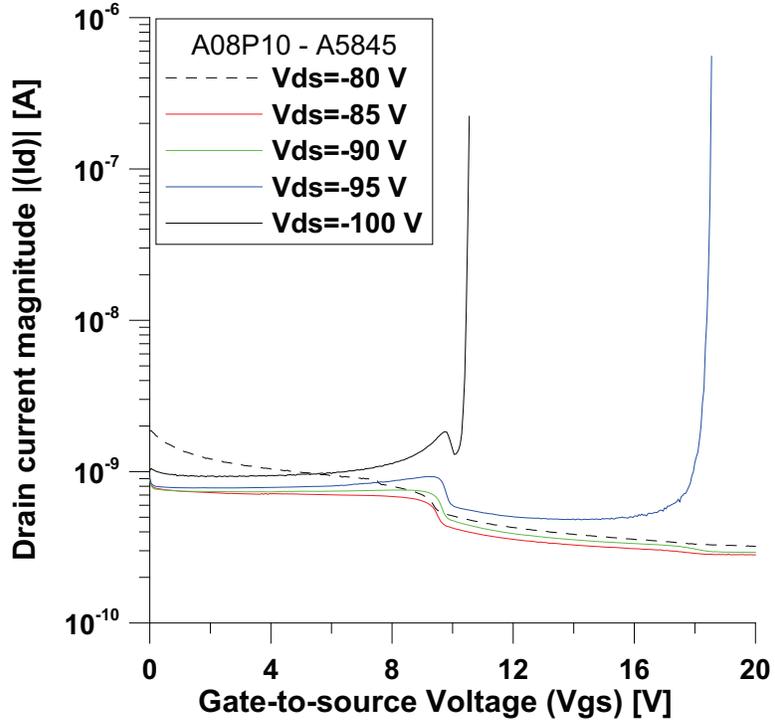


Figure 4.0-34

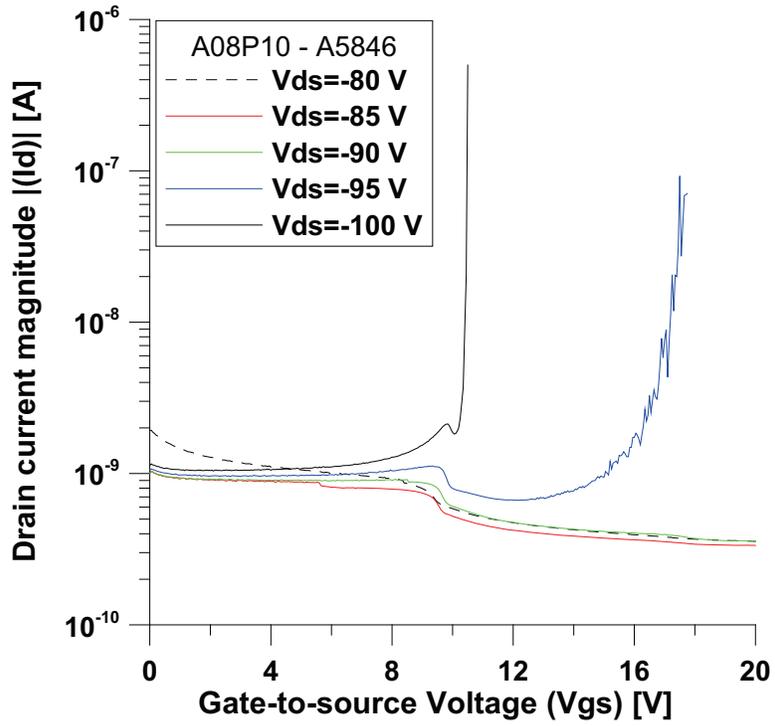


Figure 4.0-35

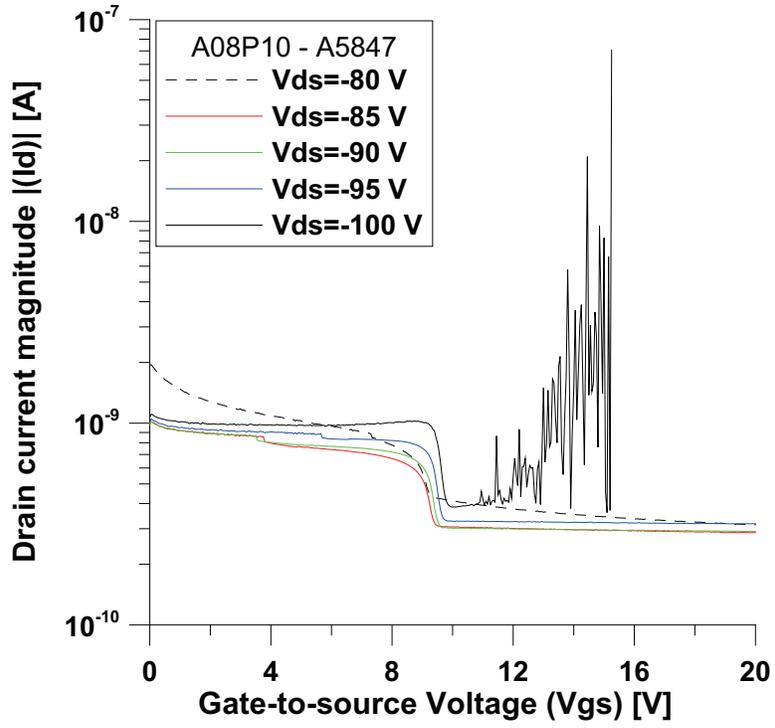


Figure 4.0-36

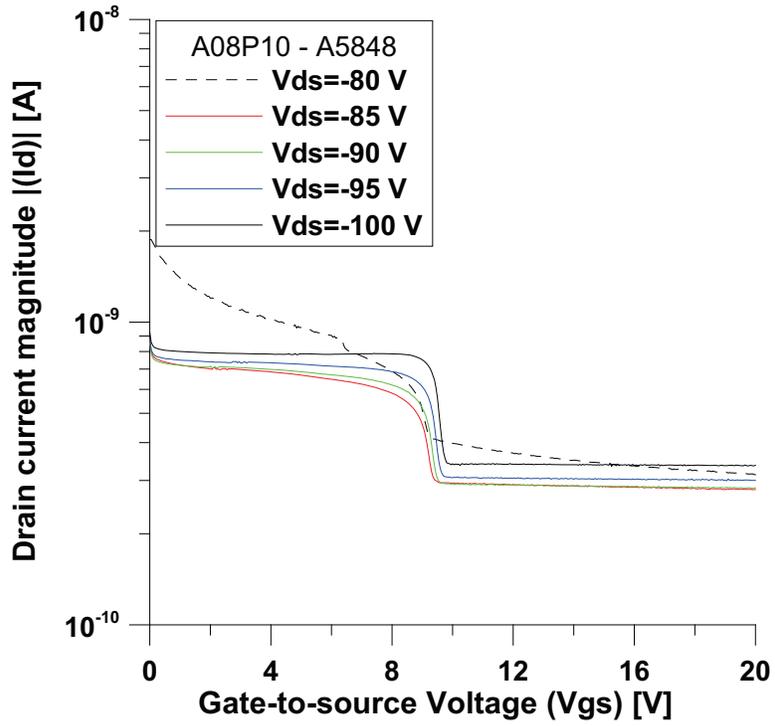


Figure 4.0-37

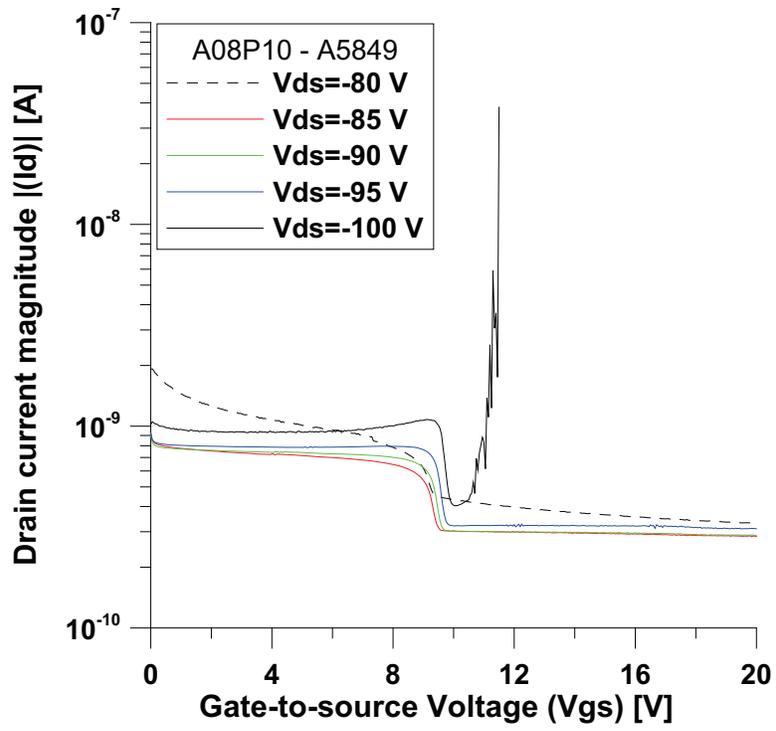


Figure 4.0-38

5.0 FAILURE CRITERIA

Failure criteria shall be classified in accordance with “The Test Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs” [JPL Publication 08-10 2/08]. Due to the 2SJ1A03 (A08P10) not being able to support full off-gate and drain bias, the post irradiation stress test (PIST) was a gate stress of -20 V followed by an application 80% of drain bias for 3 seconds. Out of specification reading during irradiation or either stress test was considered an SEE caused failure.

6.0 SCHEDULE

These tests occurred on February 22, 2012 at BNL and March.23, 2012 at TAM.

7.0 BIAS CONDITION/FIXTURES

Bias condition during the biased irradiations shall be in accordance with “The Test Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs” [JPL Publication 08-10 2/08]. Unbiased parts shall be exposed in a manner that protects them against ESD.

7.1 Setup

Failure criteria were classified in accordance with “The Test Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs” [JPL Publication 08-10 2/08]. Figure 7.1-1 shows the setup used in this experiment. An HP4142 forced the voltage and read a current with three independent SMUs. The background current on the board with no DUT was recorded to be ~ 0.5 nA in each device location. All parts were tested at ambient laboratory temperatures.

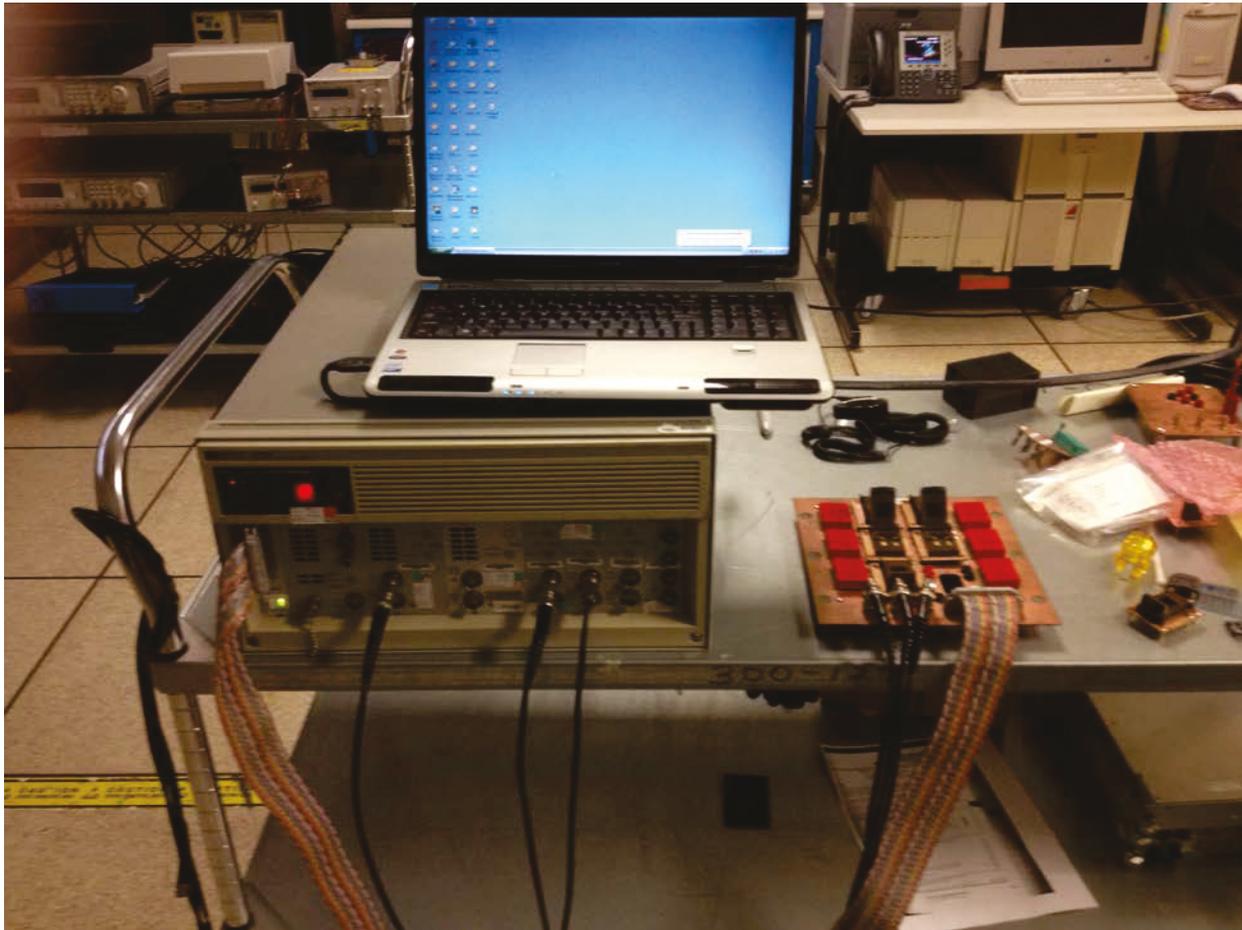


Figure 7.1-1. Setup used for SEE testing. Entire system is transported to heavy ion site

8.0 PROCEDURE

General test procedure shall adhere to the “The Test Guideline for Single Event Gate Rupture (SEGR) of Power MOSFETs” [JPL Publication 08-10 2/08]. Parts shall be serialized (if not already done), with controls marked prominently to distinguish them from test samples. Exposures shall be performed at ambient laboratory temperature.

9.0 RESULTS

All of the tests proceeded without anomaly. No latent damage or small breaks were seen, but a majority of the device failures during the post irradiation stress tests, and not during beam irradiation.

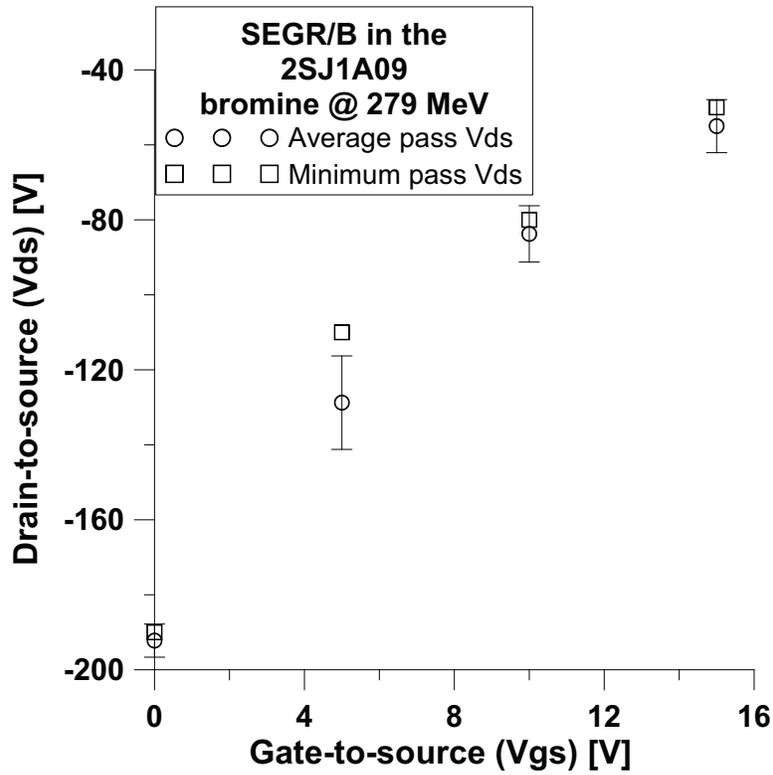


Figure 9.0-1. SEE test results of the 200 V Fuji p-channel with Br-279 at BNL. These data are comparable to results from similar ions at TAM (cf. Figure 9.0-2)

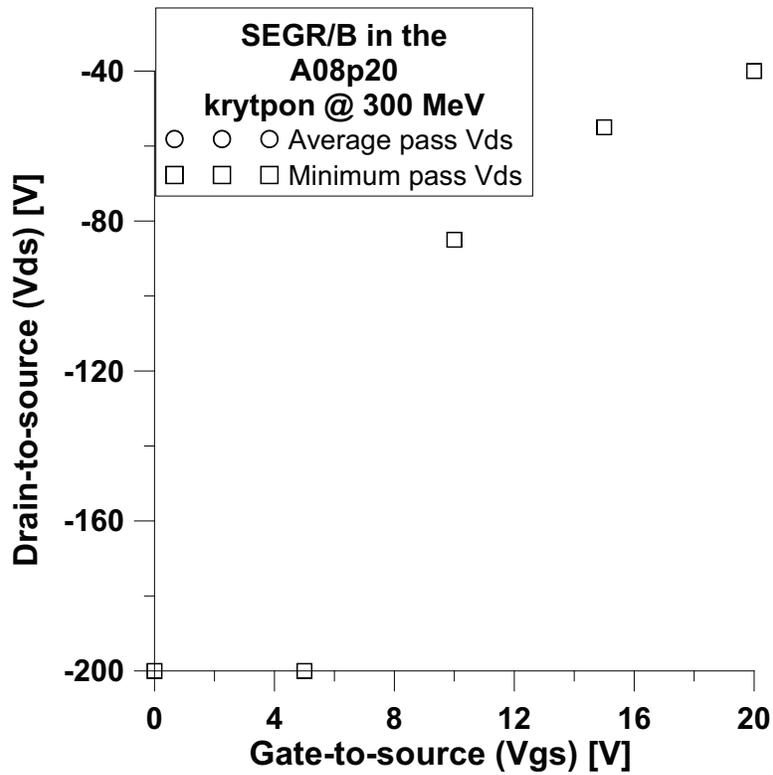


Figure 9.0-2. SEE test results of the 200 V Fuji p-channel with Kr-300 at TAM. These data are comparable to results from similar ions at BNL (cf. Figure 9.0-1). Note that at Vgs=-5 V, no SEE occurred and this effect is under investigation.

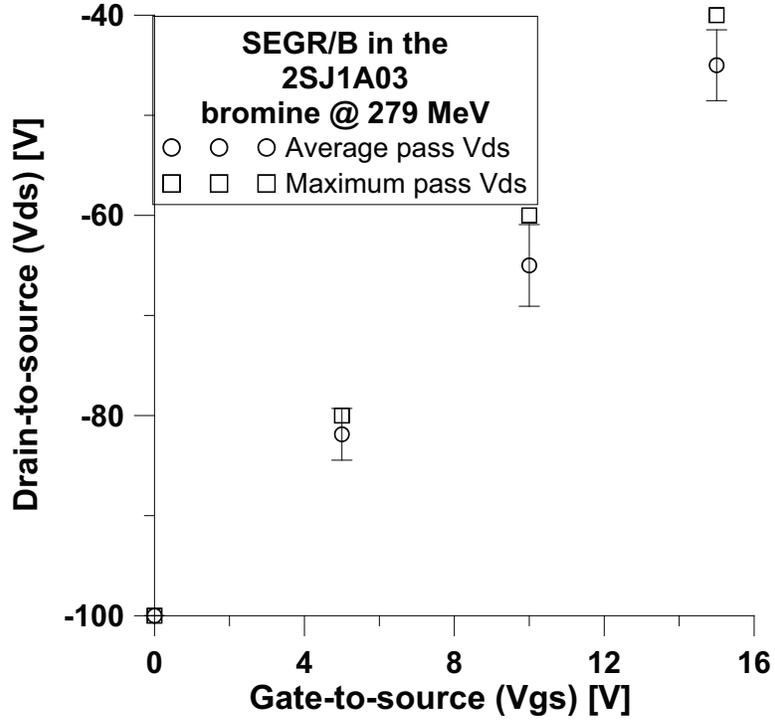


Figure 9.0-3. SEE test results of the 100 V Fuji p-channel with Br-279 at BNL. These data are comparable to results from similar ions at TAM (cf. Figure 9.0-4)

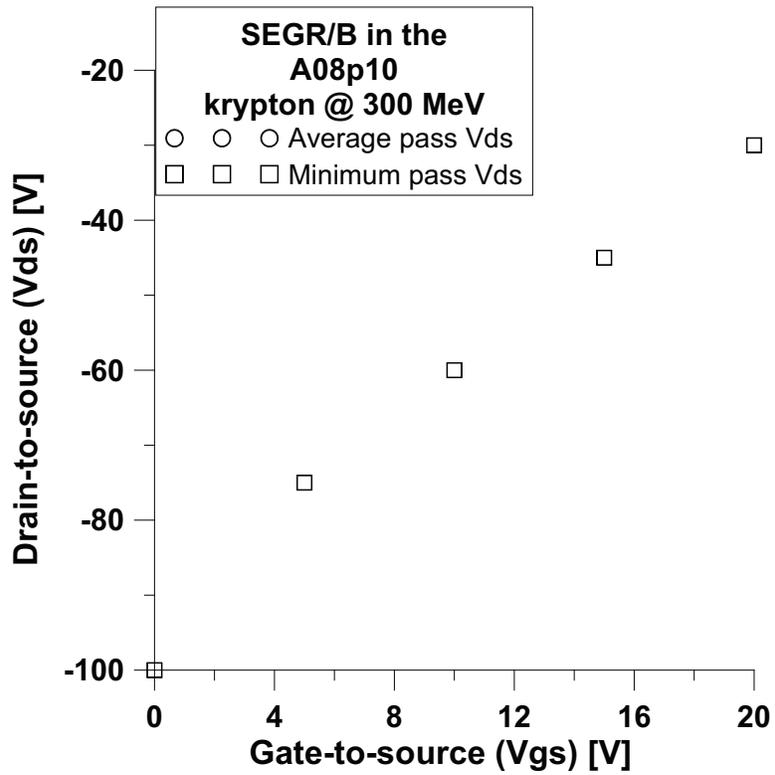


Figure 9.0-4. SEE test results of the 100 V Fuji p-channel with Kr-300 at TAM. These data are comparable to results from similar ions at BNL (cf. Figure 9.0-3).

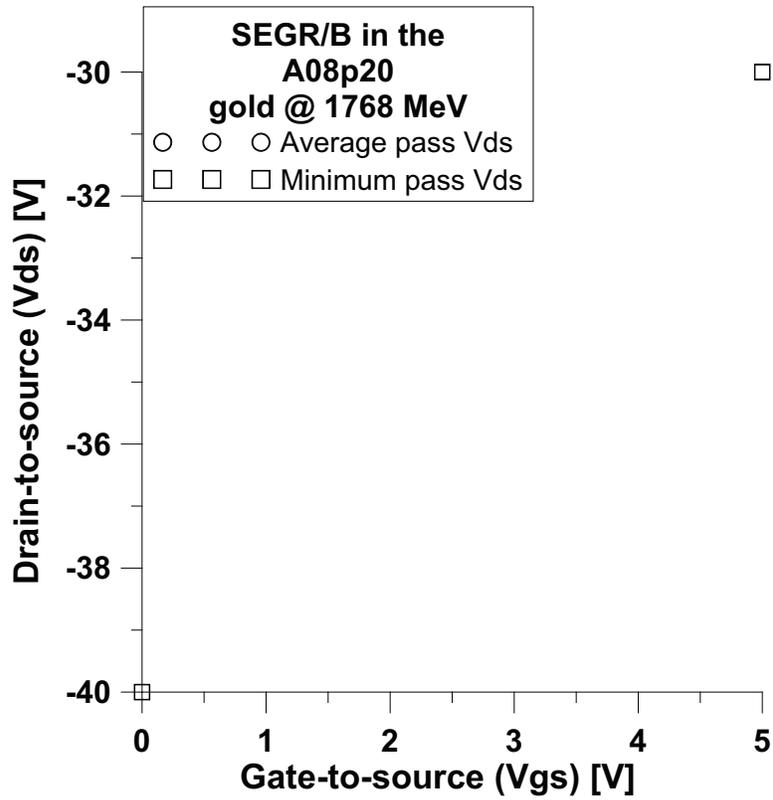


Figure 9.0-5. SEE test results of the 200 V Fuji p-channel with Au-1768 at BNL.

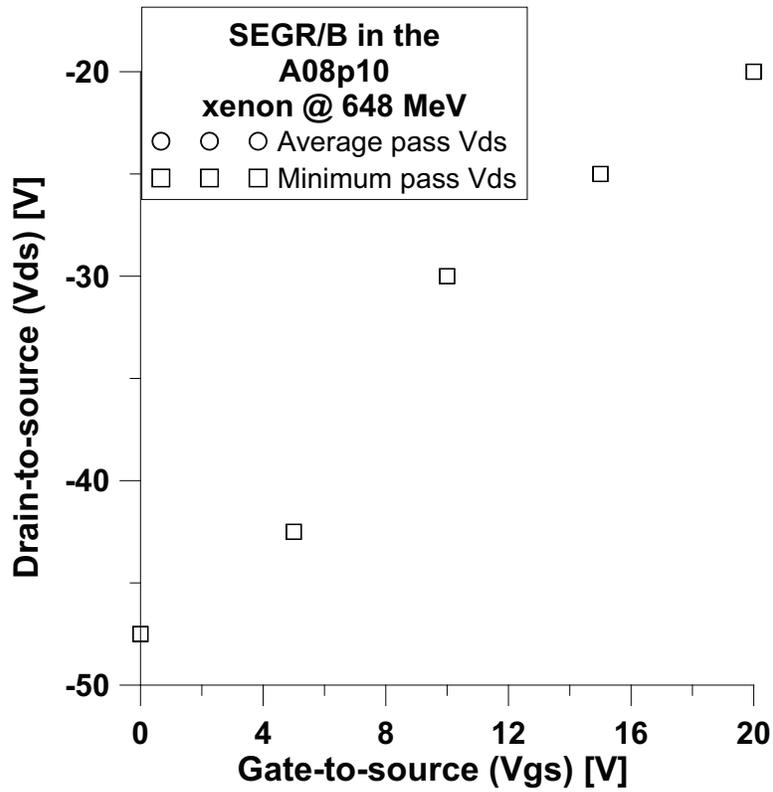


Figure 9.0-6. SEE test results of the 100 V Fuji p-channel with Xe-648 at TAM.

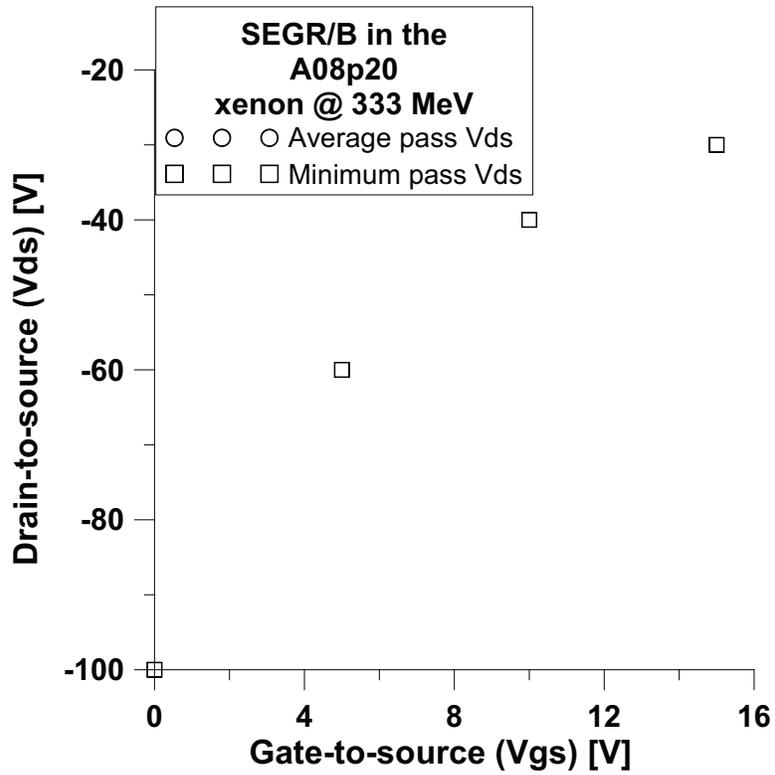


Figure 9.0-7. SEE test results of the 200 V Fuji p-channel with Xe-333 at TAM.

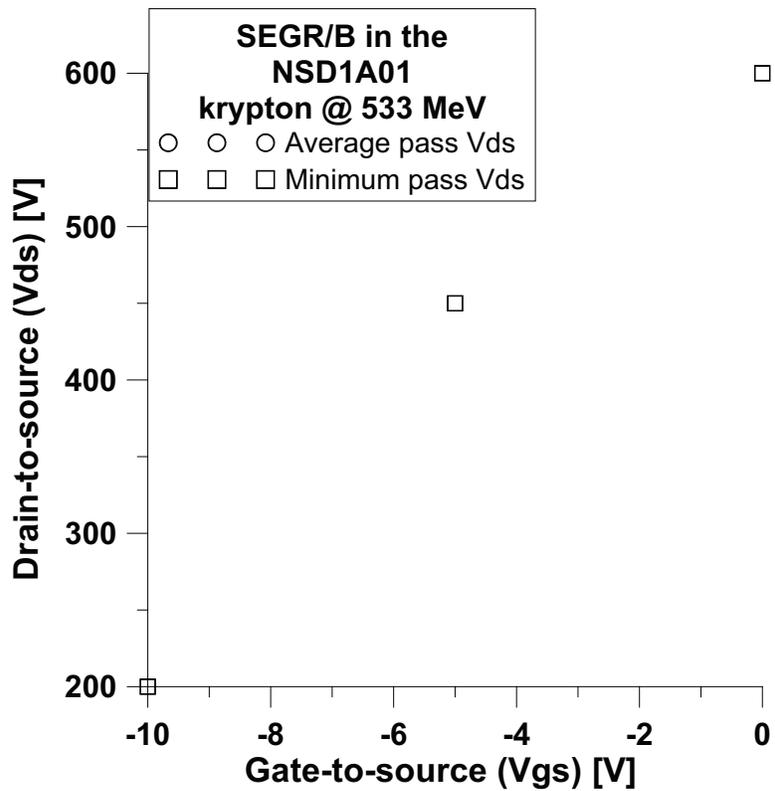


Figure 9.0-8. SEE test results of the 600 V Fuji n-channel with Kr-533 at TAM.

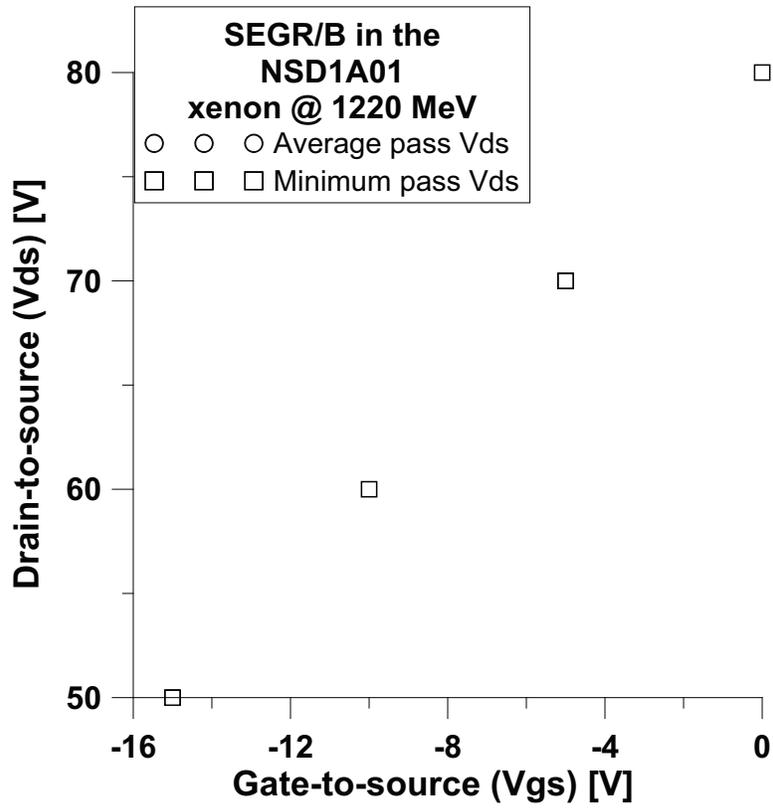


Figure 9.0-9. SEE test results of the 600 V Fuji n-channel with Xe-1220 at TAM.

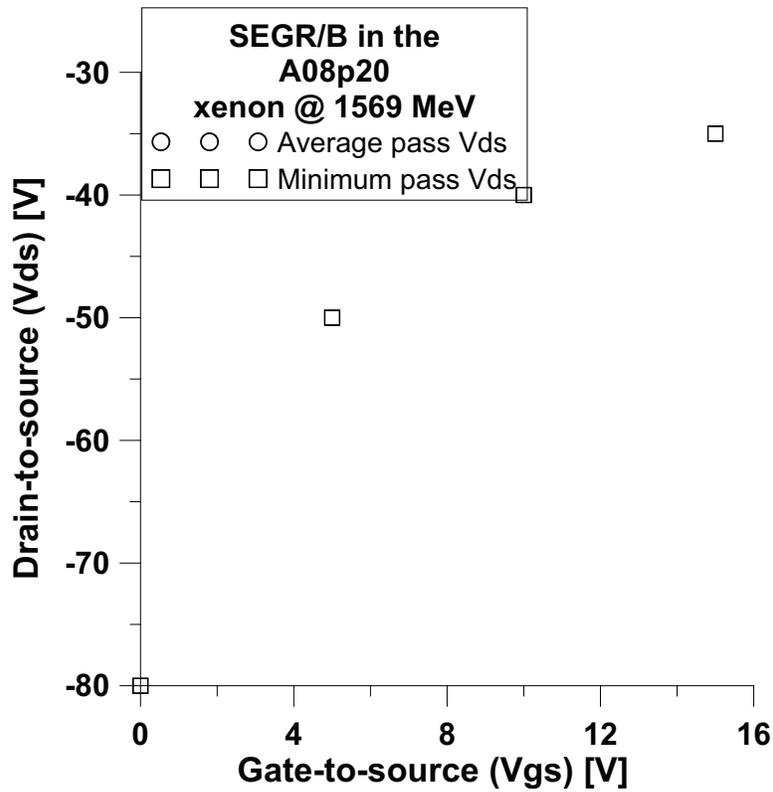


Figure 9.0-10. SEE test results of the 200 V Fuji p-channel with Xe-1569 at TAM.

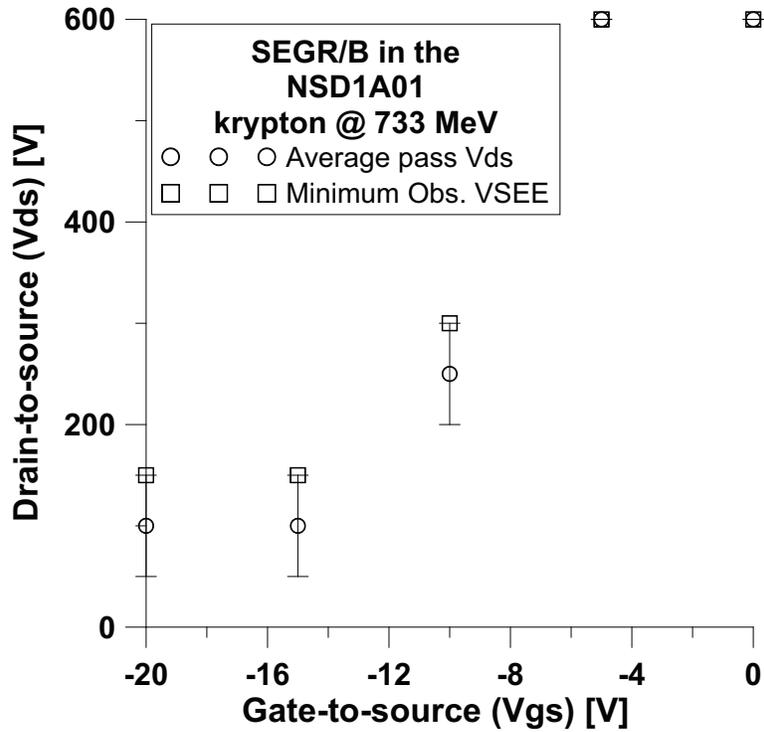


Figure 9.0-11. SEE test results of the 600 V Fuji n-channel with Kr-733 at TAM.

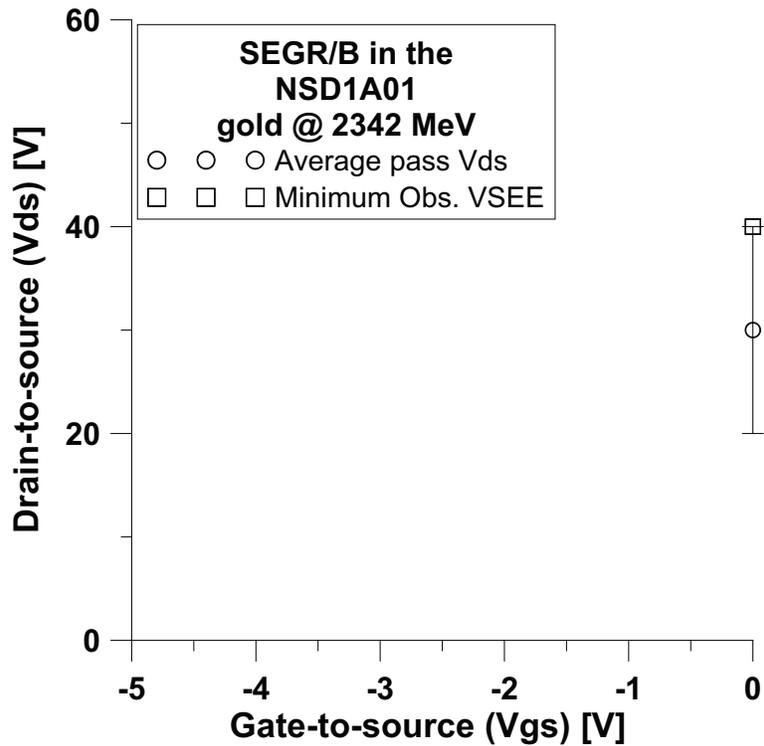


Figure 9.0-12. SEE test results of the 600 V Fuji n-channel with Au-2342 at TAM.

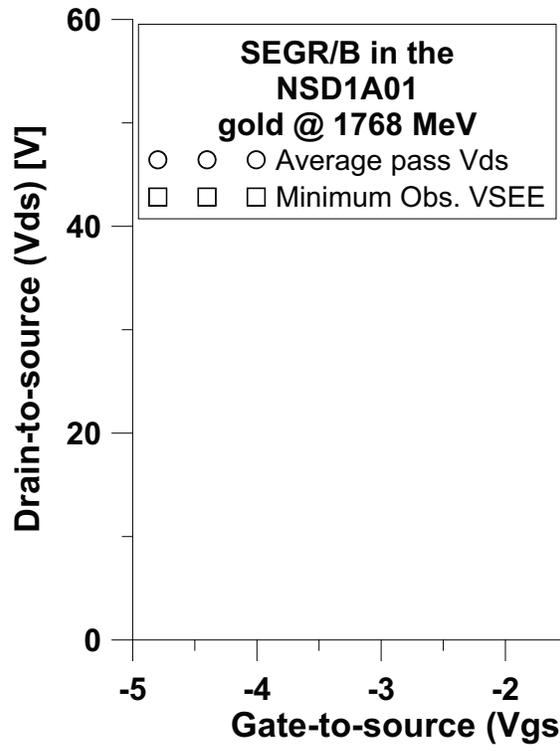


Figure 9.0-13. SEE test results of the 600 V Fuji n-channel with Au-1768 at TAM.

10.0 CONCLUSION AND RECOMMENDATION

These parts are comparable to similarly rated non-SE-hardened devices. However, the observations that the gate rupture occurred on the stress test as opposed to during the irradiation will require that testing of these devices employ the stress test for part assurance.

REPORT DOCUMENTATION PAGE

*Form Approved
OMB No. 0704-0188*

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY) 22-01-2014	2. REPORT TYPE JPL Publication	3. DATES COVERED (From - To)
--	--	-------------------------------------

4. TITLE AND SUBTITLE Single Event Gate Rupture Characterization of the Fuji MOSFETs: 2SJ1A03 (A08P10), 2SJ1A09 (A08P20), and NSD1A01	5a. CONTRACT NUMBER NAS7-03001
	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S) Scheick, Leif	5d. PROJECT NUMBER 102197
	5e. TASK NUMBER 3.23.5
	5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Jet Propulsion Laboratory California Institute of Technology 4800 Oak Grove Drive Pasadena, CA 91009	8. PERFORMING ORGANIZATION REPORT NUMBER JPL Publication 14-6
--	---

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001	10. SPONSORING/MONITOR'S ACRONYM(S)
	11. SPONSORING/MONITORING REPORT NUMBER

12. DISTRIBUTION/AVAILABILITY STATEMENT
Unclassified—Unlimited

Subject Category 33 Electronics and Electrical Engineering

Availability: NASA CASI (301) 621-0390 Distribution: Nonstandard

13. SUPPLEMENTARY NOTES

14. ABSTRACT
This testing is to characterize the power MOSFETs for single-event gate rupture (SEGR) and single-event burnout (SEB) response. Test results were compared against comparable voltage rated devices.

15. SUBJECT TERMS
Single-event burnout, SEB, metal-oxide-semiconductor field-effect transistor, MOSFET, Fuji, single-event gate rupture, SEGR, Texas A7M University, TAMU, Radiation Effect Facility, REF

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 36	19a. NAME OF RESPONSIBLE PERSON STI Help Desk at help@sti.nasa.gov
a. REPORT U	b. ABSTRACT U	c. THIS PAGE U			19b. TELEPHONE NUMBER (include area code) (301) 621-0390