SpaceCube v2.0 Space Flight Hybrid Reconfigurable Data Processing System

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www.nasa.gov
SpaceCube Family Overview

**v1.0**
- 2009 STS-125
- 2009 MISSE-7

**v1.5**
- 2012 SMART

**v2.0-EM**
- 2013 STP-H4
- 2015 STP-H5

**v2.0-FLT**
- 2015 GPS Demo
  - Robotic Servicing
  - Numerous proposals for Earth/Space/Helio

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SpaceCube, Target Applications

- Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities
  - Reconfigurable components: FPGA, Software, Mechanical
  - Promote reuse between applications
- Hybrid Flight Computing: hardware acceleration of algorithms to enable onboard data processing and increased mission capabilities
- Example Applications: Instrument Data Interfacing and On-Board Processing, Autonomous Operations, Situational Awareness, Scalable Computing Architectures

**Hardware Algorithm Acceleration**

<table>
<thead>
<tr>
<th>Application</th>
<th>Xilinx Device</th>
<th>Acceleration vs CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR Altimeter</td>
<td>Virtex-4 FX60</td>
<td>79x vs PowerPC 405 (250MHz, 300 MIPS)</td>
</tr>
<tr>
<td>RNS GN FIR FPU, Edge</td>
<td>Virtex-4 FX60</td>
<td>25x vs PowerPC 405 (250MHz, 300 MIPS)</td>
</tr>
<tr>
<td>HHT EMD, Spline</td>
<td>Virtex-1 2000</td>
<td>3x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
<tr>
<td>Hyperspectral Data Compression</td>
<td>Virtex-1 1000</td>
<td>2x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
<tr>
<td>GOES-8 GndSys Sun correction</td>
<td>Virtex-1 300E</td>
<td>6x vs Xeon Dual-Core (2.4GHz, 3000 MIPS)</td>
</tr>
</tbody>
</table>

**On-Board Data Reduction**

- On-board product generation yields factor of 165x data volume reduction
- SpaceCube 2.0 is 4x to 20x more capable than these earlier systems

Notes:
1) All functions involve processing large data sets (1MB+)
2) All timing includes moving data to/from FPGA
3) SpaceCube 2.0 is 4x to 20x more capable than these earlier systems
Example SpaceCube Processing

- Real-Time Image Tracking of Hubble
- Fire Classification
- Gigabit Instrument Interfacing

Xilinx ISS Radiation Data

Data Calibration

Image Compression
What defines a "High Performance Space Processing System"?
- Memory bandwidth and density, processing speed, reconfigurable, number of processors, I/O bandwidth, scalable, power, size and weight, temperature range, reliability, radiation, software flexibility
- Mission Context: differing driving requirements

Problem: All of these system variables push against each other
- Not taking the time to fully understand the dynamics between these variables will result in an unoptimized, inefficient design

Our Solution: SpaceCube v2.0
- Design Methodology
- Pushes all edges of technology for space flight
- Maintains excellent reliability standards
Balanced Design Closure of System Variables

- Reliability
- Processor Speed
- Number of Processors
- I/O Bandwidth
- Reconfigurablility
- System Scalability
- Software Flexibility
- Mechanical Size/Weight
- Memory Bandwidth/Density
- Thermal
- Parts Selection, Radiation, Longevity

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Design Flow for Constrained System

Design Closure Cycle

- Requirements/Concept
- Preliminary Electrical Design
- FPGA Planning
- Floorplanning
- Pre-Layout SI
- Layout Plan
- Therm/Mech

Design Confidence

Manufacturing

Design Implementation Cycle

- Schematic
- Therm/Mech
- Layout
- Vendors
- SI/PI
- Vendors
- SI/PI
SpaceCube v2.0 System

- Reconfigurable multi-processing platform based on Xilinx Virtex-5 FPGAs
- Extended 3U Compact PCI mechanical standard

Design Heritage

- v1.0: Back-to-Back, Core Software/FPGA, Aeroflex
- v1.5: Virtex-5 Design, GTX
- v2.0 EM: Layout, Key Circuits, SI/PI
- v2.0 FLT

Processor Comparison

<table>
<thead>
<tr>
<th>Processor</th>
<th>MIPS</th>
<th>Power</th>
<th>MIPS/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIL-STD-1750A</td>
<td>3</td>
<td>15W</td>
<td>0.2</td>
</tr>
<tr>
<td>RAD6000</td>
<td>35</td>
<td>15W</td>
<td>2.33</td>
</tr>
<tr>
<td>ColdFire</td>
<td>60</td>
<td>7W</td>
<td>8</td>
</tr>
<tr>
<td>RAD750</td>
<td>250</td>
<td>14W</td>
<td>18</td>
</tr>
<tr>
<td>LEON 3FT</td>
<td>89</td>
<td>5.5W</td>
<td>16</td>
</tr>
<tr>
<td>LEON3FT Dual-Core</td>
<td>200</td>
<td>10W</td>
<td>20</td>
</tr>
<tr>
<td>BRE440 (PowerPC)</td>
<td>266</td>
<td>5W</td>
<td>53</td>
</tr>
<tr>
<td>Maxwell SCS750</td>
<td>1200</td>
<td>25W</td>
<td>48</td>
</tr>
<tr>
<td>SpaceCube 1.0</td>
<td>3000</td>
<td>7.5W</td>
<td>400</td>
</tr>
<tr>
<td>SpaceCube 2.0</td>
<td>5000</td>
<td>9W</td>
<td>550</td>
</tr>
<tr>
<td>PowerPC (4x)</td>
<td>600</td>
<td>8W</td>
<td>75</td>
</tr>
<tr>
<td>MicroBlaze (4x)</td>
<td>2500</td>
<td>5W</td>
<td>400</td>
</tr>
</tbody>
</table>
v2.0 Processor Engineering Model

- 6U Board Design board layout to simulate a 3U layout for major components
- Test sample circuits, layout techniques, and interfacing architectures
- Roll lessons learned into flight system
  - Back-to-Back layout strategy for all like parts
  - Signal integrity solutions
  - Oscillator and power architecture
  - Connector selection
  - Unique layout strategy for accomplishing IPC 6012B Class 3/A PWB
SpaceCube v2.0 Flight System

Power Card
- 22-38V Input, 7A limit
- 5V/80W, 3.3V/53W,
- +/-12V/24W

Backplane Card
- 4 slots
- Point-to-Point
- Gigabit
- 2 processors, 1 I/O
- 3 processors

Chassis: 12.7 x 23 x 27 cm^3

Example I/O Card: GPS RF
### Processor Card

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Draw</td>
<td>6-12W</td>
</tr>
<tr>
<td>Weight</td>
<td>0.98-lbs</td>
</tr>
<tr>
<td>Layers</td>
<td>22 Layers, Via-in-Pad</td>
</tr>
<tr>
<td>Standards</td>
<td>IPC 6012B Class 3/A</td>
</tr>
</tbody>
</table>

- 2x Xilinx Virtex-5 (QV) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 1x 64Mb PROM, contains initial Xilinx bitfile (will also support 128Mb PROM)
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 4x 512MB DDR SDRAM
- 2x 4GB NAND Flash
- 16-channel Analog/Digital circuit for system health
- Optional 10/100 Ethernet interface
- Gigabit interfaces: 4x external, 2x on backplane
- 12x Full-Duplex dedicated differential channels
- 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Mechanical support for heat sink options and stiffener for Xilinx devices
Design Analysis

Thermal: -40°C to 65°C

Power Integrity
- Improved Flash Decoupling
- Current Density
- Xilinx Core Voltage

Structural
- 1st Box Mode (Z) – 790 Hz
- 2nd Box Mode (X) – 970 Hz
- 3rd Box Mode (Y) – 1090 Hz

Signal Integrity
- Signal Quality
- 3Gpbs GTX Eye Diagram

Crosstalk:
- Critical net < 10mV
- Non Critical net < 70mV
ISS SpaceCube Experiment 2.0

- FireStation
- SpaceCube v2.0 EM
- Camera Box
- CIB
- Antenna

Image Credit: DoD Space Test Program
STP-H4 Operational on ISS

Next Up: STP-H5 and Sounding Rocket Launch in 2015

Somewhere near Big Sky, MT
ISE2.0 Results

Operations
- GSFC Command Center
- August 2013 - Present

Radiation

<table>
<thead>
<tr>
<th>FPGA</th>
<th>SEUs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>17</td>
</tr>
<tr>
<td>2</td>
<td>13</td>
</tr>
<tr>
<td>3</td>
<td>17</td>
</tr>
</tbody>
</table>

~1 SEU/FPGA/Week
System Resets: TBD

HD Images Received: 200,000+

FireStation Instrument
Data Processing
Satellite Servicing

STP-H5 Autonomous Rendezvous and Docking Payload
- SpaceCube v2.0 EM
- Leverages SpaceCube v1.0 RNS/Argon demonstrations

Objective: Robotic Satellite Servicing Mission
- SpaceCube v2.0 Flight System
- 2 Processors/SpaceCube
- 3 SpaceCubes controlling AR&D and robotic tasks

GSFC Satellite Servicing Laboratory

Argon with SpaceCube v1.0 Control

GOES-12 Model
Raven ConOps

Range to target [m]: 2072.3
RSB to Target [m]: [-4.3, -0.1, -2072.3]
Joint Angles [deg]: 44.35, 0.61
Softstop flag: 0 0
00:03:04 [20x Realtime]
Conclusions

- An advanced HPC for space **requires** well balanced system variables
- Imperative to iterate on design plan before starting schematics
  - No use starting something that will not close on requirements
  - System Designer: Know what you want to build, and how to build it
  - Pull all disciplines into design cycle at the beginning
- SpaceCube design methodology successful in converging on a cutting-edge HPC design given constrained size requirements
  - SIZE/WEIGHT = $$ → Make it smaller!!!
  - Back-to-Back parts placement
  - Extensive analysis
  - Built to high reliability standards
- SpaceCube v2.0 Flight System
  - Design heritage leveraged from 3 prior systems
  - Operations heritage leveraged from 5 flights
    - By 2015, 9 SpaceCube systems flown → 22 Xilinx FPGAs in space
  - Competitive HPC for space
  - Multiple mission applications, reconfigurable