A stackable form-factor Peripheral Component Interconnect (PCI) device can be configured as a host controller or a master/target for use on a PCI assembly. The PCI device may comprise a multiple-input switch coupled to a PCI bus, a multiplexor coupled to the switch, and a reconfigurable device coupled to one of the switch and multiplexor. The PCI device is configured to support functionality from power-up, and either control function or add-in card function.

14 Claims, 3 Drawing Sheets
FIG. 1
(PRIOR ART)
FIG. 2
STACKABLE FORM-FACTOR PERIPHERAL COMPONENT INTERCONNECT DEVICE AND ASSEMBLY

CROSS REFERENCE TO RELATED APPLICATIONS


STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

The invention described herein was made by employees of the United States Government and may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

FIELD OF THE INVENTION

This invention relates to Peripheral Component Interconnect (PCI) hardware configurations. More specifically, the invention is a stackable form-factor PCI device that can be configured as a host controller, a master card, or a target card.

BACKGROUND OF THE INVENTION

PCI assemblies may include a host controller coupled to a PCI bus, and one or more master devices and one or more target devices. The master and target devices may also be coupled to the PCI bus. One type of PCI assembly is a stackable form-factor assembly. A representative stackable form-factor PCI assembly 100 in conformance with a PC/104 or PC/104-Plus specification is illustrated in FIG. 1. Briefly, clock signals 103 from a host controller 102 are length-matched to compensate for the distance from host controller 102 to each master/target card 104 coupled to a PCI bus 106. That is, host controller 102 adjusts or skews timing of the clock signals 103 depending on how far the clock signal 103 must travel to a particular master/target card 104.

For a PC/104-Plus assembly, each master/target card 104 utilizes 4:1 multiplexer 104A to manage clock signal selection from PCI bus 106. In terms of providing a device clock signal for the particular master/target device 104B, multiplexer 104A selects the appropriate time-skewed clock signal from PCI bus 106 for the device clock 108. Since clock signal adjustments or skewing is unique to host controller 102, the PCI assembly requires a design for a host controller 102 and a different design for a master/target card 104.

In addition, stackable form-factor PCI devices/assemblies may be constructed using SRAM-based Field Programmable Gate Arrays (FPGAs). However, these types of devices require device configuration after power up and before use thereof. This time delay (on the order of several hundred milliseconds) delays the PCI assembly’s operational functions.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a PCI device that is configurable as a host controller, a master card, or a target card in a stackable form-factor PCI assembly.
multiplexor coupled to the switch and a reconfigurable device coupled to one of the switch and the multiplexor. The reconfigurable device may be configured as a PCI host controller generating clock signals time-skewed in correspondence with known locations on the PCI bus. The reconfigurable device can provide the clock signals to the switch wherein the clock signals are driven onto the PCI bus. The reconfigurable device may be configured as at least one of a PCI master device and a PCI target device. The switch may (i) receive the clock signals from the PCI bus at one of the known locations corresponding to the at least one of a PCI master device and a PCI target device, and (ii) provide the clock signals so-received to the multiplexor wherein one of the clock signals is selected by the multiplexor for presentation to the at least one of a PCI master device and a PCI target device. The switch, multiplexor and reconfigurable device may be configured on a FPGA, which may include a flash-based FPGA.

A stackable PCI assembly is also provided comprising a PCI bus, a plurality of PCI devices coupled to the PCI bus. Each PCI devices may comprise a multiple-input switch coupled to the PCI bus; a multiplexor coupled to the switch; and a reconfigurable device coupled to one of the switch and multiplexor. The reconfigurable device may be configured as a PCI host controller generating clock signals time-skewed in correspondence with known locations on the PCI bus. The reconfigurable device can provide the clock signals to the switch such that the clock signals are driven onto the PCI bus. The reconfigurable device is configured as at least one of a PCI master device and a PCI target device. The switch can (i) receive the clock signals from the PCI bus at one of the known locations corresponding to the at least one of a PCI master device and a PCI target device, and (ii) provide the clock signals so-received to the multiplexor. One of the clock signals may be selected by the multiplexor for presentation to the at least one of a PCI master device and a PCI target device.

Each PCI devices may comprise a multiple-input switch coupled to the PCI bus; and a multiplexor coupled to the switch; and a reconfigurable device coupled to one of the switch and multiplexor. The reconfigurable device may be configured as a PCI host controller generating clock signals time-skewed in correspondence with known locations on the PCI bus. The reconfigurable device can provide the clock signals to the switch such that the clock signals are driven onto the PCI bus. The reconfigurable device is configured as at least one of a PCI master device and a PCI target device. The switch can (i) receive the clock signals from the PCI bus at one of the known locations corresponding to the at least one of a PCI master device and a PCI target device, and (ii) provide the clock signals so-received to the multiplexor. One of the clock signals may be selected by the multiplexor for presentation to the at least one of a PCI master device and a PCI target device.

The advantages of the present invention are numerous. A single hardware design can be configured as a host controller for use in a stackable form-factor PCI assembly; and an embodiment of the present invention in accordance with an embodiment of the present invention, and should not be inter-
5 interpreted as limitations on the scope of the invention as defined by the appended claims and it is to be appreciated that various changes, rearrangements and modifications may be made therein, without departing from the scope of the invention as defined by the appended claims.

What is claimed as new and desired to be secured by Letters Patent of the United States is:

1. A stackable form-factor Peripheral Component Interconnect (PCI) device, comprising:
   a multiple-input switch adapted to be coupled to a PCI bus;
   a multiplexor coupled to said switch;
   a reconfigurable device coupled to one of said switch and said multiplexor;
   wherein said switch comprises a 2:1 switch.

2. The stackable form-factor PCI device as in claim 1, wherein said switch, said multiplexor and said reconfigurable device are configured on a Field Programmable Gate Array (FPGA).

3. The stackable form-factor PCI device as in claim 2, wherein said FPGA comprises a flash-based FPGA.

4. The stackable form-factor PCI device as in claim 1, wherein said switch comprises a 2:1 switch.

5. The stackable form-factor PCI device as in claim 1, wherein said multiplexor comprises a 4:1 multiplexor.

6. A stackable form-factor Peripheral Component Interconnect (PCI) device, comprising:
   a multiple-input 2:1 switch adapted to be coupled to a PCI bus;
   a 4:1 multiplexor coupled to said switch;
   a reconfigurable device coupled to one of said switch and said multiplexor;
   wherein when said reconfigurable device is configured as a PCI host controller generating clock signals time-skewed in correspondence with known locations on the PCI bus, said reconfigurable device provides said clock signals to said switch wherein said clock signals are driven onto the PCI bus and wherein when said reconfigurable device is configured as at least one of a PCI master device and a PCI target device, said switch (i) receives said clock signals from the PCI bus at one of said known locations corresponding to said at least one of a PCI master device and a PCI target device, and (ii) provides said clock signals so-received to said multiplexor wherein one of said clock signals is selected by said multiplexor for presentation to said at least one of a PCI master device and a PCI target device.

7. The stackable form-factor PCI device as in claim 6, wherein said switch, said multiplexor and said reconfigurable device are configured on a Field Programmable Gate Array (FPGA).

8. The stackable form-factor PCI device as in claim 7, wherein said FPGA comprises a flash-based FPGA.

9. A stackable form-factor Peripheral Component Interconnect (PCI) assembly comprising:
   a PCI bus,
   a plurality of PCI devices coupled to said PCI bus, each of said PCI devices comprising:
   a multiple-input switch coupled to said PCI bus;
   a multiplexor coupled to said switch;
   a reconfigurable device coupled to one of said switch and said multiplexor;
   wherein, when said reconfigurable device is configured as a PCI host controller generating clock signals time-skewed in correspondence with known locations on said PCI bus, said reconfigurable device provides said clock signals to said switch wherein said clock signals are driven onto said PCI bus and wherein, when said reconfigurable device is configured as at least one of a PCI master device and a PCI target device, said switch (i) receives said clock signals from the PCI bus at one of said known locations corresponding to said at least one of a PCI master device and a PCI target device, and (ii) provides said clock signals so-received to said multiplexor wherein one of said clock signals is selected by said multiplexor for presentation to said at least one of a PCI master device and a PCI target device.

10. The stackable form-factor PCI assembly as in claim 9, wherein each of said PCI devices is configured on a Field Programmable Gate Array (FPGA).

11. The stackable form-factor PCI assembly as in claim 10, wherein said FPGA comprises a flash-based FPGA.

12. The stackable form-factor PCI assembly as in claim 11, wherein said FPGA is programmed with a hardware description language for instant functionality from when said power on/off control powers-on the PCI assembly.

13. The stackable form-factor PCI assembly as in claim 9, wherein said multiplexor comprises a 4:1 multiplexor.

14. The stackable form-factor PCI assembly as in claim 13, wherein said switch comprises a 2:1 switch.

* * * * *