Comparing On-Orbit and Ground Performance for an S-Band Software-Defined Radio

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Overview

- Introduction to Software Defined Radio (SDR)
  - Why SDR?
  - Space Communications and Navigation (SCaN) Testbed

- Pre-launch Characterization

- Design of a Received Power Estimator
  - Ground development
  - Space performance
Why Software-Defined Radio?

- Software-defined radio (SDR) – a modern communication platform
  - Radio frequency module
  - Signal processing module [waveform]
  - General processing module

- SDR is...

  ADAPTABLE!

  FLEXIBLE!

  PREDICTABLE…?
NASA’s SCaN Testbed (STB)

- Space Communications and Navigation (SCaN) Testbed
  - External payload on the International Space Station (ELC-3 location)

SCaN Testbed installed to the ExPRESS Logistics Carrier-3

SCaN Testbed hardware block diagram
Jet Propulsion Laboratory (JPL) SDR – part of STB

- S-band transceiver (7 Watts) with L-band receive capability
- 66 MHz SPARC (RTEMS) processor and 2 Virtex-II FPGAs

Three JPL SDRs!

- Flight model (FM)
  - Radio Frequency Module, Global Positioning System Module, Baseband Processing Module, Power Amplifier / Power Supply Module
- Engineering model (EM)
  - Same as FM, except commercial grade parts.
- Breadboard
  - Baseband Processing Module only.
Ground Testing

- **Flight model SDR testing prior to launch**
  - Establish a performance baseline in a controlled environment
  - Collect data useful for future waveform capabilities

- **Lesson Learned – test the hardware independent of the waveform**
  - Test very close to hardware interfaces
  - Do not make testing dependent on software implementation

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**Diagram:**

- Diplexer
- PLL / Down-conversion
- AGC
- ADC
- Signal Processing Module
- PA
- PLL / Up-conversion
- DAC

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**Abbreviations:**

- **ADC** – Analog-to-Digital Converter
- **DAC** – Digital-to-Analog Converter
- **PLL** – Phase Lock Loop
- **AGC** – Automatic Gain Control
- **PA** – Power Amplifier
Received Power Estimator (PE) Design

- Estimating received power is a useful diagnostic feature
- Uses existing waveform despreader digital filters
  - Performed at the intermediate frequency (IF) after downconversion
  - BPSK filter bandwidth = 2*(signal bandwidth) + (Doppler allowance)
  - Despreader PN generator is bypassed for non-spread modes.
PE Ground Calibration

- Performed testing on the engineering model
  - Map the “Integrate & Dump” value to the corresponding input power
  - Swept input power level across realistic space received power range
  - Power Estimate = Signal Power + Noise Power
- Waveform “mode” → data rate, frequency, spreading, etc.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Spread</th>
<th>Symbol Rate (ksp/s)</th>
<th>Freq. MHz</th>
<th>Filter BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Yes</td>
<td>18</td>
<td>2106</td>
<td>149</td>
</tr>
<tr>
<td>B</td>
<td>Yes</td>
<td>36</td>
<td>2106</td>
<td>188</td>
</tr>
<tr>
<td>C</td>
<td>Yes</td>
<td>18</td>
<td>2041</td>
<td>149</td>
</tr>
<tr>
<td>D</td>
<td>Yes</td>
<td>36</td>
<td>2041</td>
<td>188</td>
</tr>
<tr>
<td>E</td>
<td>No</td>
<td>155</td>
<td>2041</td>
<td>450</td>
</tr>
<tr>
<td>F</td>
<td>No</td>
<td>310</td>
<td>2041</td>
<td>789</td>
</tr>
<tr>
<td>G</td>
<td>No</td>
<td>769</td>
<td>2041</td>
<td>1793</td>
</tr>
<tr>
<td>H</td>
<td>No</td>
<td>1538</td>
<td>2041</td>
<td>3468</td>
</tr>
</tbody>
</table>
PE Space Test Considerations

♦ Limited power range and test time in space
  • Space link varies by ~2 dB due to distance over ~40 minutes
  • NASA satellites have 2 fixed transmit power levels

♦ Implemented spiral motion on the MGA
  • Swept elevation over a wide range of power (~20 dB) during 1 pass
  • Used 1-degree lap size based on in-situ antenna pattern
PE Space Test Results - Spread

♦ Spread-spectrum results versus engineering model performance

- 0.1 dB error
- 0.3 dB error
- 0.6 dB error
- 0.8 dB error
Non-spread BPSK results versus engineering model performance

- 2.2 dB error
- 1.5 dB error
- 0.4 dB error
- 11 dB error
Results

- **Overall the power estimator performance is acceptable.**
  - Spread waveform modes show less than 1 dB average error
  - Non-spread modes show 1 to 2 dB average error (except mode H)

- **The power estimator is sensitive to AGC fluctuation.**
  - AGC level directly affects the IF power level
  - Mode H has a very low AGC set point → 11 dB average error!

- **Future work**
  - Improve understanding of how wideband noise affects the AGC algorithm
  - Incorporate AGC level into the power estimator
  - Look into narrower filter bandwidths for lower received power levels