An Airborne Onboard Parallel Processing Testbed

Dan Mandl
NASA/GSFC Software Engineering Division
2014 ESTO Science and Technology Forum
Objectives for Intelligent Payload Module Testbed

• Low power/high performance benchmarking
  – Test various typical onboard science processing requirements with parallel processing via multicore processors and field programmable gate array circuits
  – Target processors that can be radiation tolerant or radiation hardened

• Airborne Intelligent Payload Module (IPM) box used as proxy for satellite version of IPM

• Research being conducted under AIST-11 effort, “A High Performance Onboard Multicore Intelligent Payload Module for Orbital and Suborbital Decadal Missions”
Potential Users of IPM

• HyspIRI Smallsat mission
  – Visible ShortWave InfraRed (VSWIR) Imaging Spectrometer
  – Multispectral Thermal InfraRed (TIR) Scanner

• HyspIRI Space Station mission
  – Visible ShortWave InfraRed (VSWIR) Imaging Spectrometer
  – Multispectral Thermal InfraRed (TIR) Scanner

• Geocape
Sample Operational Scenario: Detection of Harmful Algal Blooms with Rapid Map Downlinked to Validation Team on Ground

Realtime map with following processing steps:
- Radiance to reflectance conversion
- Atmospheric Correction
- Geocorrection/Co-registration
- Classification (Web Coverage Processing Service)
- Vectorization and data reduction

Downlink to Ipad

Harmful Algal Bloom
Processors Used in Conjunction With The Testbed
Tilera Tile64 as Proxy for Maesto

Specifications
- Launched on August 20, 2007
- **8 x 8 tile array (64 cores)**
- Each tile on chip is an independent processor capable of running an entire operating system
- 700MHz - 866MHz (No FPU)
- 15 - 22W @ 700MHz all 64 cores running
- Idle tiles can be put into low-power sleep mode
- ANSI standard C / C++ compiler
- Supports SMP Linux with 2.6 kernel

Issues
- Special data homing considerations required when programming/compiling for the TILE64
  - Uses a crude coherence strategy; each shared memory location may only be cached in one tile – its “home” tile. A location’s home tile is fixed at runtime
  - Accessing remotely-cached data is correct, but performance is low
  - Prevents TILE64 from efficiently running existing generic multithreaded code
  - Careful “homing” of data is crucial to good scalability
- TILE64’s compiler does not use the now-standard C++ ABI popularized by GCC 3.2+
  - This compiler is closed-source, based on SGI’s “MIPSPro”
  - Prevents linkage with and preprocessing by other C++ compilers, such as AESOP
Maestro as Proxy for Maestro-lite

- Origin - DARPA Polymorphic Computer Architecture (PCA Program)
- DARPA/DTRA Radiation Hardened By Design (RHBD) 90 nm IBM CMOS process
- Government purchased Tilera Corp’s (commercial 64 core processor) software intellectual property (IP) for government space-based applications
- Program managed by National Reconnaissance Office (NRO)
- Maestro Chip developed by Boeing Solid-State Electronics Development (SSED)
- Government customers: NASA, NRO, Air Force Research Laboratory
- Maestro basic specifications
  - 7 x 7 tile array (49 cores)
  - 300 MHz, 45 GOPs, 22 GFLOPS (FPU on each tile)
  - 18 Watts typical
  - RHBD Total Ionizing Dose (TID) >500krad
Tilera TilePro64 as Proxy for Maestro

Specifications
• Launched on September 22, 2008
• 8 x 8 tile array (64 cores)
• Each tile on chip is an independent processor capable of running an entire operating system
• 700MHz - 866MHz (No FPU)
• 19 - 23W @ 700MHz all 64 cores running
• Idle tiles can be put into low-power sleep mode
• ANSI standard C / C++ compiler
• Supports SMP Linux with 2.6 kernel

Addressed issues exhibit in TILE64
• Uses a better cache coherence protocol allowing many tiles to cache the same data
• The native compiler is now an open-source port of GCC 4.4, using standard C++ ABI
  ▪ Compiler and toolchain is actively supported
  ▪ October 14 2011 - Tilera contributed its port back to the GCC project
• First-class Linux kernel architecture
• Presently in IPM used during recent flights
Tilera Tile-Gx8036 / Tile-Gx8009 as Proxy for Maestro

Specifications

- Launched on January 30, 2012
- 6 x 6 tile array (36 cores) / 3 x 3 tile array (9 cores)
- Each tile on chip is an independent processor
- capable of running an entire operating system
- 1GHz – 1.5GHz (FPU)

- 27 - 30W @ 1.2GHz all 36 cores running
- 9 – 10W @ 1.0GHz all 9 cores running
- Idle tiles can be put into low-power sleep mode
- ANSI standard C / C++ compiler
- Supports SMP Linux with 2.6 kernel
<table>
<thead>
<tr>
<th>Unit</th>
<th>Mission</th>
<th>Notes</th>
<th>Specs</th>
<th>Stats</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpaceCube 1.0a</td>
<td>Hubble SM 4 RNS Experiment STS-125 May 2009</td>
<td>4&quot;x4&quot; card (2) Virtex4</td>
<td>Size: 5&quot;x5&quot;x7&quot; Wt: 7.5 lbs Pwr: 16W x 2</td>
<td>2009 Flight</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 1.0b</td>
<td>MISSE-7/8 added RS-485, RHBS, STS-129 Nov 2009</td>
<td>4&quot;x4&quot; card (2) Virtex4</td>
<td>Size: 5&quot;x5&quot;x7&quot; Wt: 7.5 lbs Pwr: 16W x 2</td>
<td>Operating on ISS Since Nov 2009</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 1.5</td>
<td>SMART added GigE &amp; SATA SubTec-5 Jun 2011</td>
<td>4&quot;x4&quot; card (1) Virtex5</td>
<td>Size: 5&quot;x5&quot;x4&quot; Wt: 4 lbs Pwr: 10W</td>
<td>2011 Flight</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 1.0c</td>
<td>Argon Demo added 1553 &amp; Ethernet</td>
<td>4&quot;x4&quot; card (2) Virtex4</td>
<td>Size: 5&quot;x5&quot;x7&quot; Wt: 7.5 lbs Pwr: 18W x 2</td>
<td>Demonstration Testbed</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 1.0 d, e, f</td>
<td>STP-H4, future STP-H5 &amp; RRM3 added 1553 &amp; Ethernet</td>
<td>4&quot;x4&quot; card (2) Virtex4</td>
<td>Size: 5&quot;x5&quot;x7&quot; Wt: 7.5 lbs Pwr: 15W</td>
<td>On ISS Since Aug 2013</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 2.0</td>
<td>Earth/Space Science, SSCO, GPS Nav Std 3U form factor, GigE, SATA, Spacewire, cPCI</td>
<td>4&quot;x7&quot; card (2) Virtex 5 + (1) Aeroflex</td>
<td>Size: 5&quot;x5&quot;x7&quot; Wt: &lt; 10 lbs Pwr: 15-20W</td>
<td>EM On ISS Since Aug 2013 (Flight Unit In Development)</td>
<td></td>
</tr>
<tr>
<td>SpaceCube 2.0 Mini</td>
<td>CubeSats, Sounding Rocket, UAV “Mini” version of SpaceCube 2.0</td>
<td>3.5&quot;x3.5&quot; card (1) Virtex 5 + (1) Aeroflex</td>
<td>Size: 4&quot;x4&quot;x4&quot; Wt: &lt; 3 lbs Pwr: 8W</td>
<td>Flight Unit in Development (2016 launch)</td>
<td></td>
</tr>
</tbody>
</table>
**SpaceCube Family Overview**

**v1.0**
- 2009 STS-125
- 2009 MISSE-7
- 2013 STP-H4
- 2016 STP-H5

**v1.5**
- 2012 SMART

**v2.0-EM**
- 2013 STP-H4
- 2016 STP-H5

**v2.0-FLT**
- 2015 GPS Demo
  - Robotic Servicing
  - Numerous proposals for Earth/Space/Helio
## Processor Comparison

<table>
<thead>
<tr>
<th>Processor</th>
<th>MIPS</th>
<th>Power</th>
<th>MIPS/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIL-STD-1750A</td>
<td>3</td>
<td>15W</td>
<td>0.2</td>
</tr>
<tr>
<td>RAD6000</td>
<td>35</td>
<td>15W</td>
<td>2.33</td>
</tr>
<tr>
<td>RAD750</td>
<td>300</td>
<td>15W</td>
<td>20</td>
</tr>
<tr>
<td>LEON 3FT</td>
<td>75</td>
<td>5W</td>
<td>15</td>
</tr>
<tr>
<td>LEON3FT Dual-Core</td>
<td>250</td>
<td>10W</td>
<td>25</td>
</tr>
<tr>
<td>BRE440 (PPC)</td>
<td>230</td>
<td>5W</td>
<td>46</td>
</tr>
<tr>
<td>Maxwell SCS750</td>
<td>1200</td>
<td>25W</td>
<td>48</td>
</tr>
<tr>
<td>SpaceCube 1.0</td>
<td>3000</td>
<td>7.5W</td>
<td>400</td>
</tr>
<tr>
<td>SpaceCube 2.0</td>
<td>6000</td>
<td>10W</td>
<td>600</td>
</tr>
<tr>
<td>SpaceCube Mini</td>
<td>3000</td>
<td>5W</td>
<td>600</td>
</tr>
</tbody>
</table>
ZC702 – Zynq (ARM/FPGA Processor) Proxy for COTS+RH+FTC CHREC Space Processor (CSP)

### COTS
- Zynq-7020 hybrid SoC
  - Dual ARM A9/NEON cores
  - Artix-7 FPGA fabric + hard IP
- DDR3 memory

### RadHard
- NAND flash
- Power circuit
- Reset circuit
- Watchdog unit

### FTC = Fault-Tolerant Computing
- Variety of mechanisms
  - External watchdog unit to monitor Zynq health and reset as needed
  - RSA-authenticated bootstrap (primary, secondary) on NAND flash
  - ECC memory controller for DDR3 within Zynq
  - ADDAM middleware with message, health, and job services
  - FPGA configuration scrubber with multiple modes
  - Internal watchdogs within Zynq to monitor behavior
  - Optional hardware, information, network, software, and time redundancy
IPM Hardware

- 14 x 14 x 6 inches
- Wide-Input-Range DC voltage (6V-30V)
- Made of strong durable aluminum alloy
- Dual mounting brackets
- Flush design
- Removable side panels
- Mounting racks are electrically isolated from the box
- Appropriate space allocation for interchangeable Tilera and SpaceCube boards
- Electronic components
  - Tilera development board
  - SpaceCube development board
  - Single board computer
  - 600GB SSD
  - Gigabit Ethernet switch
  - Transceiver radio
  - Power board
IPM Hardware
# Compact Hyperspectral Advanced Imager (CHAI V640)

## Specifications

### Mechanicals

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Estimate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (with lens)</td>
<td>125 x 101 x 75 mm</td>
</tr>
<tr>
<td>Size (with telescope)</td>
<td>200 x 101 x 75 mm</td>
</tr>
<tr>
<td>Weight</td>
<td>48 kg (.99 lbs)</td>
</tr>
<tr>
<td>Power</td>
<td>20 watts</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-20 to +50 °C</td>
</tr>
<tr>
<td>Size does not include NS/GPS</td>
<td></td>
</tr>
</tbody>
</table>

### Optics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spectrometer Type</td>
<td>Diyan</td>
</tr>
<tr>
<td>Telescope</td>
<td>All-reflective telescope</td>
</tr>
<tr>
<td>Field of View</td>
<td>40 degrees</td>
</tr>
<tr>
<td>Cross Track Pixels</td>
<td>640</td>
</tr>
<tr>
<td>F-Number</td>
<td>f/2</td>
</tr>
<tr>
<td>Spectral Range</td>
<td>350-1080 nm (Reflective)</td>
</tr>
<tr>
<td></td>
<td>400-1000 nm (Refractive)</td>
</tr>
<tr>
<td>Smile Distortion</td>
<td>&lt; 0.1 pixels</td>
</tr>
<tr>
<td>Keystone Distortion</td>
<td>&lt; 0.1 pixels</td>
</tr>
<tr>
<td>Stray Light</td>
<td>&lt; 1e-4 Point Source Transmission</td>
</tr>
<tr>
<td>Spectral Bands</td>
<td>256</td>
</tr>
<tr>
<td>Spectral Sampling</td>
<td>2.5, 5, 10 nm</td>
</tr>
<tr>
<td>Peak Grating Efficiency</td>
<td>88%</td>
</tr>
<tr>
<td>Slit Size</td>
<td>9.6 x .015 mm</td>
</tr>
</tbody>
</table>

## Image Sensor

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image Sensor</td>
<td>640 x 512, with 15 μm pixels</td>
</tr>
<tr>
<td>Full Well Capacity</td>
<td>Gain 0: 500,000</td>
</tr>
<tr>
<td></td>
<td>Gain 1: 80,000</td>
</tr>
<tr>
<td></td>
<td>Gain 2: 10,000</td>
</tr>
<tr>
<td>Read Noise</td>
<td>Gain 0: &lt; 83 electrons</td>
</tr>
<tr>
<td></td>
<td>Gain 1: &lt; 42 electrons</td>
</tr>
<tr>
<td></td>
<td>Gain 1: &lt; 10 electrons</td>
</tr>
<tr>
<td>Maximum Frame Rate</td>
<td>1000 frames/second</td>
</tr>
<tr>
<td>Quantum Efficiency</td>
<td>&gt; 50% @ 380 nm</td>
</tr>
<tr>
<td></td>
<td>80% @ 400-900 nm</td>
</tr>
<tr>
<td></td>
<td>&gt; 30% @ 1000 nm</td>
</tr>
<tr>
<td>Camera Interface</td>
<td>USB-3</td>
</tr>
<tr>
<td>Data Acquisition</td>
<td>500 MB Solid State Recorder, Serial Interface for GPS/INS</td>
</tr>
</tbody>
</table>

## CHAI Software

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger Modes</td>
<td>Pilot, GUI, electronic, and Lat/Long triggered acquisition</td>
</tr>
<tr>
<td>Visualization</td>
<td>3-band RGB waterfall display of real-time and recorded data</td>
</tr>
<tr>
<td>Metadata</td>
<td>Temperature, pressure, and humidity</td>
</tr>
<tr>
<td>Data Format</td>
<td>RAW, ENVI Bil, or Processed</td>
</tr>
<tr>
<td>Processing</td>
<td>EXPRESSO™</td>
</tr>
</tbody>
</table>

---

from Brandywine Electronics
Contact: John Fisher
ChaiV640 Box and IPM (Tilera Multicore Proxy for Maestro)
Software with Addition of Publisher Node Onboard IPM

Hyperspectral Instrument

ASIST

Publisher future

FLAASH Atmospheric Correction

WCPS

TlmOut

CmdIn

Geocorrection for Airborne Platforms (GCAP)

CFDP

Level 0 & Level 1 Processing

Level 2 – e.g. Spectral Angle Mapper

WCPS – Web Coverage Processing Service
CmdIn – Command Ingest
TlmOut – Telemetry Output
CASPER - Continuous Activity Scheduling Planning Execution and Replanning system
CFDP - CCSDS File Delivery Protocol
ASIST - Advanced Spacecraft Integration and System Testing Software
Data Processing Chain for Benchmarking

Main Data Source

170 Mbps

Ingest/Level 0 → Level 1R → FLAASH AC → Level 1G → WCPS

Radiometric Correction

Atmospheric Correction

Geometric Correction

Classifiers & Other Algorithms

Downlink high level data products to ground at 200 kbps

Alternative Data Sources

AMS on Citation Forest Service

GLiHT on UC-12 Langley

CHAI v640 on UC-12 Langley

EO1 ALI and Hyperion Data

AMS on Citation Forest Service

GLiHT on UC-12 Langley

CHAI v640 on UC-12 Langley

EO1 ALI and Hyperion Data

Level 2 SAM

Level 2 Vectorizer
Publisher/Consumer/GeoSocial API Architecture

Publisher

Intelligent Payload Module in S/C

Publisher

Mobile Application

Regional/Consumer Node

Web Application

API

API

API

Social Networks

[Big] Data

Societal Products

Publisher

Publisher

Publisher

Publisher

A methodology to rapidly discover, obtain and distribute satellite data products via social network and open source software

Concept developed by Pat Cappelaere (Vightel/GSFC) and Stu Frye (SGT/GSFC)
# Initial Hyperspectral Image Processing Benchmark

<table>
<thead>
<tr>
<th></th>
<th>Radiometric Correction</th>
<th>*Atmospheric Correction (FLAASH)</th>
<th>Geometric Correction (GCAP)</th>
<th>*WCPS (vis_composite)</th>
</tr>
</thead>
<tbody>
<tr>
<td>864 MHz TILEPro64</td>
<td>121.95</td>
<td>2477.74</td>
<td>183.42</td>
<td>72.39</td>
</tr>
<tr>
<td>(1 core)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>864 MHz TILEPro64</td>
<td>23.83</td>
<td>TBD</td>
<td>4.59</td>
<td>21.63</td>
</tr>
<tr>
<td>(49 cores)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2 GHz TILE-Gx36</td>
<td>57.22</td>
<td>897.71</td>
<td>28.51</td>
<td>19.93</td>
</tr>
<tr>
<td>(1 core)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2 GHz TILE-Gx36</td>
<td>9.21</td>
<td>TBD</td>
<td>1.41</td>
<td>8.72</td>
</tr>
<tr>
<td>(36 cores)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.2GHz Intel Core I7</td>
<td>2.09</td>
<td>58.29</td>
<td>0.169</td>
<td>2.26</td>
</tr>
<tr>
<td>Virtex 5 FPGA</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>

Image data: GLiHT 1004 x 1028 x 402 (829,818,048 bytes)  
Hyperion 256 x 6702 x 242 (830,404,608 bytes)  
Chai640 696 x 2103 x 283 (828,447,408 bytes)

Notes: Unit is in seconds  
TILEPro64 – No floating point support  
TILE-GX36 – Partial floating point support  
* Indicates time includes file I/O
• Worked with Spectral Sciences to modify FLAASH GLUT version to support airborne atmospheric correction.

• Optimized FLAASH to run on the multicore Tilera processor.

• Processed CHAI v640 data with FLAASH to create reflectance values

Using this subroutine which takes about 20% of processing time and is a Fast Fourier Transform to benchmark FPGA acceleration.
## FFT Benchmark Tests with Various CPU Processors and FPGA

<table>
<thead>
<tr>
<th>Processor</th>
<th>Cores</th>
<th>FFTW 1 band 128 x 256 time (Msec)</th>
<th>Clock rate (Mhz)</th>
<th>Power Consumption (watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TileGX</td>
<td>1</td>
<td>21.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TileGX</td>
<td>4</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maestro</td>
<td>1</td>
<td>187</td>
<td>200</td>
<td>14 watts</td>
</tr>
<tr>
<td>Maestro</td>
<td>8</td>
<td>55</td>
<td>200</td>
<td>14 watts</td>
</tr>
<tr>
<td>ZynqARM</td>
<td>1</td>
<td>8.7</td>
<td>667</td>
<td>3 watts</td>
</tr>
<tr>
<td>ZynqARM</td>
<td>2</td>
<td>6.9</td>
<td>667</td>
<td>3 watts</td>
</tr>
<tr>
<td>XeonPhi</td>
<td>1</td>
<td>9.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XeonPhi</td>
<td>171</td>
<td>0.221</td>
<td></td>
<td>225 watts</td>
</tr>
<tr>
<td>FPGA</td>
<td>NA</td>
<td>1.5</td>
<td>100</td>
<td>&lt;3 watts</td>
</tr>
</tbody>
</table>
Goal

• Experimenting with putting almost all of the data processing chain in FPGA using the Zynq based ZC702 (proxy for CSP) to do the benchmark
• Install ZC702 in IPM and fly on helicopter as part of our flight tests
• Issues
  – Moving data between programmable logic, processor system and memory
  – Design of data processing chain buffering scheme
• Based on DMA access, throughput speed of as much as 10 Gbps might be possible
• Would like to demonstrate producing high level data products while keeping up with an input instrument data rate of between 500 – 1000 Mbps
CHREC Space Processor (CSP) Missions

• CSP Tech Demo ISIM (Space Station)
  – 2 CSP’s
  – Targeted to be on Space Station Summer 2015
  – Gary Crum/587

• Compact Radiation BElt Explorer (CeREs) is part of NASA's Low-Cost Access to Space program
  – 3U Cubesat
  – 1 CSP
  – Launch May 2015
Conclusion

• Working towards IPM and GeoSocial API integrated architecture
• Working towards radiation tolerant IPM
• Prototype how much of the flight software and data processing software can be hosted
• Measure relative throughput performance of representative data processing chain
• Present AIST-11 effort is working mostly in multicore processor environment and only begins to explore FPGA performance