Pixels, imagers and related fabrication methods are described. The described methods result in cross-talk reduction in imagers and related devices by generating depletion regions. The devices can also be used with electronic circuits for imaging applications.

37 Claims, 5 Drawing Sheets
PIXELS, IMAGERS AND RELATED FABRICATION METHODS

STATEMENT OF GOVERNMENT GRANT

The invention described herein was made with government support under grants and contracts, and is subject to public law 96-517 (35 USC 202). In accordance with provisions of public law 96-517 (35 USC 202), the United States Government has certain rights in the invention.

FIELD

The present disclosure relates to imagers and related devices. More in particular, it relates to pixels, imagers and related fabrication methods.

BACKGROUND

FIG. 1 shows a cross sectional view of a pixel (110) used as part of a conventional four transistor (4T) pixel architecture (100). The pixel (110) comprises a P-type conducting region (140) formed in an N-type substrate (120). A pinning n+ layer (130) is also shown in FIG. 1. A combination of the pinning layer (130), the conducting region (140) and the substrate (120) forms a conventional pinned photodiode (135), as shown by a dotted line in FIG. 1.

A shallow trench isolation region (150) (STI) is further shown in FIG. 1. The STI region (150) isolates one pixel from another. The pixel (110) comprises a transfer gate (160). In operation, during an integration period when the pixel (110) is exposed to light, the transfer gate (160) is OFF and charges in the conducting region (140) are accumulated in the conducting region (140). The pixel (110) comprises also a source follower (122). The source follower (122) converts charge to output voltage.

The pixel (110) as described above is an example of conventional CMOS imagers with pinned photodiodes. Such devices when implemented in deep sub-micron technology, suffer from both reduced charge handling capacity and increased electrical cross-talk due to operation from a reduced power supply. The reduced voltage operation limits the maximum internal field and hence reduced depletion width. Both of these are responsible for increased cross-talk and limited charge handling capacity. For small pixels, lateral depletion cannot be extended due to the structure of the imager and therefore more lateral carrier diffusion due to thermal gradients, will result. The problem is more accentuated for a back-illuminated CMOS imager where the photo-generated carriers have to travel across the entire thickness of the device. In this case, there is a higher likelihood that the charges generated within the imager diffuse laterally and this results in a worse inter-pixel cross-talk.

SUMMARY

According to a first aspect, a pixel is provided, comprising: a first semiconductor layer of a first conductivity type; a second semiconductor layer of a first conductivity type, formed on the first semiconductor layer; a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type, formed on the second semiconductor layer; a fourth semiconductor layer of the first conductivity type formed on the third semiconductor layer having a first depth from a pixel front side; and a charge collection region of the second conductivity type formed within the third semiconductor layer and the fourth semiconductor layer extending vertically to a second depth from the pixel front side.

According to a second aspect, an imager is provided, comprising: a first semiconductor layer of a first conductivity type; a second semiconductor layer of the first conductivity type, deposited on the first semiconductor layer; a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type deposited on the second semiconductor layer; a fourth semiconductor layer of the first conductivity type formed on the third semiconductor layer having a first depth from a pixel front side; a charge collection region of the second conductivity type formed inside the third semiconductor layer and the fourth semiconductor layer extending vertically to a first depth from the imager front side; an insulating region formed above an imager front side; a transfer gate formed above the insulating region; and a floating region of the second conductivity type formed under the imager front side and inside the fourth semiconductor layer.

According to a third aspect, a method of carrier generation in a pixel is provided, comprising: providing a first semiconductor layer of a first conductivity type; providing a second semiconductor layer of the first conductivity type; providing a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type; providing a fourth semiconductor layer of the first conductivity type havin a first depth from an imager front side; forming the second semiconductor layer on the first semiconductor layer; forming the third semiconductor layer on the second semiconductor layer; forming a charge collection region of the second conductivity type inside the third semiconductor layer and the fourth semiconductor layer; forming the charge collection region extending vertically to a second depth from the imager front side; illuminating the pixel from either the back side or the front side; applying a first voltage level to the front side; and applying a second voltage level to the back side in such a way that all areas under the semiconductor region and the charge blocking region are depleted.

Further aspects of the present disclosure are shown in the description, drawings and claims of the present application.

BRIEF DESCRIPTION OF FIGURES

FIG. 1 shows a schematic partial cross sectional view of a known pixel architecture. FIGS. 2 and 3 show a schematic partial cross sectional view according to embodiments of the present disclosure. FIGS. 4A-4B show representations of doping profiles along different sections of the device of FIG. 3. FIG. 5 shows voltage levels corresponding to regions inside the device of FIG. 3.

DETAILED DESCRIPTION

In what follows, methods for reducing cross-talk in imagers and related devices will be described. FIG. 2 shows a cross sectional view of a device (200) comprising an imager (205) in accordance with an embodi-
ment of the disclosure, connectable, in operation, to an electronic circuit block (203). Two vertical lines XX' (201) and YY' (202) are shown in FIG. 2. The imager (205) comprises a pixel (215). The pixel (215) is a portion of the imager (205) lying between the two vertical lines (201, 202) as shown in FIG. 2.

The electronic circuit block (203) comprises electronic circuits (e.g., conventional 3L, 5T structures, digital/analog circuits, etc.). The imager (205) comprises a first semiconductor layer (210) of a first conductivity type (e.g., N), a second semiconductor layer (220) of the first conductivity type (e.g., N) and a third semiconductor layer (240) of a second conductivity type (e.g., P) opposite to the first conductivity type. The first semiconductor layer (210) has a back side (207) and the third semiconductor layer (240) has a front side (206). As shown in FIG. 2, the second semiconductor layer (220) is formed on top of the first semiconductor layer (210) and the third semiconductor layer (240) is formed on top of the second semiconductor layer (220). A fourth semiconductor layer (280) of the same type as the first semiconductor layer is formed on top of the third semiconductor layer (240) by, for example, ion-implantation or by means of epitaxial growth. The person skilled in the art will understand that the layers may be built by means of epitaxial growth and/or by ion-implantation. One may build the structure top down (280, then 240, then 220, and then 210) or bottom up, or a combination thereof.

As further shown in FIG. 2, the imager (205) further comprises a charge collection region (250) of the second conductivity type (e.g., P). The charge collection region (250) is formed within the third semiconductor layer (240) and the fourth semiconductor layer (280) (e.g., by way of implanting) extending vertically to a first depth d1 as shown in FIG. 2. According to an embodiment of the disclosure, the charge collection region is formed by using two implants, a heavier one for the electronic section (296) and the rest of the imager (205). The person skilled in the art will appreciate that the depleted region (230) is obtained by virtue of the third semiconductor region (261) of the same type as the first semiconductor region (280) a vertical depth of d2 from rest of the imager (205). The deep trench isolation region (295) borders the entire imaging array, and not each pixel. The person skilled in the art will understand that the electronic section (296) can include, for example, digital and analog circuits requiring completely different biasing conditions than those of the rest of the imager (205).

A first metal contact (292) and a second metal contact (291) are also shown in FIG. 2. The first metal contact (292) and the second metal contact (291) provide bias contacts respectively for the electronic section (296) and the rest of the imager (205). The person skilled in the art will appreciate that the deep trench isolation region (295) will provide both thermal and electrical isolation of the electronics section (296) from the rest of the imager (205). Also, by keeping the first metal contact (292) separate from the second metal contact (291), different bias voltages can be applied to the electronics section (296) and the rest of the imager (205). In this way, the electronic section (296) can be biased based on requirements of any conventional technology used to fabricate the electronics section (296) and at the same time, a different bias voltage resulting in a better performance of the imager (205) can be used to bias the rest of the imager (205). In addition, this arrangement makes the device (200) impervious to substrate noise and ground bounce resulting from a high speed operation and intermittent current fluctuations in the electronic section (296).

According to an embodiment of the disclosure, the imager (205) is configured to be illuminated from the bottom side (207). However, the person skilled in the art will understand that other variations of the imager (205) will allow illumination from the front side (206).

According to an embodiment of the disclosure, also shown in FIG. 2, doping concentrations of the second semiconductor layer (220) and the third semiconductor layer (240) are chosen such that a depleted region (230) is formed when proper bias voltages are applied to the front side (206) and the bottom side (207). As a result, the front side (206) and the bottom side (207) becomes electrically isolated, therefore, biases applied to the front side (206) and the adjacent transfer gate (275) can be completely different from that applied to the bottom side (207). As an example, while CMOS-compatible voltages (e.g., 3V) is applied to the front side (206) and the transfer gate (275), the bottom side (207) can be biased to a much larger voltage (e.g. 5V) applied via the second metal contact (291), resulting in the depleted region (230). It is understood that, depletion results in collection of carriers (holes in the case of the embodiment shown in FIG. 2) under the influence of an electric field, causing the carriers to travel vertically rather than laterally. As a result, cross-talk is significantly reduced. Simultaneously, depletion also increases the charge storage volume, and hence the charge handling capacity. According to an embodiment of the disclosure, once the depleted region (230) is generated by applying proper bias voltages, a further increase in the bias voltage applied to the bottom side (207) will result in more degree of depletion and as a result, further improvement in cross-talk can be achieved. The person skilled in the art will appreciate that the depleted region (230) is obtained by virtue of the third semiconductor layer (240).

According to an embodiment of the disclosure, as also explained later, during operation, the fourth semiconductor layer (280) will experience a higher potential than the charge collection region (250). Therefore, generated carriers (holes in case of the embodiment shown in FIG. 2), will be channeled more efficiently towards the collection region (250) which has a lower potential. Consequently, less lateral charge drift will occur and as a result, cross-talk will further improve.
The present disclosure relates to a method of generating and collecting photogenerated carriers in a pixel. A pixel includes a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, a first shallow trench isolation (STI) region formed under the pixel front side, and a first conductivity type semiconductor region bottom side; and a second STI region formed under the pixel front side, and a second conductivity type semiconductor region bottom side, wherein the second conductivity type semiconductor region is opposite to the first conductivity type. Exemplary embodiments of the pixel provide for efficient collection of photogenerated carriers in the pixel and the semiconductor region bottom side. The present disclosure may be practiced in a wide variety of applications, including imagers.
additional regions extending vertically into the third semiconductor layer and the fourth semiconductor layer.

6. The pixel of claim 5, wherein the additional regions have lighter dopings than the respective first semiconductor region and the second semiconductor region.

7. The pixel of claim 4 wherein the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, the fourth semiconductor layer, the first semiconductor region and the second semiconductor region, the charge collection region, the fourth semiconductor layer, the second semiconductor layer, the third semiconductor layer, are respectively of (n+, n—, p—, p+, n, n++, and n+) type or (p+, p—, n+, p, p++, and p+) type.

8. The pixel of claim 4 wherein: the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, the fourth semiconductor layer, the first semiconductor region and the second semiconductor region, the charge collection region and the fourth semiconductor region have respective doping concentrations of (10^{16} to 10^{17}, 10^{14} to 10^{15}, 10^{14} to 10^{15}, 10^{17} to 10^{18}, 10^{15} to 10^{16}, 10^{15} / cm^3).

9. A pixel comprising:
a first semiconductor layer of a first conductivity type; a second semiconductor layer of the first conductivity type, formed on the first semiconductor layer; a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type, formed on the second semiconductor layer; a fourth semiconductor layer of the first conductivity type formed on the third semiconductor layer having a first depth from a pixel front side; and a charge collection region of the second conductivity type formed within the third semiconductor layer and the fourth semiconductor layer and extending vertically to a second depth from the pixel front side, wherein the charge collection region is formed by using a first implant and a second implant below the first implant, the second implant having a lighter doping than that of the first implant.

10. A pixel comprising:
a first semiconductor layer of a first conductivity type; a second semiconductor layer of the first conductivity type, formed on the first semiconductor layer; a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type, formed on the second semiconductor layer; a fourth semiconductor layer of the first conductivity type formed on the third semiconductor layer having a first depth from a pixel front side; and a charge collection region of the second conductivity type formed within the third semiconductor layer and the fourth semiconductor layer and extending vertically to a second depth from the pixel front side; and a pixel back side, wherein the pixel back side is adapted to be illuminated in an operative condition of the pixel.

11. An imager comprising:
a first semiconductor layer of a first conductivity type; a second semiconductor layer of the first conductivity type, deposited on the first semiconductor layer; a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type deposited on the second semiconductor layer; a fourth semiconductor layer of the first conductivity type formed on the third semiconductor layer having a first depth from a pixel front side; a charge collection region of the second conductivity type formed inside the third semiconductor layer and the fourth semiconductor layer and extending vertically to a second depth from an imager front side; an insulating region formed above the imager front side; a transfer gate formed above the insulating region; and a floating region of the second conductivity type formed under the imager front side and inside the fourth semiconductor layer.

12. The imager of claim 11, further comprising: a first shallow trench isolation (STI) region formed under the imager front side and beside an imager first lateral side; and a second STI region formed under the imager front side and beside an imager second lateral side.

13. The imager of claim 12, wherein a first semiconductor region of the first conductivity type is formed under the pixel front side, the first semiconductor region overlying the charge collection region, extending into the fourth semiconductor layer and surrounding a first STI region side wall and a first STI region bottom side.

14. The imager of claim 13, further comprising a second semiconductor region of the first conductivity type, wherein each of the first semiconductor region and the second semiconductor region comprises an additional region of the first conductivity type, the additional regions extending vertically into the third semiconductor layer and the fourth semiconductor layer.

15. The imager of claim 14, wherein the additional regions have lighter dopings than the respective first semiconductor region and the second semiconductor region.

16. The imager of claim 13 wherein: the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, the fourth semiconductor layer, the first semiconductor region and the second semiconductor region are respectively of (n+, n—, p—, p+, n, n++, and n+) type or (p+, p—, n+, p, p++, and p+) type.

17. The imager of claim 13 wherein the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, a charge blocking region, the first semiconductor region and a second semiconductor region have respective doping concentrations of (10^{16} to 10^{17}, 10^{14} to 10^{15}, 10^{14} to 10^{15}, 10^{17} to 10^{18}, 10^{18} to 10^{19}, 10^{18} / cm^3).

18. The imager of claim 11, wherein the charge collection region is formed by using a first implant and a second implant below the first implant, the second implant having a lighter doping than that of the first implant.

19. The imager of claim 11 wherein the second depth is deeper than the first depth.

20. The imager of claim 11 wherein the imager front side is adapted to be illuminated in an operative condition of the imager.

21. The imager of claim 11 wherein an imager back side is adapted to be illuminated in an operative condition of the imager.

22. The imager of claim 11 further comprising an electronics region vertically isolated by a deep trench isolation region.

23. The image of claim 22 wherein the deep trench isolation region is extended vertically from the imager front side up to an imager back side.

24. The imager of claim 22 wherein the electronic region comprises digital and analog circuits.

25. The image of claim 22 wherein a first metal contact is provided on the imager back side isolated from a second metal contact provided on an electronics region bottom side.

26. The imager of claim 11 wherein the imager is part of a CMOS image sensor.

27. The imager of claim 11 wherein the imager is part of a CCD image sensor.

28. The imager of claim 11 wherein: the imager is part of a 3T, 4T, 5T, 6T, or 7T architecture.
29. A method of carrier generation in a pixel comprising:
providing a first semiconductor layer of a first conductivity type;
providing a second semiconductor layer of the first conductivity type;
providing a third semiconductor layer of a second conductivity type that is opposite to the first conductivity type;
providing a fourth semiconductor layer of the first conductivity type having a first depth from an imager front side;
forming the second semiconductor layer on the first semiconductor layer;
forming the third semiconductor layer on the second semiconductor layer;
forming the fourth semiconductor layer on the third semiconductor layer;
forming a charge collection region of the second conductivity type inside the third semiconductor layer and the fourth semiconductor layer, the charge collection region extending vertically to a second depth from the imager front side;
illuminating the pixel from either an imager back side or the imager front side;
applying a first voltage level to the front side;
and
applying a second voltage level to the back side in such a way that a semiconductor region in correspondence of a width of the pixel is depleted.
30. The method of claim 29 wherein the second depth is deeper than the first depth.
31. The method of claim 29, further comprising:
forming a semiconductor region of the first conductivity type under the pixel front side, the semiconductor region overlying the charge collection region and extending vertically into the fourth semiconductor layer.
32. The method of claim 31, wherein the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, and the first semiconductor region are respectively of (n+, n−, p−, p+, and n++) type.
33. The method of claim 31, wherein the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, the fourth semiconductor layer and the first semiconductor region have respective doping concentrations of (10^{16} to 10^{17}, 10^{14} to 10^{15}, 10^{15} to 10^{17}, 10^{17} to 10^{18}, 10^{18}, 10^{18} \text{cm}^{-3}).
34. The method of claim 31, wherein the first semiconductor layer, the second semiconductor layer, the third semiconductor layer, the charge collection region, a fourth semiconductor region and a first semiconductor region are respectively of (n+, n−, p−, p+, n, and n++) type.
35. The method of claim 29, wherein: the second voltage level is larger than the first voltage level.
36. The method of claim 29, wherein the first voltage level is 3V, the second voltage level is 5V and the pixel is illuminated from the back side.
37. The method of claim 29, further comprising forming a charge blocking region within the fourth semiconductor layer, wherein said second voltage level is applied in such a way that also all areas under the charge blocking region are depleted.