INORGANIC-ORGANIC HYBRID THIN-FILM TRANSISTORS USING INORGANIC SEMICONDUCTING FILMS

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ABSTRACT
Inorganic semiconducting compounds, composites and compositions thereof, and related device structures.

20 Claims, 23 Drawing Sheets
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Figure 1(A)

1. SiO$_2$

2. Nanodielectrics

3. Polymer Dielectrics: CPVP-C$_6$

Figure 1(B)

Polymer Dielectrics: CPVP-C$_6$
Figure 2(C)

Figure 2(D)
Figure 5
Figure 8A

Figure 8B

$V_0 = 100 \text{ V}$

$I_{DS}(10^3 \text{ A})$

$I_{DS}(\text{A})$

$L_0(10^{-2}\text{ A}^2/V^2)$

$V_0 (\text{ V})$

$V_0 (\text{ V})$
Figure 8G

![Graph showing the relationship between $\sqrt[12]{I_{DS} (10^{-2} A^{1/2})}$ and $n_0 (10^{12} \text{ cm}^{-2})$. The graph compares two different samples: Si/SiO$_2$/In$_2$O$_3$/Au and Si/SAS/In$_2$O$_3$/Au.](image)
Figure 13(A)

Figure 13(B)
Figure 14(A)

Figure 14(B)
INORGANIC-ORGANIC HYBRID THIN-FILM TRANSISTORS USING INORGANIC SEMICONDUCTING FILMS

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BACKGROUND OF THE INVENTION

Thin-film transistors (TFTs) pervade our daily lives as indispensable elements in a myriad of electronic/photonics products, such as computers, cell phones, displays, household appliances and sensors. Furthermore, the future demand for next-generation mobile computing, communication and identification devices is expected to increase markedly. For diverse multiple functionalities, the electronics of ideal mobile devices must achieve light weight, low power consumption, low operating voltages (powered by household batteries) and compatibility with diverse substrates. Additional desirable features include optical transparency ("invisible electronics"), mechanical ruggedness, environmental stability and inexpensive room-temperature/large-area fabrication.

TFTs meeting all the aforementioned requirements have proved elusive and will doubtless require a new direction in choice of materials and processing strategies. Conventional inorganic TFTs based on silicon and related semiconductors exhibit desirable features, such as high carrier mobilities, but are also limited by marginal mechanical flexibility and/or mandatory high-temperature processing (typically >400°C for III/V and II/VI compound semiconductors and >250°C for Si TFTs). While amorphous silicon TFTs have been fabricated on flexible plastic substrates at temperatures as low as 75-150°C, reported carrier mobilities are modest (<0.03-1 cm² V⁻¹ s⁻¹ on inorganic insulators) and the material is optically opaque. Organic semiconductor materials provide low temperature processability and are compatible with substrate flexibility, but have typically provided low field-effect mobilities. Likewise, various concerns persist relating to choice of dielectric material and corresponding fabrication technique, such concerns as can relate to choice and incorporation of any one particular semiconductor material. Such complexities and competing issues illustrate an on-going concern in the art. The search continues for a comprehensive approach to TFT fabrication, one available at low process temperatures and/or compatible with flexible plastic substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-D. Schematic views of TFTs using thin-film metal oxide semiconductors as a channel, showing In₉₀O₂ₓ as one such possible semiconductor material: (A) TFTs on doped-Si gate substrates; the dielectrics include 300 nm thermally-grown SiO₂, SAS nanodielectrics (iteratively applied, where n can be e.g., 3), and cross-linked polymer dielectrics; (B) transparent flexible TFTs using a polymer blend dielectric (see also Fig. 1G), on PET/ITO substrates; (C) TFTs, L (channel length)≈50/100 µm, W (channel width)≈5 mm, on doped Si gate substrates (left): the dielectrics are 500 nm thickly grown SiO₂, a 16.5 nm self-assembled SAS dielectric or a 20 nm CBP dielectric, and drain/source electrodes are Au thin films; fully transparent TFTs on glass/ITO substrates (right): the dielectric is a 16.5 nm self-assembled SAS dielectric, and drain/source electrodes are high-conductivity In₂O₃ thin films. (D) Molecular structure of a representative nanoscopic SAS dielectric and its component constituents.

Figs. 2E-G. Inorganic-only and inorganic-organic hybrid TFTs fabricated using In₂O₃ thin films as the n-channel semiconductor and CPB dielectric as the gate insulator: E) TFTs on doped Si gate substrates with Au drain/source electrodes; F) flexible TFTs on PET/ITO substrates with high-conductivity In₂O₃ drain/source electrodes. G) Molecular structure of a representative crosslinked polymer blend (CPB) dielectric.

Figs. 3A-C. AFM images of In₂O₃ thin films from three TFT structures: (A) p⁺-Si/SiO₂/In₂O₃; (B) n⁺-Si/(SAS nanodielectric)/In₂O₃; (C) n⁺-Si/(polymer dielectric)/In₂O₃, and (D) Hall-effect mobility versus carrier density.

Figs. 4A-B. Optical characteristics of 120 nm as-deposited In₂O₃ thin films on clean Eagle 2000 glass: (A) Optical transmittance spectrum; (B) derivation of the optical band gap.

Figs. 5. X-ray reflectivity of n⁺-Si/(SAS nanodielectric)/In₂O₃ films using an asymmetric Ge(111) compressor.

Figs. 6. Secondary ion mass spectrum (SIMS) depth profile of inorganic-organic hybrid TFTs: n⁺-Si/(SAS nanodielectric)/In₂O₃.

Figs. 7. SIMS spectra of inorganic-organic hybrid TFTs: n⁺-Si/(SAS nanodielectric)/In₂O₃. The labeling of each spectrum corresponds to the numbers in Fig. 6. Note that the peak of 69 is from Ga⁺ ion source.

Figs. 8A-G. Field-effect device characteristics of inorganic-only TFTs on p⁺ Si substrates and inorganic-organic hybrid TFTs on n⁺ Si substrates and Corning 1737F glass substrates; (A-B), Field-effect device characteristics of inorganic-only TFTs on p⁺ Si substrates: current-voltage output characteristics as a function of gate voltage (A); TFT transfer characteristics of current versus gate voltage (B) (thin-film In₂O₃ as the semiconductor (100 µm (L)x5 mm(W)) and 300 nm SiO₂ as the gate dielectric, with Au drain/source electrodes). C-D, Field-effect device characteristics of inorganic-organic hybrid TFTs on n⁺ Si substrates: current-voltage output characteristics as a function of gate voltage (C); TFT transfer characteristics of current versus gate voltage (D) (thin-film In₂O₃ as the semiconductor (50 µm (L)x5 mm(W)) and a 16.5 nm SAS dielectric with Au drain/source electrodes). E-F, Field-effect device characteristics of inorganic-organic hybrid TFTs on Corning 1737F glass substrates: current-voltage output characteristics as a function of gate voltage (E); TFT transfer characteristics of current versus gate voltage (F) (thin-film In₂O₃ as the semiconductor (100 µm (L)x5 mm(W)) and a 16.5 nm SAS dielectric with Au drain/source electrodes). G) Comparison of TFT transfer current as a function of accumulated charge-carrier density: p⁺ Si/SiO₂/In₂O₃/Au (left) and n⁺ Si/SAS/In₂O₃/Au (right). Note that inspection of the plots reveals possible contact resistance effects, indicating that performance might be enhanced by contact optimization.

Figs. 9A-C. Typical field-effect device characteristics of fully transparent inorganic-organic hybrid TFTs on Corning 1737F glass substrates. (A) Current-voltage output characteristics as a function of gate voltage; (B) TFT transfer characteristics of current versus gate voltage (thin-film In₂O₃ as the
semiconductor (100 µm (L)x5 mm(W)) and a 16.5 nm SAS 
gate dielectric on glass/ITO substrates with high-conductiv-
ity In$_2$O$_3$ drain/source electrodes; and (C) Transmission 
optical spectrum of an array of 70 transparent inorganic-
organic hybrid TFTs (glass/ITO/SAS/In$_2$O$_3$/In$_2$O$_3$ drain 
and source electrodes) taken through the In$_2$O$_3$ drain/source 
region; transmission optical spectra of glass/ITO/SAS 
glass/ITO/SAS/In$_2$O$_3$ structures are also shown for compari-
son. 

FIG. 10. Secondary ion mass spectrometric (SIMS) depth 
profile analysis of an n$^+$-Si/SAS/In$_2$O$_3$ structure.

FIGS. 11A-D. Typical field-effect characteristics of inor-
organic-organic hybrid TFTs using 60 nm thin-film In$_2$O$_3$ as 
the channel layer and a 70 nm CPB as the gate insulator on 
n$^+$-Si substrates with Au drain/source electrodes: (A) transfer 
current-voltage characteristics; (B) output characteristics as 
a function of gate voltage; typical field-effect characteristics 
of flexible inorganic-organic hybrid TFTs using 60 nm thin-film 
In$_2$O$_3$ as the channel layer and a 165 nm CPB as the gate 
insulator on PET/ITO substrates with Au drain/source elec-
trodes; (C) transfer current-voltage characteristics; and (D) output 
characteristics as a function of gate voltage. 

FIGS. 12A-C. Typical field-effect characteristics of fully 
transparent and flexible inorganic-organic hybrid TFTs using 
60 nm thin-film In$_2$O$_3$ as the channel layer and a 165 nm CPB 
as the gate insulator on PET/ITO substrates with high-con-
ductivity In$_2$O$_3$ drain/source electrodes: (A) transfer current-
voltage characteristics; (B) output characteristics as a func-
tion of gate voltage; and (C) Transmission optical spectrum of 
an array of 30 transparent inorganic-organic hybrid TFTs 
(PET/ITO/SAS/In$_2$O$_3$/In$_2$O$_3$ drain and source electrodes) 
taken through the In$_2$O$_3$ drain/source region; transmission 
optical spectrum of blank PET and normalized transmission 
optical spectrum of PET/ITO/SAS/In$_2$O$_3$ (referred to 
blank PET) are also shown for comparison. 

FIGS. 13A-B. Typical field-effect device characteristics of 
organic TFTs using a thin-film ZnO semiconductor and 
SiO$_x$ dielectric on n$^+$-Si substrates: (A) current-voltage 
output characteristics as a function of gate voltage; and (B) 
TFT transfer characteristics of current vs. gate voltage. 

FIGS. 14A-B. Typical field-effect device characteristics of 
inorganic-organic hybrid TFTs using thin-film ZnO as the 
semiconductor and cross-linked polymer dielectrics on n$^+$-Si 
substrates: (A) current-voltage output characteristics as 
a function of gate voltage; and (B) TFT transfer characteristics 
of current vs. gate voltage.

SUMMARY OF THE INVENTION 

In light of the foregoing, it is an object of the present 
invention to provide various semiconductor and dielectric 
components and/or transistor devices and related methods 
for their production and/or assembly, thereby overcoming vari-
ous deficiencies and shortcomings of the prior art, including 
those outlined above. It will be understood by those skilled in 
the art that one or more aspects of this invention can meet 
certain objectives, while one or more other aspects can meet 
certain other objectives. Each objective may not apply 
equally, in all its respects, to every aspect of this invention. As 
such, the following objects can be viewed in the alternative 
with respect to any one aspect of this invention.

It can be an object of the present invention to provide 
material components, structures and/or device configurations 
meeting the aforementioned requirements while, in addition, 
fully realizing the benefits available from TFT technologies.

It can be an object of the present invention, alone or in 
conjunction with the preceding objective, to provide an inor-
ganic semiconductor component, as can comprise but is not 
limited to a metal oxide, with favorable performance proper-
ties, including crystallinity and field-effect mobilities, as can 
be available through fabrication at or near room temperatures 
or at temperatures non-deleterious to temperature-sensitive 
substrates.

It can be an object of this invention to provide a wide range 
of organic or inorganic dielectric materials compatible with a 
variety of substrates, including organic and/or flexible sub-
strates, compatible with a variety of inorganic semiconduc-
tors (including both n- and p-type), and enable efficient 
operation of such semiconductor components.

It can be another object of the present invention, alone or in 
junction with one or more of the preceding objectives, to 
provide a dielectric component with favorable performance 
properties including but not limited to capacitance and ther-
mal stability.

It can be another object of the present invention, alone or in 
junction with one or more of the preceding objectives to 
provide various compatible combinations of such compo-
ents through the fabrication of a range of transistor configura-
tions and related device structures.

Other objects, features, benefits and advantages of the 
present invention will be apparent from this summary and the 
following descriptions of certain embodiments, and will be 
readily apparent to those skilled in the art having knowledge 
of thin film transistor devices, transistor components and 
related assembly/fabrication techniques. Such objects, fea-
tures, benefits and advantages will be apparent from the above 
as taken into conjunction with the accompanying examples, 
data, figures and all reasonable inferences to be drawn there-
from, alone or with consideration of the references incorpo-
rated herein.

In part, the present invention can be directed to a transistor 
device, such a device comprising a substrate, a dielectric 
component on or coupled to the substrate, and an inorganic 
semiconductor component. Available substrate materials 
are known in the art and include, without limitation, various 
organic or inorganic dielectric materials compatible with a 
metal oxide, as well as other inorganic materials of the sort 
discussed herein. For instance, such components can comprise 
other available Group 12 metals, Group 13 metals, Group 14 
metals, and Group 15 metals, particularly oxides thereof, as 
well as nitrides, phosphides, and arsenides thereof, as would 
be understood by those skilled in the art. In some embodi-
ments, the oxides can include two or more metals. In certain 
embodiments, the semiconductor component can include two 
or more different types of metal oxides. Alternatively, from a 
structural-functional perspective described more fully below, 
such semiconductor components can comprise a metal oxide 
providing advantageous field-effect mobilities, such mobili-

ties as can be approached through improved component crys-
tallinity and interfacial and related morphological consider-
ations of the type described herein.

Alternatively, with respect to a broader aspect of this inven-
tion, an inorganic semiconductor component can comprise 
one or more semiconducting metal or metalloid chalcogen-
ides (e.g., sulfides, selenides, tellurides), pnictides (e.g.,
precursors can include, but are not limited to, C1-3 Si(CH2)m-NH-L-(CH2)n-Si(CH3)3, (Me2N)3Si(CH2)n-Si(NMe2)n, where m is an integer in the range of 1-10 (i.e., n can be 1, 2, 3, 4, 5, 6, 7, 8, 9, or 10). As discussed more fully herein, such groups are hydrolyzable to a degree sufficient for substrate sorption or condensation or intermolecular crosslinking via siloxane bond formation under the processing or fabrication conditions employed. Similarly, the polarizable moiety can be derivatized to include similar silyl hydrolysable groups, to allow bond formation with the siloxane capping layer and/or the organic layer. In particular embodiments, the organic layers and the chromophore layers can be individually self-assembled monolayers that include the silyl or siloxane moiety, or the p-polarizable moiety.

In some embodiments, the dielectric component can comprise at least one organic dipolar layer comprising a compound comprising a p-polarizable moiety covalently bonded to or cross-linked with a siloxane bond sequence. Such compounds are illustrated in the aforementioned incorporated reference in their entirety. Further, as would be understood by those skilled in the art made aware thereof. For instance, without limitation, a halogenated, alkoxylated and/or carboxylated silyl moiety and a hydroxyl functionality. As understood in the art and explained more fully in one or more of the references incorporated herein, such a bonding sequence can derive from use of starting material compounds for the respective dielectric layers, such compounds substituted with one or more hydrolysable silicon moieties, hydrolysis of such a moiety under self-assembly conditions, and condensation with a subsequent layer starting material or precursor compound.

Precursor compounds which can be incorporated into such layers can include, for instance, bis-trichlorosilyl, octachlorotrisiloxane and (Me2N)3Si(CH2)n-Si(NMe2)n, where m is an integer in the range of 1-10, such compounds condensed one with another, with corresponding layers assembled to provide dielectric components in accordance with this invention.

While several of the aforementioned dielectric component compounds, layers and moieties are illustrated in the aforementioned incorporated reference, various other component compounds and associated moieties are contemplated within the scope of this invention, as would be understood by those skilled in the art. As understood in the art, the p-polarizable moiety covalently bonded to or cross-linked with a siloxane bond sequence. Such compounds are illustrated in the aforementioned incorporated reference in their entirety. Further, as would be understood by those skilled in the art, various other nonlinear optical chromophore compounds are described in “Supramolecular Approaches to Second-Order Nonlinear Optical Materials. Self-Assembly and Microstructural Characterization of Intrinsically Acentric” (Aminophenyl)azo-
recognized in the art, limited only by structure or functional- 
or substantially transparent source and drain contacts. As 
prise a dielectric polymeric component and optionally a sily-
transparent substrate, a transparent or substantially transpar-
ture by ion-assisted deposition (IAD) sputtering, and all TFTs 
in other embodiments, TFTs can also comprise inorganic 
material and a range of thin organic dielectrics. Alternatively, 
include poly(vinylphenol), polystyrene and copolymers 
incorporated herein by reference.

In certain embodiments, the multi-layered dielectric com-
ponent can also include one or more layers that include an 
inorganic moiety (“an inorganic layer”). The inorganic layers 
can periodically alternate among the organic layers and the 
chromophore layers, and can include one or more main group 
and/or transition metals. For example, the metal(s) can be 
selected from a Group 5 metal, a Group 4 metal, a Group 5 
metal, and a Group 13 metal. In particular embodiments, the 
main group metal(s) can be selected from a Group 13 metal 
such as, but not limited to, gallium (Ga), indium (In), and 
thallium (Tl) etc., and the transition metal can be selected 
from a Group 5 metal such as, but not limited to, iridium (Y), 
a Group 4 metal such as, but not limited to, titanium (T), 
zirconium (Zr), and hafnium (Hf), and a Group 5 metal, such 
as but not limited to, tantalum (Ta).

In some embodiments, the dielectric component can com-
prise a dielectric polymeric component and optionally a sily-
lated component comprising a moiety, e.g., an alkyl group or 
a haloalkyl group, linking two or more silyl groups having 
hydrolyzable moieties. Various other linking moieties will be 
recognized in the art, limited only by structure or functional-
ity precluding intermolecular siloxane bond and matrix for-
nation. The range of the hydrolyzable silyl groups will be 
known by those skilled in the art made aware of this invention, 
and include but are not limited to groups such as trialkoxysi-
lyl, trihalosilyl, dialkoxysilyl, dialkylhalosilyl, diha-
loalkylsilyl and dihaloalkoxysilyl. Such polymeric composi-
tions are described more fully in co-pending application Ser. 
No. 60/638,862, filed Dec. 23, 2004, the entirety of which is 
incorporated herein by reference.

In certain non-limiting embodiments, a bis(silylated) com-
ponent can comprise an alkyl moiety ranging from about C 3 
to about C 20 , linking two trialkoxysilyl groups, two trialkoxysi-
lyl groups or a combination thereof. As discussed more fully 
herein, such groups are hydrolyzable to a degree sufficient for 
substrate sorption or condensation or intermolecular crosslinking via siloxane bond formation under the process-
ing or fabrication conditions employed. Regardless, the poly-
meric component of such compositions can be selected from 
a range of such dielectric polymers otherwise used in the 
as separate gate insulator materials or layers in OTFT fabri-
cation. For purpose of example only, dielectric polymers can 
include poly(vinylphenol), polystyrene and copolymers 
thereof. In some embodiments, such polymeric compositions 
can be crosslinked. Such compositions of this invention are 
limited only by the availability of suitable silylated com-
ponents and polymeric dielectric components, the mixture 
or miscibility thereof one with another for device fabrication, 
and the resulting polymer-incorporated siloxane-bonded 
matrix/network and corresponding dielectric/insulator func-
tion.

From a device perspective, in certain non-limiting embodi-
ments, this invention can comprise various high-performance 
inorganic-organic hybrid TFTs fabricated, for example, with 
semiconducting thin-films as the n-channel or p-channel 
material and a range of thin organic dielectrics. Alternatively, 
in other embodiments, TFTs can also comprise inorganic 
dielectrics such as but not limited to SiO 2 . As shown below, 
representative In 2 O 3 films can be deposited at room tempera-
ture by ion-assisted deposition (IAD) sputtering, and all TFTs 
can be fabricated at room/near-room temperatures. Semicon-
ducting In 2 O 3 films, organic dielectrics, and TFT device 
structures were characterized in detail. It is found that inor-
ganic semiconductor components with sufficient microstruc-
tural crystallinity exhibit n-type or p-type field-effect behav-
ior, and thin organic (or, e.g. SiO 2 ) dielectric components 
with sufficient insulating properties enable ultra-low-voltage 
TFT operation. Such hybrid TFTs can show exceptionally 
large field-effect mobilities of >100 cm²/N·s at low operating 
voltages (1–2 V). Furthermore, such a fabrication approach 
is shown to be applicable to transparent flexible plastic sub-
strates, as well as other temperature-sensitive substrate mate-
rials.

As such, one aspect of the invention therefore is directed to 
a TFT device that includes a substrate (including a substrate-
gate material such as, but not limited to, doped-silicon wafer, 
tin-doped indium oxide on glass, tin-doped indium oxide on 
mylar film, and alumnum on polyethylene terephthalate), a 
dielectric material as described herein deposited on the sub-
strate substrate-gate, a semiconductor material deposited on 
the dielectric material, and source-drain contacts. In some 
eMBEDMENTS

Throughout the description, where compositions are 
described as having, including, or comprising specific com-
ponents, or where processes are described as having, includ-
ing, or comprising specific process steps, it is contemplated 
that the compositions also consist essentially of, or consist of, 
the recited components, and that the processes also consist 
essentially of, or consist of, the recited processing steps.

In the application, where an element or component is said 
to be included in and/or selected from a list of recited ele-
ments or components, it should be understood that the ele-
ment or component can be any one of the recited elements 
or components and can be selected from a group consisting 
of two or more of the recited elements or components.

The use of the singular herein includes the plural (and vice 
versa) unless specifically stated otherwise. In addition, where 
the use of the term “about” is before a quantitative value, the 
invention also includes the specific quantitative value itself, 
unless specifically stated otherwise.

It should be understood that the order of steps or order for 
performing certain actions is immaterial so long as the 
method remains operable. Moreover, two or more steps or 
actions can be conducted simultaneously.

Various embodiments of this invention can be considered 
in light of the following: dielectric and semiconductor TFT 
components, and related parameters for evaluating TFT per-
formance, such as the field-effect mobility (μ) and the drain-
source current on/off ratio (I D On/I D Off). High μ values lead 
to large drain current, fast charged/discharged capacitive loads,
high operating speeds, and thus enable wide range of applications. \( I_{ds} \) and \( I_{ds0} \) are the gate-controlled drain-source current (I_{ds0}). \( I_{ds} \) in the saturation region is expressed by Equation 1, where \( W \) and \( L \) are the channel width and length, respectively, \( V_T \) is the threshold voltage, and \( C_i \) is the dielectric capacitance per unit area. The threshold voltage \( V_T \) is defined as the \( V_G \) at which a device switches off the state to the off state, and vice versa. Ideally, \( V_T \) should be minimal (e.g., 0.0V) to minimize power consumption. \( C_i \) is expressed by Equation 2, where \( k \) is the dielectric constant, \( \varepsilon_r \) is the vacuum permittivity, and \( d \) is the dielectric thickness.

\[
I_{ds} = \frac{W_C \mu}{2 \varepsilon_r} (V_G - V_T)^2
\]

(1)

\[
C_i = \frac{k \varepsilon_0}{d}
\]

(2)

Note that for a certain device geometry, a given \( I_{ds} \) can be achieved at lower operating bias by increasing \( \mu \) in the semiconductor or increasing \( C_i \) in the dielectric. However, previous efforts have only focused on one or the other of these parameters. To simultaneously achieve a large \( \mu \) and a large \( C_i \), suitable semiconductors and dielectrics are needed, with sufficient compatibility therewith.

Metal oxides are a class of semiconductor or component materials for transparent flexible TFTs. The attraction of metal oxides includes high mobility, wide band gap, broad visible window, controllable electrical properties, and room-temperature growth. So far, metal-oxide-based TFTs have not been optimized, and the majority of metal-oxide-based TFTs demand either high growth temperatures or post-annealing treatment (usually >500°C) in order to improve the crystallinity and therefore the field-effect mobility. However, high-temperature processing prevents applications in most flexible (polymer-based) electronics. Previous metal-oxide-based TFTs fabricated at room temperature exhibit poor performance, in particular low field-effect mobilities, low \( I_{ds} / I_{g} \) ratios and large operating voltages, any of which tend to preclude most practical applications. Moreover, conventional growth techniques tend to be incompatible with practical large-area/scale deposition and device fabrication.

In \(_2\)O \(_3\) is a promising n-type material having a wide band gap (3.6–3.75 eV), high mobility as single crystals (160 cm\(^2\)V\(^{-1}\)s\(^{-1}\)), considerable transparency in the visible region (>90%), but has not been used previously to fabricate TFT devices. See, respectively, Radha Krishna, B.; Subramanyam, T. K.; Srinivasulu Naidu, B.; Utthana, S. Opt. Mater. 2000, 15, 217; Welther R. L.; Ley, R. P.; J. Appl. Phys. 1966, 37, 299; Welther, R. L.; J. Appl. Phys. 1962, 33, 2834; Wang, L.; Yang, Y.; Marks, T. J.; Liu, Z.; Ho, S.-T. Appl. Phys. Lett. In press. On the other hand, thin organic dielectrics (e.g., self-assembled multilayer and cross-linked polymer nanodielectrics) have been proved to remarkably effective in enhancing the response characteristics of organic TFT properties, while exhibiting good transparency in visible region. As demonstrated below, the efficient incorporation of inorganic In \(_2\)O \(_3\) semiconductors and thin organic dielectrics—both at room temperatures using scalable growth processes—can provide transparent flexible TFTs with high mobility, good optical transparency, and low-voltage operation.

Representative top-contact TFT device structures are shown in FIGS. 1A-B. In \(_2\)O \(_3\) thin films were deposited on inorganic dielectrics (SiO \(_2\)) and organic dielectrics by room-temperature IAD sputtering, a representative deposition technique. Organic dielectrics were fabricated on n’-doped Si (100) wafers and transparent flexible ITO/PET substrates (as the back gate; where ITO denotes tin-doped indium oxide) via either solution phase spin coating or layer-by-layer self-assembled techniques. Finally, conducting source and drain electrodes (e.g., from Au, ITO, and other suitable materials known in the art) were patterned through shadow masks, using techniques known in the art.
organic or inorganic), which is further supported by AFM; and (2) the intrinsic efficacy of the IAD growth technique to deposit smooth films.

All the present as-grown In$_2$O$_3$ films are colorless and highly optically transparent, and the films on the glass show an average transmittance of ~90% in visible region (FIG. 4A). The direct optical band gap was investigated and estimated from the linear part of the plot of (αhv)$^2$ versus $hv$ to $\alpha \sim 0$. Band gap data shows a typical value of 3.65 eV for the IAD-derived In$_2$O$_3$ films (FIG. 4B). Transmittance and band gap results suggest that In$_2$O$_3$ thin films are ideal re-channel materials for transparent TFT fabrication. The room-temperature growth process expands the application of In$_2$O$_3$ semiconductors to transparent flexible substrates.

Organic dielectrics were fabricated (e.g., self-assembled or spin-coated) by solution-phase-based growth techniques, leading to good smoothness, strong adhesion, good thermal stability, pin-hole-free and remarkable electrical insulating characteristics. For instance, self-assembled superlattice (SAS) nanodielectrics, of the type described more fully in several of the incorporated references, exhibit a large capacitance of 180 nF/cm$^2$, an effective dielectric constant of 4.7, leakage current as low as $10^{-13}$ A, and breakdown fields as high as 4 MV/cm, as determined from the capacitance measurement. As a result, thin organic dielectrics promise TFT operation at very low gate and drain-source voltages. Note that such thin organic dielectrics are mechanically/chemically robust, and careful control of the IAD growth process ensures that such dielectric materials survive the ion/plasma exposure during metal oxide deposition.

The multilayer structures and composition of the present hybrid TFTs with the device structure of n'-Si/SAS nanodielectrics/In$_2$O$_3$ were investigated by X-ray reflectivity (XRR) (FIG 5) and secondary ion mass spectroscopy (SIMS) quantitative in-depth analysis (FIGS. 6 and 7). The XRR fringe pattern persists to large $q$ values (as much as $q \sim 0.3$), qualitatively smoothing smooth interfaces of hybrid TFTs. In addition, SIMS depth profile results and spectra show these devices have abrupt In$_2$O$_3$-dielectric interfaces, minimal interfacial cross-diffusion, and phase purity. Clean interfaces in principle minimize electron traps and hysteresis, and should thereby enhance $\mu_{FE}$. Generally, weak adhesion between inorganic and organic interfaces is a significant factor degrading organic field-effect transistor performance and stability. For the present devices, the conventional 'Scotch tape' adhesion test reveals no detectable change in multilayer thickness, optical microscopic images or optical transparency before and after the test, indicating that IAD-grown In$_2$O$_3$ films on the organic dielectrics exhibit strong interfacial adhesion.

In$_2$O$_3$-based TFTs were first characterized on p+-Si substrates having a conventional SiO$_2$ dielectric, next on n+-Si substrates with the SAS and CPB dielectrics (FIGS. 8A-E), and then on glass/indium tin oxide (ITO) substrates with the SAS dielectric (FIGS. 8E-F and 5). TFT device response parameters are summarized in Table 1. The In$_2$O$_3$ devices using SiO$_2$ gate dielectrics show reasonable field-effect responses ($\mu_{FE}$=10 cm$^2$/V$^s$/s; $I_{on}/I_{off}$=10$^5$) with operating voltages in the 100 V range (FIG. 8A-B, Table 1). In contrast, inorganic-hybrid TFTs fabricated on n+-Si/SAS substrates exhibit excellent I-V characteristics (FIGS. 8C-D, Table 1) with classical/crisp pinch-off linear curves and saturation lines at very low operating voltages. Low operating voltages (~1 V) are essential for mobile electronics powered by simple household batteries.

### Table 1

<table>
<thead>
<tr>
<th>Material</th>
<th>In$_2$O$_3$ thickness (nm)</th>
<th>Dielectric thickness (nm)/C$_0$ (nF cm$^{-2}$)</th>
<th>D &amp; S electrodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. p+-Si</td>
<td>120</td>
<td>SiO$_2$/300/10</td>
<td>Au</td>
</tr>
<tr>
<td>2. n+-Si</td>
<td>60</td>
<td>SAS/16/5/180</td>
<td>Au</td>
</tr>
<tr>
<td>3. n+-Si</td>
<td>60</td>
<td>CPB/2/25/0</td>
<td>Au</td>
</tr>
<tr>
<td>4. Glass/ITO</td>
<td>60</td>
<td>SAS/16/5/180</td>
<td>Au</td>
</tr>
<tr>
<td>5. Glass/ITO</td>
<td>60</td>
<td>SAS/16/5/180</td>
<td>In$_2$O$_3$</td>
</tr>
</tbody>
</table>

Note: SAS = Self-assembled superlattice dielectric. 
CPB = Poly(4-vinylphenol) + 1,6-bis(trichlorosilyl)hexane dielectric.

**Analysis of the n+-Si/SAS/In$_2$O$_3$ device electrical response reveals large saturation-regime field-effect mobilities of ~140 cm$^2$/V$^s$/s, encouraging for high-speed applications. Such mobilities are ~10x greater than previously reported for metal oxide TFTs fabricated at room temperature, and are attributed to the following: (1) substantial crystallinity of the IAD-derived In$_2$O$_3$ semiconductor, verified by the XRD results and grain-boundary trapping model analysis (vide infra), and the resulting suppressed neutral impurity scattering, (2) very small values of the interfacial trap density ($N_t$ $\sim$ 10$^{-11}$ cm$^{-2}$), (Table 1), (3) minimal ionized-impurity scattering (the carrier concentration is ~10$^{13}$/10$^{14}$ cm$^{-3}$) (4) strong adhesion and smooth, abrupt semiconductor/dielectric interfaces to minimize electron traps and (5) advantageous characteristics of the high-capacitance organic nanoscopic dielectrics. The threshold voltage $V_T$ of the present devices is close to 0.0 V, with nearly hysteresis-free response and minimal trapped charge. These devices are generated by a positive gate bias $V_G$, verifies that In$_2$O$_3$ shows n-channel behavior. Furthermore, $I_{on}/I_{off}$ ratios of ~10$^5$ are achieved, and the maximum drain-source current reaches the mA level, sufficient for most portable circuit applications. Small subthreshold gate voltage swings of 150 mV per decade (Table 1) are achieved at the maximum slope for devices fabricated with the SAS dielectric (FIG. 8D).

To correct for the differences in the different dielectric layers (for example capacitance thickness and applied bias), the TFT transfer current characteristics are plotted versus accumulated charge carrier density (FIG. 8G). It can be seen that the n+-Si/SAS/In$_2$O$_3$/Au hybrid devices switch on at much lower accumulated charge carrier densities than the inorganic-only p+-Si/SiO$_2$/In$_2$O$_3$/Au devices, revealing that electron mobilities and charge-injection efficiency between the In$_2$O$_3$ channel and drain/source electrodes are markedly greater in the hybrid TFT case.

To further investigate the generality and applicability of the present inorganic-organic hybrid TFT strategy, In$_2$O$_3$ TFTs were next fabricated on n+-Si/20 nm CPB dielectric with Au source and drain electrodes. These n+-Si/CPB/In$_2$O$_3$ devices also have good field-effect electrical response with field-effect mobilities of ~80 cm$^2$/V$^s$/s, $I_{on}/I_{off}$ ratios of 10$^3$, and low $V_T$=0.0 V. Next, using the same fabrication techniques, hybrid TFTs were grown at room temperature on glass/IAD-
ITO/SAS gate structures with Au drain/source electrodes (FIGS. 8E-F, Table 1). Such TFTs also have excellent field-effect 1-V characteristics with large field-effect mobilities of 140 cm² V⁻¹ s⁻¹, high mobility on/off ratio of 10⁵, near 1.0 V operation with non-hysteretic characteristics, and small gate voltage swings of only 80 mV per decade.

Using high-conductivity IAD-derived In₂O₃ as drain and source electrodes affords completely transparent TFTs (FIG. 9), having field-effect mobilities of 120 cm² V⁻¹ s⁻¹, large on/off ratios of 10⁶, ~1.0 V operation, essentially hysteresis free characteristics and very small sub-threshold gate voltage swings of 90 mV per decade. Note that such small gate voltage swings (benefiting from both the high-quality In₂O₃ semiconductor and the high-capacitance organic nanoscopic dielectric) are only slightly larger than the theoretical limit for Si-based TFTs (~60 mV per decade). Estimation of the grain-boundary mobilities \( \mu_{GB} \) using a grain-boundary trapping model, provides important information on intrinsic carrier transport characteristics within a single semiconductor grain (Table 1). It can be seen that \( \mu_{GB} \) trends are in good agreement with the crystallinity results provided by XRD (FIGS. 2A-B) and that the values of \( \mu_{GB} \) are slightly larger than values of \( \mu_{EF} \), suggesting that grain-boundary scattering/trapping in these In₂O₃ films may limit \( \mu_{EF} \). That these hybrid TFTs on glass substrates are colorless and highly transparent is shown by transmission optical spectra (FIG. 9C). The transmittance of an entire 70-device TFT array (glass/ITO/SAS/In₂O₃/In₂O₃ drain and source electrodes) is >80% in the visible region, and a colourful pattern beneath the aforementioned TFT array can easily be seen.

Following a similar approach, transparent flexible hybrid TFTs fabricated with organic CPB gate dielectrics were spin-coated by solution-phase techniques at near room temperature. By using commercial available starting materials, organic CPB dielectric films with great cohesion and insulating characteristics (robust, smooth, conformal, pin-hole-free, thermally stable) can be deposited on a variety of rigid and flexible substrates. Structures, components, and processes relating to such hybrid TFTs are shown in FIGS. 1E-G. The device structures, and electrical properties, were characterized as described below. Such hybrid TFTs exhibit excellent field-effect characteristics on Si substrates, and this fabrication approach is applicable to plastic substrates—e.g., PET to realize flexible “invisible” TFTs with good performance.

The microstructures and surface morphologies of an In₂O₃ channel layer in such present hybrid TFTs were characterized by X-ray diffraction (XRD) 6-20 scans and contact-mode atomic force microscope (AFM), respectively (FIGS. 2C and 3C). Obviously, In₂O₃ films possesses the characteristic cubic bixbyte structure with (100)-series orientation and considerable crystallinity/texture even when grown on n⁺-Si/CPB at room temperature, evidenced by the narrow XRD peak width. AFM images show the In₂O₃ thin films grown on n⁺-Si/CPB to be compact, dense, and uniform, exhibiting relatively small RMS surface roughnesses of 3.3±0.2 nm on n⁺-Si/CPB substrates and 6.9±0.3 nm on PET/ITO/CPB substrates. Note that n⁺-Si surface morphologies (RMS roughness: ~0.1 nm) are much smoother PET surface (RMS roughness: ~2.2 nm), which to some extent contribute to In₂O₃ rough surfaces on plastic substrates. The multilayer structural and compositional characteristics of the present hybrid TFTs were investigated on n⁺-Si/CPB/In₂O₃ structures by secondary ion mass spectrometric (SIMS) depth-profiling (FIG. 10). The SIMS results show that these multilayer devices have clear channel/dielectric and dielectric/gate interfaces, and minimal interfacial cross-diffusion. Clear channel/dielectric interfaces no double minimize electron traps and hysteresis effect, and thus lead to large \( \mu_{EF} \). The conventional “Scotch tape” adhesion test was carried out to inspect the interfacial adhesion at each interface. No detectable change was found in the thickness, optical microscopic images, and optical transparency before and after the test, revealing that both CPB/In₂O₃ and gate/CPB interfaces possess strong interfacial adhesion.

The \( \mu_{EF} \) in the saturation region is calculated using Equation 1, above; grain-boundary mobilities \( \mu_{GB} \) and the interfacial trap densities \( N_s \) between the semiconductor and dielectric were computed by plotting \( \ln(I_{DS}/V_s) \) at a given drain-source voltage according to Equation 3 (the grain boundary trapping model); the subthreshold voltage swings are obtained at the maximum slope of \( dV_g/d(\log I_{DS}) \) based on Equation 4.

\[
I_{DS} = \frac{W_{REF}V_{DS}C_vG_{VDSS}V_{G}}{L} \exp \left( -\frac{qV_s^2}{3k_BT}\right)
\]

\[
S = \frac{dV_g}{d(\log I_{DS})}
\]

where \( q \) is the electron charge, \( t \) is the channel thickness, \( E \) is the In₂O₃ permittivity, \( k \) is the Boltzmann constant, and \( T \) is the absolute temperature at room temperature. In₂O₃ based TFTs were first characterized on n⁺-Si/CPB substrates, and then on PET/IAD-ITO/CPB substrates (FIGS. 1E-F). TFT device response parameters are summarized in Table 2.

<table>
<thead>
<tr>
<th>Gate</th>
<th>Thickness (nm)</th>
<th>Dielectric Thickness (nm²/cm²)</th>
<th>D &amp; S Electrodes</th>
<th>( \mu_{EF} ) (cm²/V·s)</th>
<th>( \mu_{GB} ) (cm²/V·s)</th>
<th>( I_{on}/I_{off} )</th>
<th>( V_T ) (V)</th>
<th>( N_s ) (cm⁻²)</th>
<th>( S ) (V/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n⁺-Si</td>
<td>60</td>
<td>70/100</td>
<td>Au</td>
<td>160</td>
<td>171</td>
<td>10⁴</td>
<td>0.21</td>
<td>9.1 x 10¹⁴</td>
<td>0.24</td>
</tr>
<tr>
<td>PET/ITO</td>
<td>60</td>
<td>160/30</td>
<td>Au</td>
<td>20</td>
<td>26</td>
<td>10³</td>
<td>0.12</td>
<td>2.9 x 10¹⁰</td>
<td>2.78</td>
</tr>
<tr>
<td>PET/ITO</td>
<td>60</td>
<td>160/30</td>
<td>In₂O₃</td>
<td>20</td>
<td>26</td>
<td>10³</td>
<td>0.23</td>
<td>3.5 x 10¹⁰</td>
<td>2.98</td>
</tr>
</tbody>
</table>

The inorganic-organic hybrid TFTs fabricated on n⁺-Si/CPB substrates exhibit remarkable I-V characteristics (FIGS. 11A and 11B) at very low operating biases (1-2 V) with classical/crisp pinch-off linear curves in the linear region and steady/flat lines in the saturation region. Owing to In₂O₃ substantial crystallinity, small interfacial trap densities between channel layers and dielectric layers (Table 2), and advantages of the inorganic-organic hybrid TFT structure, large saturation regime field-effect mobilities of ~160 cm²/V·s were obtained in n⁺-Si/SAS/In₂O₃/Au devices. This large
value represents the highest field-effect mobility in room-temperature TFTs and thus is very promising for high-speed electronics. The threshold voltage $V_T$ of the present devices is only 0.21 V with nearly hysteresis-free response, reflecting that In$_2$O$_3$ exhibits n-channel materials behavior. Furthermore, $I_{on}/I_{off}$ ratios of $10^4$ are achieved, and the maximum drain-source current reaches the mA level, a sufficient value for most portable circuit applications. Small sub-threshold gate voltage swing of 240 mV/decade (Table 2) is achieved at the maximum slope of the current-voltage output curve (FIG. 11A).

To further explore the versatility and demonstrate the transparency and flexibility of the present inorganic-organic hybrid TFT strategy, In$_2$O$_3$ TFTs were next fabricated on PET/IAD-ITO/PET gate structures at room temperature with Au drain/source electrodes (FIGS. 11C and 11D). These TFTs also exhibit excellent field-effect non-hysteretic I-V characteristics, with large field-effect mobilities of $\sim 20 \text{ cm}^2/\text{V s}$, $I_{on}/I_{off}$ ratio of $10^5$, with moderate operating voltage and gate voltage swing being 10 V and 2.78 V/decade, respectively.

High-conductivity IAD-derived In$_2$O$_3$ drain and source electrodes afford completely transparent TFTs (FIGS. 12A-C), having substantial field-effect mobilities of $\sim 10^5 \text{ cm}^2/\text{V s}$, on/off ratios $>10^5$, sub-threshold gate voltage swings of 2.98 mV/decade, and essentially hysteresis-free characteristics. Computed with the grain boundary trapping model (Equation 3), the grain boundary mobilities $\mu_{gb}$ and the interfacial trap densities $N_t$ reveal important information on intrinsic carrier transport and trapping characteristics (Table 2), and explain the differences of aforementioned TFT performance on two substrates (silicon and PET). It can be seen that the grain boundary mobilities on PET are much smaller than that on silicon substrates, and qualitatively agree with the field-effect mobility results, reflecting that In$_2$O$_3$ texture/crystallinity are modest on PET which in turn leads to somewhat lower field-effect mobilities on PET. On the other hand, the value of interfacial trap densities on PET is found to be greater than that on silicon substrates, which also partially explains the smaller mobilities on PET. Intrinsically, the large interfacial trap density is usually caused by rougher morphology, substrate/film mismatch (e.g. density, thermal expansion, hardness), unoptimized processing procedure, and thereby affects TFT properties, especially the field-effect mobility.

The bending effect on flexible TFTs was investigated by bending these flexible TFTs into a curve. No significant changes or residual effects were observed when the bending radius of curvature is as low as 4 cm. That these hybrid TFTs on plastic substrates are colorless and highly transparent is shown by transmission optical spectra and the photo image (FIG. 12C), where the transmittance of an entire 30-device TFT array (PET/ITO/CPB/In$_2$O$_3$/In$_2$O$_3$ drain and source electrodes) is ~80% in the visible region.

As demonstrated, representative inorganic-organic hybrid TFTs have been fabricated at room temperature using IAD-derived high-quality semiconducting In$_2$O$_3$ and organic spin-coatable polymer gate dielectrics. On silicon substrates, the TFTs exhibit field-effect mobilities up to 160 cm$^2$/V s, $I_{on}/I_{off}$ $10^5$, sub-threshold gate voltage swings of 240 mV/decade and function at $\sim 2.0$ V. Integrated with PET substrates and transparent drain/source electrodes, optical transparency and mechanical flexibility can be achieved as well as other good field-effect characteristics. Furthermore, the present TFT devices are obtained by large-scale/area fabrication techniques (scalable patterning organic semiconductor and simple spin-coatable organic dielectric process) and of all transparent components with good bendability, and thus represent a promising pathway for flexible “invisibles” electronics.

To further demonstrate the generality of the present inorganic-organic hybrid approach, ZnO-based TFTs were fabricated on p'-Si/SiO$_2$ and n'-Si/polymer dielectric at near-room temperature. Clear field-effect responses were observed for ZnO-based TFTs with complete light- and air-stability. (See, Table 1, example 2 and FIGS. 12A-B). The results on ZnO-based TFTs further support that such a hybrid approach can be extended to the use of various other semiconducting metal-oxide materials.

Such results demonstrate that hybrid integration of an oxide semiconductor, as illustrated by representative In$_2$O$_3$ and nanoscopic organic dielectrics provides room-temperature fabricated transparent TFTs with performance unobtainable via conventional approaches. Such a hybrid TFT strategy is applicable to other oxide-based TFT structures (bottom source-drain contacts, top gate, etc.), as well as to other wide-bandgap metal oxide semiconductors and to other transparent ultrathin organic dielectrics. Furthermore, these hybrid devices are compatible with large-scale/area deposition techniques and simple dielectric growth processes, and are transparent—a promising approach to high-performance, transparent electronics.

**EXAMPLES OF THE INVENTION**

The following non-limiting examples and data illustrate various aspects and featuring related to the components/devices and/or methods of the present invention including the fabrication of thin film transistor devices comprising various semiconductor and dielectric components, as are available through the fabrication techniques described herein. In comparison with the prior art, the present components/devices and/or methods provide results and data which are surprising, unexpected and contrary thereto. While the utility of this invention is illustrated through the use of the components/device configurations, they will be understood by those skilled in the art that comparable results are obtainable with various other components, devices or configurations thereof as are commensurate with the scope of this invention.

**Example 1**

**TFT Fabrication.** In$_2$O$_3$ thin films were deposited on p'-Si/SiO$_2$ (Process Specialties, Inc.), n'-Si/polymer dielectric (n'-Si from Process Specialties, Inc.), n'-Si/crosslinked polymer blend dielectric, and PET/ITO (crosslinked polymer blend dielectric) (ITO/PET, (R$_{sheet}$=800Ω)), from CPFilms Inc., and IAD-derived glass/ITO (Corning 1737I glass substrates from Precision Glass & Optics; the ITO gate was deposited by IAD at room temperature; sheet resistance=60Ω as the back gate. The nanoscopic organic gate dielectrics (SAAS, three 5.5 nm layers of type III; CPB, 20 nm prepared from poly-4-vinylphenol1+1,6-bis(trichlorosilyl)hexane) were grown via layer-by-layer assembly or spin-coating, as provided in the references incorporated herein. Poly-4-vinylphenol and 1,6-bis(trichlorosilyl)hexane were purchased from Aldrich and Gelest, respectively.

In$_2$O$_3$ films were grown with a Veeco horizontal dual-gate IAD system at room temperature. The In$_2$O$_3$ target (99.99%) was purchased from Plasmametrics. During the semiconducting In$_2$O$_3$ deposition process, the growth system pressure and O$_2$ partial pressure were optimized at 4.0x10$^{-4}$–4.4x10$^{-4}$ torr and 2.2x10$^{-4}$–2.6x10$^{-4}$ torr, respectively. The growth rate of the In$_2$O$_3$ thin films was 3.2±0.2 nm min$^{-1}$. During the In$_2$O$_3$
An example of the text: "...between the drain and source electrodes, the growth system pressure and O₂ partial pressure were at 2.7x10⁻⁴ torr and 0.4x10⁻⁴ torr, respectively. The conductivity of the In₂O₃ drain and source electrodes was measured to be 1,400 S cm⁻¹ by a four-probe technique. The ITO films were deposited using the same IAD growth system at room temperature. The ITO target (In₂O₃/SiO₂=9:1) was purchased from Sputtering Materials, and the ITO growth process details have been reported elsewhere.

A top-contact electrode architecture was used in TFT device fabrication. The 50 nm Au source and drain electrodes were deposited by thermal evaporation (pressure ~10⁻⁴ torr) through shadow masks, affording channel dimensions of 50/100 μm (L x 5 mm W). Alternatively, 150 nm In₂O₃ source and drain electrodes were deposited by IAD through the same shadow masks for completely transparent TFTs. The top-contact Si/SiO₂/In₂O₃/Au, Si/SAS/In₂O₃/Au and glass/ITO/SAS/In₂O₃/Au or In₂O₃) TFT device structures are shown in FIG. 1. Further details concerning organic dielectric growth and device fabrication are provided in the aforementioned incorporated references and are also reported in the literature. See Yoon, M. H.; Fanfetti, A.; Marks, T. J. Am. Chem. Soc. 2005, 127, 10388.

Example 2

Characterization. In₂O₃ film thicknesses were verified using a Tencor P-10 step profiler by etching a step following film growth. XRD 0-20 scans of In₂O₃ were acquired with a Rigaku DMAX-A diffractometer using Ni-filtered Cu Kα radiation. Optical transmittance spectra were acquired with a Cary 500 ultraviolet-visible-near-infrared spectrophotometer and were referenced to the spectrum of uncoated Corning 1737F glass. Film morphology images were imaged on a Digital Instruments Nanoscope III AFM. Quantitative SIMS analysis was carried out on a MATS quadrupole SIMS instrument using a 15 keV Ga⁺ ion source. Conductivities of the semiconducting In₂O₃ thin films were measured with a Keithley 2182A nanovoltmeter and 6221 current source. The electrical properties of highly conductive ITO and In₂O₃ films were characterized on a Bio-Rad HL5500 van der Pauw Hall-effect measurement system. TFT device characterization was carried out on a customized probe station in a typical field-effect I-V characteristics (FIG. 13A) with classical linear and pinch-off saturation lines. ZnO TFTs show a field-effect mobility of 0.02 cm²/V·s and drain current on/off ratio of ~10⁴, respectively, with great light- and air-stability when exposed to ambient environment.

The invention claimed is:

1. A metal oxide thin film transistor device comprising a substrate, a gate conductor, source-drain contacts, and an inorganic-organic hybrid thin film composition comprising an inorganic semiconductor layer coupled to an organic layer, wherein the inorganic semiconductor layer is a channel layer and comprises a metal oxide comprising indium.

2. The device of claim 1, wherein the inorganic semiconductor layer comprises a metal oxide comprising indium and one or more metals independently selected from a Group 12 metal, a Group 13 metal, and a Group 14 metal.

3. The device of claim 1, wherein the organic layer comprises a polymeric component, a π-polarizable component, or a combination thereof.

4. The device of claim 1, wherein the organic layer comprises hydroxylatable moieties.

5. The device of claim 1, wherein the organic layer comprises a π-polarizable component that is coupled to at least one of a silyl moiety and a siloxane moiety.

6. The device of claim 5, wherein the organic layer comprises a π-polarizable component comprising a polymer selected from poly(vinylphenol), polystyrene, and copolymers thereof.

7. The device of claim 5, wherein the organic layer comprises a π-polarizable ensemble, the polymer blend comprising a π-polarizable component and a component promoting substrate sorption, condensation, or intermolecular crosslinking.

8. The device of claim 5, wherein the organic layer comprises a π-polarizable component comprising a non-linear optical chromophore.

9. The device of claim 5, wherein the π-polarizable component comprises a multi-layered composition, the multi-layered composition comprising periodically alternating layers of different materials.

10. The device of claim 5, wherein at least some of the periodically alternating layers are coupled to an adjacent layer by a coupling layer comprising a siloxane matrix.
12. The device of claim 1, wherein the substrate comprises a transparent material and is coupled to the inorganic-organic hybrid thin film composition.

13. The device of claim 12, wherein the device is a completely transparent thin film transistor device.

14. The device of claim 1, wherein the substrate comprises a flexible plastic material and is coupled to the inorganic-organic hybrid thin film composition.

15. The device of claim 14, wherein the device is bendable up to a bending radius of curvature of about 4 cm without residual effects.

16. The device of claim 1, wherein the inorganic semiconductor layer is physically adhered to the organic layer.

17. The device of claim 1, wherein the inorganic semiconductor layer is physically adhered to the organic layer by adsorption.

18. The device of claim 1, wherein the organic layer is chemically bonded to the inorganic semiconductor layer.

19. The device of claim 1, wherein the device operates at an operating voltage \( V_{op} \) between about 1 V and about 20 V.

20. The device of claim 1, wherein the device exhibits a field-effect mobility of greater than about 100 cm\(^2\)V\(^{-1}\)s\(^{-1}\) at an operating voltage \( V_{op} \) between about 1 V and about 2 V.

* * * * *