Ni-$BaTiO_3$-Based Base-Metal Electrode (BME) Ceramic Capacitors for Space Applications

David (Donhang) Liu, Sr. Staff Engineer II
301-286-8573; donhang.liu-1@NASA.gov

Lou Fetter, Task Manager
301-286-8339; lula.r.fetter@nasa.gov

Bruce Meinhold, Group Lead
301-286-1494; bruce.meinhold@nasa.gov

ASRC Federal Space and Defense

Work performed for the Parts, Packaging, and Assembly Technology Branch, Code 562

NASA Goddard Space Flight Center

Greenbelt, Maryland

To be presented by Donhang (David) Liu at the 2015 Components for Military and Space Electronics (CMSE) Conference and Exhibition, Los Angeles, CA, March 1-3, 2015.

Acronyms

AEC-Q200	Automotive Electronics Council standards for automotive electronic components, Section Q200: passive components
Ag	Silver
ASTM	American Society for Testing and Materials
BME	Base-Metal Electrode
CMSE	Components for Military and Space Electronics
Cu	Copper
CV	Capacitance x Voltage
DLA	Defense Logistics Agency
DLA	Defense Logistics Agency
EIA/ECA	Electronic Industries Alliance/Electronic Components Association
ESCC	European Space Component Coordination
GSFC	Goddard Space Flight Center
MLCC	Multi-Layer Ceramic Capacitor
NEPP	NASA Electrical Parts and Packaging Program
Ni	Nickel
Pd	Palladium
PDC	Product Development Certification
PME	Precious-Metal Electrode
PRVT	Processing Reliability Verification Test
QPLD	Qualified Parts List Directory
SCD	Source Control Drawing
SEM	Scanning Electron Microscopy

Presentation Outline

- Background of Base-Metal Electrode (BME) Technology
- Rationale for Adopting BME Technologies
- NASA GSFC S-311-P-838
  - Basis for specification
  - Product highlights
  - Product Development Inspections
    - Processing Reliability Verification Test (PRVT)
    - In-Process Inspection
    - Group A Inspection
    - Group B Inspection
- Summary

Background of BME Technology

- All Multi-Layer Chip Capacitors (MLCC) for high-reliability applications are fabricated using precious metal electrodes (PME), Palladium (Pd)/ Silver (Ag) with minimum dielectric thickness and maximum dielectric constant restrictions.
- High materials cost plus questionable supply assurance forced commercial industry to shift from PME to BME (Nickel (Ni), Copper (Cu)) technology.
  - Change from PMEs to BMEs was totally driven by economics.
- Current designs require higher Capacitance x Voltage (CV) value and lower rated voltage Multi-Layer Ceramic Capacitors (MLCCs).
  - PME capacitor values inadequate for many requirements
  - BME capacitors meet design requirements but violate the minimum dielectric thickness requirement
- Use of BME MLCCs for military/space applications requires new specifications.

Rationale for Adopting BME Technologies

- BME is not a new technology; used for >30 years
- 99% of MLCCs manufactured worldwide use BME technology
  - Lion's share of research activity and technical support is for BME
  - Wide selection of products with short lead time
  - Low cost
- Select BME capacitors are ready for space-level applications
  - Significant improvements in processing quality and control
  - BME technology widely used in harsh automotive environments and challenging medical applications
  - Several hybrid manufacturers are using BME capacitors in space-level products
- European Space Component Coordination (ESCC) BME capacitor specification for space programs to be finalized March 2015
- MIL-PRF-Thin Dielectric Specification is under development by G11/G12 and Defense Logistics Agency (DLA)

NASA GSFC S-311-P-838

- Goddard Space Flight Center (GSFC) Source Control Drawing (SCD) for BME capacitors
- Basis for SCD:
  - MIL-PRF-123 for PME capacitors
  - MIL-PRF-55681 for PME capacitors
  - GSFC EEE-INST-002 requirements for ceramic capacitors
  - Preliminary ESCC Specification – to be finalized March 2015
  - GSFC S-311-P-829, SCD for PME MLCCs with smaller EIA chip sizes less than 0805 and with thinner dielectric layers (~8 μm)
  - Automotive Electronics Council standards for automotive electronic components, Section Q200: passive components (AEC-Q200) for automotive grade BME MLCCs
  - NASA NEPP-funded studies on BME MLCC reliability and failure mechanisms

S-311-P-838 Product Highlights

- Chip Size from 0603 to 1812
- Minimum dielectric layer thickness: 7.11μm (0.28 mil)
- Voltage Range from 16V to 100V
- X7R Dielectric

Table II. Allowable Capacitance/Voltage Combinations				
Component Size	Capacitance Range (pF)	Rated Voltage (V_R)	Minimum Dielectric Thickness 1/ in µm (mils)	Tolerance (+/-) (%)
0603	2,200 to 18,000	100	15.24 (0.6)	5, 10, 20
0603	2,200 to 150,000	50	8.38 (0.33)	5, 10, 20
0603	2,200 to 180,000	16, 25	7.11 (0.28)	5, 10, 20
0805	2,200 to 100,000	100	15.24 (0.6)	5, 10, 20
0805	2,200 to 470,000	50	8.38 (0.33)	5, 10, 20
0805	2,200 to 1,000,000	16, 25	7.11 (0.28)	5, 10, 20
1206	18,000 to 390,000	100	15.24 (0.6)	5, 10, 20
1206	18,000 to 1,000,000	50	8.38 (0.33)	5, 10, 20
1206	18,000 to 2,200,000	16, 25	7.11 (0.28)	5, 10, 20
1210	47,000 to 820,000	100	15.24 (0.6)	5, 10, 20
1210	47,000 to 1,000,000	50	8.38 (0.33)	5, 10, 20
1210	47,000 to 1,000,000	16, 25	7.11 (0.28)	5, 10, 20
1812	150,000 to 2,200,000	100	15.24 (0.6)	5, 10, 20
1812	150,000 to 4,700,000	50	8.38 (0.33)	5, 10, 20
1812	150,000 to 8,200,000	16, 25	7.11 (0.28)	5, 10, 20

1/ Thickness measured after firing

Product Development Certification Inspections

<u>Four Required Inspections</u>

1. Processing Reliability Verification Test (PRVT)
   - Uses construction and microstructural parameters to estimate long term reliability.
2. In-Process Inspection
   - Internal examination to verify lot construction
3. Group A Inspection
   - Screening of 100% capacitors supplied to specification
4. Group B Inspection with Product Development Certification (PDC) requirements
   - Is required for each capacitance/voltage/size combination to be approved per this specification.
   - Group B PDC Requirements include enhanced Life, Temperature-Humidity Bias, and Breakdown Voltage Tests.

Processing Reliability Verification Test

- Pre-screening lot acceptance test
  - Cross-section samples from side of capacitor body to reveal end margins
  - Use Scanning Electron Microscopy (SEM) to make at least three measurements of the parameters in the following table.

Parameter	Measurement	Requirement
Dielectric Thickness	Sample Average	>50Vdc: 7.11µm (0.28 mils) min.
Side Margin	Sample Average	<25V: 15µm (0.6 mils) min. ≥25V: Per EIA/ECA-469, Table 6
End Margin	Sample Average	<25V: 25µm (1 mil) min. ≥25V: Per EIA/ECA-469, Table 7
Cover Plate Thickness	Sample Average	<25V: 25µm (1 mil) min. ≥25V: Per EIA/ECA-469, Table 8
Dielectric Layers	Measurement	≤ 300 layers

  - Uses wet or dry chemical etch to reveal dielectric structure and measure average grain size using Linear Intercept Method per American Society for Testing and Materials (ASTM) E112-10 section 13.

Processing Reliability Verification Test

To meet the PVRT requirement and qualify the lot, the capacitor samples shall meet the following equation for *initial reliability* $\bar{R}_i$

$$\bar{R}_i = \left[1 - \left(\frac{\bar{r}}{d}\right)^{\alpha}\right]^{N} > 0.99999$$

where $\bar{r}$ = measured average grain size

d = average dielectric thickness

N = total number of dielectric layers

α = 5 for capacitors rated > 100V

α = 6 for capacitors rated ≤ 100V

- D. Liu, "How to Characterize the Reliability of Ceramic Capacitors with Base-Metal Electrodes." Components for Military and Space Electronics (CMSE) 2015 Presentation 6-1
- D. Liu, "A General Reliability Model for Ni-$BaTiO_3$-Based Multilayer Ceramic Capacitors." CARTS Proceedings, p. 31-44, (2014)
- D. Liu and M. Sampson, "Some Aspects of the Failure Mechanisms in $BaTiO_3$-Based Multilayer Ceramic Capacitors." CARTS Proceedings, p. 59-71, (2012)

In-Process and Group A Inspections

- In-Process Inspection

  Required for each capacitor lot supplied to this specification.

  - Nondestructive internal examination per MIL-PRF-123 para. 4.6.1 (ultrasonic)
  - Destructive Physical Analysis (pre-termination) per MIL-PRF-123 para. 3.6.

- Group A Inspection

  Required on 100% of capacitors supplied to this specification.

Group A Inspection Tests
Thermal Shock (Conditions: -55°C to +125°C, 20 cycles 20)
Voltage Conditioning (Conditions: 2x rated voltage, 168 hrs. min., +125°C)
Insulation Resistance at +125°C
Dielectric Withstanding Voltage
Insulation Resistance at +25°C
Capacitance
Dissipation Factor
Percent Defective Allowable (PDA) (Requirement 5% max.)
Visual Inspection

Group B Inspection

Group B Inspection with PDC requirements

Required for each lot of capacitor supplied to this specification.

Group B Inspection Tests	Quantity (Accept Number)
Subgroup 1	45 or 125 (0)
Thermal Shock	Note: If dielectric thickness is ≥ 20.3 μm (0.8 mils), quantity is 45. If dielectric thickness is < 20.3 μm (0.8 mils), quantity is 125
Life Test	
Insulation Resistance (at 125°C)	
Dielectric Withstanding Voltage	
Insulation Resistance (at +25°C)	
Capacitance	
Dissipation Factor	
Subgroup 2	12(0)
Temperature Humidity Bias	
Subgroup 3	6(0)
Solderability	

Group B Inspection Tests (cont.)	Quantity (Accept Number)
Subgroup 4	6(0)
Insulation Resistance (at +25°C)	
Capacitance	
Dissipation Factor	
Resistance to Soldering Heat	
Insulation Resistance (at +25°C)	
Capacitance	
Dissipation Factor	
Subgroup 5	6(0)
Shear Stress	
Subgroup 6	12(0)
Breakdown Voltage Test	
Subgroup 7	6(0)
Board Flex Test	

Conditions/Requirements

Thermal Shock:	-55°C to 125°C, 100 cycles
Life Test:	2x rated voltage, +125°C, 1000 hrs. (PDC 4000 hrs.)
Temperature Humidity Bias:	96 hrs min. (PDC 1000 hrs. min.)
Breakdown Voltage PDC:	Sample size of 30 pieces.

Summary

- Select BME capacitors are ready for military and space applications.
- NASA GSFC S-311-P-838 specification provides framework for BME capacitor approval for space.
  - Pre-screening lot tests (PVRT testing) in S-311-P-838 ensures reliable part construction, improving chance of successful completion of screening and lot acceptance.
- ESCC specification for BME capacitors to be finalized in March 2015.
  - The NASA and ESCC specifications have comparable requirements