A DC-DC converter for generating a DC output voltage includes: a digitally controlled pulse width modulator (DPWM) for controlling a switching power stage to supply a varying voltage to an inductor; and a digital voltage feedback circuit for controlling the DPWM in accordance with a feedback voltage corresponding to the DC output voltage, the digital voltage feedback circuit including: a first voltage controlled oscillator for converting the feedback voltage into a first frequency signal and to supply the first frequency signal to a first frequency discriminator; a second voltage controlled oscillator for converting a reference voltage into a second frequency signal and to supply the second frequency signal to a second frequency discriminator; a digital comparator for comparing digital outputs of the first and second frequency discriminators and for outputting a digital feedback signal; and a controller for controlling the DPWM in accordance with the digital feedback signal.
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FIG. 2B
FIG. 3B
Supply triangular waveform to device under test (DUT)

Measure voltage waveform across DUT

Compute inductance of DUT from voltage waveform

Compute resistance of DUT from voltage waveform

Configure driving circuitry based on computed inductance and resistance

FIG. 8
Triangular Voltage: 1.1V-2.2V

Analog Output Difference Voltage ($V_{DIFF}$)
LOW-TO-MEDIUM POWER SINGLE CHIP
DIGITAL CONTROLLED DC-DC
REGULATOR FOR POINT-OF-LOAD
APPLICATIONS

CROSS-REFERENCE TO RELATED
APPLICATION(S)

This non-provisional application claims the benefit of U.S.
Provisional Application No. 61/425,126, filed on Dec. 20,
2010.

STATEMENT REGARDING FEDERALLY
SPONSORED RESEARCH OR DEVELOPMENT

The invention described herein was made in the
performance of work under a NASA contract, and is subject to the
provisions of Public Law 96-517 (35 U.S.C. §202) in which
the Contractor has elected to retain title.

BACKGROUND

Embodiments of the present invention are directed to the
field of DC-DC conversion circuits.

DC-DC converters such as buck (step-down) converters,
boost (step-up) converters, and buck-boost converters, use
inductors as a storage element to perform the DC-DC
conversion. In addition, DC-DC converter designs also include a
current sense resistor for short circuit detection, multi-stage
converter load balancing, thermal control, and current
independent control. More recently, the inductor DC resistance
(DCR) may be used instead of a separate current sense
resistor to reduce circuit complexity and reduce losses. However,
the DCR value as reported by a data sheet often deviates by
+/−15% or more from the actual DCR value of the inductor. In
addition, temperature effects can also influence the resistance
of the inductor.

The characteristics of the driving waveforms applied to the
DC-DC converter for generating various output DC voltages
generally depend on the inductance value of the inductor. As
such, a DC-DC converter is typically designed to operate in
conjunction with an inductor having an inductance within a
particular, predetermined range. In addition, the DCR (or the
temperature profile of the DCR) of the inductor is generally
assumed to be relatively constant over the life of the device.

SUMMARY

Aspects of embodiments of the present invention are
directed to a DC-DC converter which provides a digital feed-
back signal to control the DC output.

Other aspects of the present invention are directed to a
DC-DC converter which includes a built-in-self-test (BIST)
circuit for measuring, with good accuracy, the inductance and
series DC resistance (DCR) of an inductor in the circuit and
methods for measuring an inductance and series DCR of an
inductor in the circuit during the start-up of the DC-DC
converter.

Aspects of embodiments of the present invention are also
directed to a digitally controlled single chip solution, making
high switching frequency and high resolution applications
possible, and having a high accuracy, low complexity, on-line
inductor characterization circuit to enable: current mode con-
trol; lossless average current sensing using the DCR of the
inductor; and flexible, time-efficient, and analog friendly
design capabilities using field programmable gate array
(FPGA) proportional integral-derivative (PID) register-trans-
fer level (RTL) code.

An all-digital controlled DC-DC switching converter that
provides a stable DC output voltage from an unregulated
source with optimum efficiency includes: a digitally con-
trolled pulse width modulator (DPWM) for controlling a
switching power stage to supply a varying voltage to an
inductor; and a digital voltage feedback circuit for controlling
the DPWM in accordance with a feedback voltage corre-
sponding to the DC output voltage. The digital voltage feed-
back circuit includes: a ΔΣ analog-to-digital converter (ADC)
that is built with two voltage controlled oscillators (VCOs),
one converts the output voltage into a frequency signal, the
other serves as a reference; two sigma-delta discriminators
that digitize the two frequency signals generated from the
VCOs and a digital comparator that generates the digital error
between the two digitized frequency signals; a proportional
integrator derivative (PID) circuit that accurately generates a
9-bit number to the DPWM blocks before being converted in
the actual duty cycle that drives the power stage.

According to one embodiment of the present invention, a
DC-DC converter configured to generate a DC output voltage
includes: a digitally controlled pulse width modulator con-
figured to control a switching power stage to supply a varying
voltage to an inductor; and a digital voltage feedback circuit
configured to control the digitally controlled pulse width
modulator in accordance with a feedback voltage corre-
sponding to the DC output voltage, the digital voltage feedback
circuit including: a first voltage controlled oscillator con-
figured to convert the feedback voltage into a first frequency
signal and to supply the first frequency signal to a first fre-
quency discriminator; a second voltage controlled oscillator
configured to convert a reference voltage into a second fre-
quency signal and to supply the second frequency signal to a
second frequency discriminator; a digital comparator configured
to compare digital outputs of the first and second fre-
quency discriminators and to output a digital feedback signal;
and a controller configured to control the digitally controlled
pulse width modulator in accordance with the digital feed-
back signal.

The DC-DC converter may further include: a triangular
current source coupled to the inductor; and a read-out circuit
for measuring a voltage across the inductor, the read-out
circuit comprising: a low-pass filter having a first terminal
coupled to a first end of the inductor and a second terminal
coupled to a second end of the inductor, the low-pass filter
supplying an inductor voltage corresponding to the voltage
across the inductor; and a third voltage controlled oscillator
configured to convert the inductor voltage into a third fre-
quency signal and to supply the third frequency signal to a
third frequency discriminator, the third frequency discrimi-
nator being coupled to the digital comparator to compare the
digital outputs of the second and third frequency discrimina-
tors; wherein the controller is configured to measure an
inductance of the inductor based on a magnitude of a voltage
waveform of the inductor voltage, the voltage waveform
being generated when a triangular current waveform is
applied to the inductor, and wherein the controller is further
configured to control the digitally controlled pulse width
modulator in accordance with the measured inductance.

The controller may be further configured to measure a
resistance of the inductor based on a slope of the voltage
waveform of the inductor voltage.

The controller may be further configured to compute a
magnitude of a current flowing through a load coupled to the
DC output voltage, the magnitude of the current being com-
The low-pass filter may be a first order low pass filter. The low-pass filter may include: an op-amp; and a feedback resistor and a feedback capacitor coupled in parallel between the output of the op-amp and an inverting input of the op-amp.

The DC-DC converter may further include a DC-offset control circuit, the DC-offset control circuit including: a feedback resistor and a feedback capacitor coupled in parallel between a reference voltage source and a non-inverting input of the op-amp.

The low-pass filter may be a Sallen-Key or Tow-Thomas biquad filter.

The DC-DC converter may be a buck converter, a boost converter, or a buck-boost converter.

The DC-DC converter may further include a CIC decimator coupled between the digital comparator and the controller, and configured to decimate the digital feedback signal received from the digital comparator and to supply the decimated digital feedback signal to the controller.

The further may further include a plurality of CIC decimators, each of the CIC decimators being coupled between a corresponding one of the frequency discriminators and the digital comparator, and configured to decimate the digital outputs received from the frequency discriminators and to supply the decimated digital outputs to the digital comparator.

The digitally controlled pulse width modulator may be configured to have an output duty cycle controlled by a plurality of most significant bits and a plurality of least significant bits, and wherein the digitally controlled pulse width modulator includes: a counter configured to supply the most significant bits; and a delay locked loop configured to supply the least significant bits.

According to another embodiment of the present invention, a method of operating a DC-DC converter including an inductor includes, during power up of the DC-DC converter: supplying a triangular current to the inductor; measuring a voltage waveform across the inductor; computing an inductance of the inductor based on a magnitude of the voltage waveform; and computing a resistance of the inductor based on a magnitude of the voltage waveform.

The method may further include decimating the first digital signal and the second digital signal, wherein the comparing the first digital signal to the second digital signal comprises comparing the decimated first digital signal and the decimated second digital signal.

The method may further include decimating the measured voltage waveform.

The method may further include, during operation of the DC-DC converter, converting an output voltage of the DC-DC converter to a third frequency signal corresponding to the frequency of the third frequency signal; converting a second reference voltage to a fourth frequency signal corresponding to the second reference voltage; converting the fourth frequency signal into a fourth digital signal corresponding to the frequency of the fourth frequency signal; and comparing the third digital signal to the fourth digital signal to produce a digital feedback signal.

The method may further include, during operation of the DC-DC converter: measuring a current sense voltage across the inductor; and computing a load current flowing through a load coupled to an output of the DC-DC converter in accordance with the measured current sense voltage and the computed resistance.
DETAILED DESCRIPTION

In the following detailed description, only certain exemplary embodiments of the present invention are shown and described, by way of illustration. As those skilled in the art would recognize, the invention may be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Like reference numerals designate like elements throughout the specification.

Lossless load current sensing is a desirable feature of current or voltage mode controlled DC-DC converters. Current sensing can be used for short circuit detection, multi-stage converter load balancing, thermal control, and load independent control of DC-DC converters. In addition, current sensing techniques have recently used the existing inductor series resistance (DCR) instead of a separate current sensing resistor to achieve the reduced complexity and reduced losses associated with such circuits.

As such, accurate measurements of the DCR \( R_{\text{DCR}} \) and the inductance \( L \) of an inductor are important to provide for proper control of DC-DC converters. However, in certain usage environments, the inductance and the DCR of the inductor may vary and/or drift over time. For example, space-borne DC-DC circuits may be exposed to radiation (e.g., total ionizing dose or galactic cosmic rays) which may cause temporary perturbations of the output signal or permanent drifts of the electrical parameters of components in the circuit. As another example, components of DC-DC converters used in automotive or aerospace applications may also have component values (e.g., resistances and inductances) which may drift due to exposure to heat or changes in temperature. On the one hand, the temporary variation in the output voltage can be filtered out due to the digital implementation. On the other hand, drift of the components may also be tracked using current measurements.

Embodiments of the present invention are directed to a digitally controlled DC-DC converter which includes a built-in self-test (BST) feature to measure the DCR \( R_{\text{DCR}} \) and the inductance \( L \) of the inductor. The BST feature may be used to obtain a digital measurement of the DCR and the inductance of the inductor during start-up, thereby allowing more accurate load current sensing and tuning of the driving waveforms to match the actual values of components of the circuit. Embodiments of the present invention also include an offset independent inductor characterization, enabling a digital continuous lossless load current sensing scheme which may be used with voltage-mode or current-mode controlled converters, as well as multi-stage parallel converters.

FIG. 1 is a block diagram illustrating a DC-DC converter according to one embodiment of the present invention where the DC-DC converter is a digital PWM buck converter utilizing a first order sigma delta (ΣΔ) based frequency discriminator to generate an accurate representation of an instantaneous frequency of a carrier signal. In other embodiments of the present invention, the digital control approach is not only limited to the buck topology; this approach may be used to build a boost converter or a buck-boost converter. The discriminator and proportional-integral-derivative (PID) controller, which uses the error signal to derive the appropriate duty cycle for the pulse width modulator, may be implemented using an FPGA, a separate integrated circuit, or other circuits as are well known in the art. The PID controller may implement control algorithms, broadly termed as “nonlinear control” or “adaptive control”, which are well known to those of ordinary skill in the art and which take account of the load characteristics, thereby offering improved efficiency and reliability.

FIG. 2A is a block diagram illustrating a DC-DC converter according to one embodiment of the present invention in more detail. The DC-DC converter includes a digital feedback circuit which converts a feedback voltage \( V_{fb} \) (which is representative of the output voltage \( V_{out} \)) to a frequency using a voltage controlled oscillator (VCO) \( \text{610a} \) (which may be referred to herein as the “first” VCO). The frequency signal is then converted to a single-bit sigma-delta modulated feedback signal using a ΣΔ (sigma-delta) discriminator \( \text{630a} \) (which may be referred to herein as the “first” ΣΔ discriminator) which is compared to an analog voltage reference \( V_{ref} \) which is sigma-delta modulated via a matched VCO \( \text{610b} \) (which may be referred to herein as the “second” VCO) and a ΣΔ discriminator \( \text{630b} \) (which may be referred to herein as the “second” ΣΔ discriminator). The 3-level filter \( 1 \Sigma \Delta \) noise shaped error signal is then decimated using a 2-stage comb (CIC) filter (or decimator) \( \text{650} \) to reduce the signal rate and the decimated signal is applied to the compensator (PID) \( \text{700} \) input. In other embodiments of the present invention (as shown, for example, in FIG. 1), first and second decimators \( \text{650a} \) and \( \text{650b} \) are used to reduce the signal rate prior to supplying the signal to the digital comparator \( \text{690} \). The PID compensator \( \text{700} \) which may be a 9-bit PID compensator calculates the duty cycle for reaching the target output voltage and supplies a duty cycle command to the digital PWM \( \text{100} \) to drive the PFET and NFET of the power stage \( \text{300} \) via a non-overlap dead-time gate driver \( \text{200} \).

FIG. 2B is a block diagram illustrating an Infinite Impulse Response (IIR) filter \( \text{710} \), which implements a PID compensator \( \text{700} \), according to one embodiment of the present invention. The PID controller can also be implemented as a simple look-up table, emulating the response of the IIR filter.

Although the circuit shown in FIG. 2A includes a single gate driver stage \( \text{200} \), embodiments of the present invention are compatible with multiple gate driver stages and power FETs, including external ones. In addition, FIG. 2A illustrates the use of a buck converter, which are generally well known to one of ordinary skill in the art. However, embodiments of the present invention are not limited thereto and may also be used with other DC-DC converters such as a boost converter or a buck-boost converter.

According to one embodiment of the present invention, in the digital comparison block \( \text{600} \), a reference voltage \( V_{ref} \) is compared to the output voltage \( V_{out} \) using a digital feedback circuit implementing a digitally intensive scheme based on voltage-to-frequency conversion, instead of using a full analog-to-digital converter (ADC). In some embodiments the output voltage \( V_{out} \) is scaled using a scalar \( \text{510} \) (e.g., a resistor divider) to produce a feedback voltage \( V_{fb} \) and the reference voltage \( V_{ref} \) is compared to the feedback voltage \( V_{fb} \). The reference voltage and output voltage drive matched Voltage Controlled Oscillators (VCOs) \( \text{610a} \) and \( \text{610b} \) which will be referred to generically as \( \text{610} \), which output signals having frequencies corresponding to the voltages supplied. The generated frequencies are measured using frequency discriminators (e.g., digitally intensive Delta-Sigma frequency discriminators) \( \text{630a} \) and \( \text{630b} \) which will be referred to generically as \( \text{630} \) and the measured frequencies are compared at a digital comparator \( \text{690} \).

Embodiments of the present invention which use time/frequency based digitization may be substantially independent of process variations because VCO paths are matched. In addition, frequency domain ADC circuits can be implemented in much smaller die areas than comparable voltage mode ADC circuits, are easily combined with digital pro-
cesses, and can be ported to different fabrication processes easily. In addition, the use of a digital scheme avoids the additional design requirements and circuit sensitivities associated with analog comparator offset and analog ramp linearity. However, embodiments of the present invention are not restricted to the above described use of VCOs and frequency discriminators to obtain and compare a digital representation of the output voltage with a reference value. For example, a fully analog loop filter based ADC can also be used for this purpose. Other suitable ADC approaches include two-step and sub-ranging ADCs.

The Digital Pulse Width Modulator (DPWM) 100 derives its output signal (which is supplied to the gate driver 200 through a level shifter 210 to control the power stage 300) from a segmented coarse/fine scheme where the fine delay is generated using a high accuracy phase locked digitally controlled ring oscillator, e.g., a delay locked loop (DLL) 110 (see, e.g., FIG. 3), within the DPWM and the coarse delay is supplied from a counter driven by a clock signal (e.g., f_coarse as shown in FIG. 2). The coarse delay is set by a simple counter driven by f_coarse. The coarse delay controls the majority of the output signal. In the proposed figure, the 3 most significant bits control the coarse delay and thus the coarse delay controls the output voltage at increments of 1/40 of the full output range. As such, the output duty cycle according to embodiments of the present invention is substantially independent of process variations and ambient temperature, which would have affected the duty cycle of an open loop analog oscillator. The coarse/fine approach significantly reduces the size of the delay line and reduces the overall clock cycle while maintaining high duty cycle resolution. Locking the DLL to the clock improves the monotonicity of the output, which can be difficult to achieve in segmented approaches which use open loop feedback circuits. In addition, embodiments of the present invention also include a load and filter characterization engine, enabling auto calibration and built-in self-test of the load and filter, which will be illustrated and described below in reference to, for example, FIG. 6.

FIG. 3A illustrates a DPWM 100 according to one embodiment of the present invention. FIG. 3B is a diagram illustrating various driving waveforms labeled in FIG. 3A, according to one embodiment of the present invention. According to this embodiment, the DPWM 100 is configured to have its 5 most significant bits (5 bits MSB) controlled by a counter 120 and its 4 least significant bits (4 bits LSB) controlled by the DLL circuit 110. However, in other embodiments of the present invention, various other numbers of bits may be controlled by the counter 120 or the DLL circuit 110, depending on the resolution desired for the application. The clock frequency f_coarse is supplied to a frequency divider 130 to generate a switching frequency f_s. According to one embodiment, the switching frequency is approximately 500 kHz. The clock frequency f_coarse is reduced from \( f_{coarse} = 2^{MSB_{ref}} f_s \) to \( f_{coarse} = 2^{MSB_{ref}} f_s \), where f_s is switching frequency and n is the PWM resolution. Such a circuit is suitable for high resolution and high switching frequency applications.

A 16 MHz clock f_coarse (e.g., CLK_16M) is used to generate the pulse with a 1 µs switching frame. A 4 bit counter 120 from the 16 MHz clock generates the coarse count CNT (i.e., 0-15 clock edges). The coarse count CNT is compared with the most significant bits supplied by the PID controller (PID_MSB) to control the time period of the coarse count COMP_OUT. A 16-stage delay line 118 divides the clock pulse into 16 equal time periods. A 16-to-1 mux 122 selects the appropriate tap from the delay line 118 in accordance with the least significant bits supplied by the PID controller PID_LSB. The time period from the coarse count COMPOUT is summed with the time period DLL_OUT from the delay line 118 to achieve 8 bits of output resolution FF_RST. The combined coarse and fine delay signals, in turn, control the width of the pulses of the output signal PWM (see, e.g., “Coarse Delay” and “Fine Delay” in FIG. 3B). Monotonicity is substantially improved or guaranteed with this scheme over equivalent analog circuits, as is independence from process variation and ambient temperature. Higher resolution is possible by increasing the clock frequency and number of bits in the coarse counter and/or increasing the number of stages in the DLL.

A DLL circuit 110 according to one embodiment of the present invention is illustrated in FIG. 4A. A phase frequency detector (PFD) 112 receives a reference signal \( f_{ref}(CLK_{ref}) \) and a feedback signal CLK_fb. The PFD supplies an “up” signal and a “down” signal to the Q-pump 114, which supplies a Vctrl signal to the bias generator 116, which, in turn, supplies Vp and Vn signals to the delay line 118. In some embodiments of the present invention, for Vctrl from 0–Vdd, the DLL does not lock in a multiple periods state. In addition, the capacitors and bias can be tuned to calibrate for process variations and the initial value of Vctrl can be set and monitored. As an alternative approach, instead of an analog phase-frequency detector, a digital phase detector followed by a digital loop filter can also be used to control this DLL. This approach is termed all-digital DLL (ADDLL) in the literature and the delay line is controlled digitally.

The proposed DLL should be stable across all temperature and voltage ranges. It should not lock to higher harmonics of the input frequency. These properties are desired for most of the DLL applications. A start-up calibration can be used to ensure that the DLL does not lock to higher harmonics across all process, temperature, and voltage variations.

The delay line is current controlled, and the delay line should be functional even upon start up when the control voltage can be zero. As such, according to one embodiment, a current mirror 115 as shown in FIG. 4B supplies voltages vb and vba to Q-pump 114 to supply a bias for the delay line 118 upon start-up.

FIG. 5 is a circuit diagram illustrating a voltage controlled oscillator (VCO) 610 (e.g., VCO 610a or 610b) as shown in FIG. 2) and a frequency discriminator 630 (e.g., frequency discriminator 630a or 630b) according to one embodiment of the present invention. The VCO 610 illustrated in FIG. 5 includes a current mirror 611 and a ring oscillator 614, but other embodiments of the present invention may use a VCO having a variety of alternative structures, as would be understood by one of ordinary skill in the art.

The VCO 610 provides an output signal \( f_{out}(t) \) which depends on the voltage supplied to the VCO 610. The output signal \( f_{out}(t) \) is supplied to the frequency discriminator 630 in which it is compared with a reference frequency \( f_{ref} \) and converted into a digital representation thereof, then output as \( \Delta \Delta M \) Bitstream y.

Referring again to FIG. 2, the outputs of the discriminators 630a and 630b (e.g., the \( \Delta \Delta M \) Bitstreams from each of the discriminators) are supplied to a digital comparator 650, and the output of the digital comparator is supplied to a CIC decimator (e.g., a 2-stage comb filter) 650f, which closes the
feedback loop by supplying a digital feedback signal to PID compensator \( 700 \) which is configured to control the DPWM

100.

As such, embodiments of the present invention provide a digital feedback signal to control the output voltage of the DC-DC converter, thereby improving reliability and output uniformity over analog feedback approaches by reducing the effect of process variation and changes due to environmental conditions.

According to one aspect of embodiments of the present invention, embodiments of the present invention may be operated in a built-in self-test (BIST) mode to measure an inductance (L) and a DC resistance (DCR) of a device-under-test (DUT), e.g., a power inductor, in the converter circuit.

FIG. 6A is an annotated circuit illustrating a readout circuit for measuring a voltage across the DUT of a DC-DC converter as shown in the embodiment of FIG. 2. For the sake of convenience, the digital feedback portion of the circuit of FIG. 2 (e.g., the scalar 510, the VCO 610a, and the \( \Sigma \Delta \) discriminator 630a) is not repeated in FIG. 6A, and a triangular current generator \( T_{TR} \) 160 and a read-out chain (including an op-amp circuit 520, a VCO, and a sigma-delta discriminator) are included to illustrate components for operating the DC-DC converter in BIST mode. Switches 522 are coupled between the read-out chain and the device under test to disconnect the read-out chain from the rest of the circuit when the read-out chain is not in use.

FIG. 6B is a waveform diagram illustrating voltage and current waveforms at various portions of the circuit illustrated in FIG. 6A.

Referring to FIG. 6A, according to one embodiment, the triangular current generator \( T_{TR} \) 160 supplies a triangular waveform to the device-under-test (DUT) 410, which is an inductor having inductance L, and is part of the LC circuit 400. The inductance of the device-under-test 410 can be based on the magnitude of the voltage across the inductor when a time varying current is applied through the inductor. In particular, the time varying voltage across a real inductor is given by

\[
\gamma(t) = \frac{d\theta(t)}{dt} + R(t),
\]

where \( \theta(t) \) is the current passing through the inductor, \( L \) is the inductance of the inductor, and \( R \) (or \( R_{DCR} \)) is the resistance of the inductor.

The voltage across the inductor \( V_{ND} \) is amplified by a first-order low-pass filter (or a lossy integrator) 520 which includes an operational amplifier OPA with input resistors \( R_p \) and a feedback capacitor \( C_f \) in parallel with a feedback resistor \( R_f \). The input resistors \( R_p \) have a resistance large enough such that the current flowing through them is substantially ignorable compared to \( T_{TR} \). The feedback capacitor \( C_f \) and the feedback resistor \( R_f \) can filter the ringing high frequency signal generated by the inductance and the parasitic capacitance of the power stage.

According to other embodiments of the present invention, higher order filters such as those that utilize Sallen-Key or Tow-Thomas biquad topologies may be used in place of the first order low pass filter 520.

In addition, in some embodiments of the present invention, a DC offset control circuit 530 may be used to set the DC level of the output difference voltage \( V_{DIFF} \). The DC offset control circuit 530 includes a voltage source \( V_{DBS} \) coupled to the non-inverting input of the operational amplifier OPA through a resistor in parallel with a capacitor, the resistor and capacitor having values respectively matching values of the feedback resistor \( R_f \) and the feedback capacitor \( C_f \).

As such, the resistance \( R \) (or \( R_{DCR} \)) of the inductor is proportional to the slope of the upper and lower portions of the waveform (e.g., between point B and C as labeled in FIG. 6B). For the sake of convenience, the slope of the upper end and lower end portions of the waveform will be referred to as the “slope” of the waveform. In addition, the inductance \( L \) of the inductor is proportional to the voltage across the inductor after subtracting the effect of the resistance of the inductor (e.g., the average voltage between points B and C). For sake of convenience, this voltage across the inductor after subtracting the resistance will be referred to herein as the “magnitude” of the waveform.

The output voltage difference \( V_{DIFF} \) is processed through substantially the same processing path as the feedback signal during normal operation. The voltage difference signal \( V_{DIFF} \) is passed through a VCO 610c (which may be referred to herein as the “third” VCO) to be converted into a frequency signal and converted to a digital representation thereof by a \( \Sigma \Delta \) discriminator 630c (which may be referred to herein as the “third” \( \Sigma \Delta \) discriminator). The digitized representation of the voltage difference signal \( V_{DIFF} \) is compared to a frequency signal corresponding to reference voltage \( V_{DR} \) as output by a matched VCO 610b coupled to the \( \Sigma \Delta \) discriminator 630b. The reference voltage \( V_{DR} \), may have different values during normal operation and during BIST operations. The digital output of the digital comparator 690 is then decimated by the CIC Decimator 650r, and the resulting bitstream is supplied to a digital post processing component 670, which may supply a digital signal to the PID controller 700 (see, e.g., FIG. 2) in order to modify the driving waveforms in accordance with the inductance and resistance characteristics of the inductor 410.

Referring to FIG. 7, an adaptive DC-DC converter according to embodiments of the present invention includes both the digital feedback circuit (including the scalar 510, the first VCO 610a, and the first \( \Sigma \Delta \) discriminator 630a) illustrated, for example, in FIG. 2A and the readout circuit (including the op-amp circuit 520, the third VCO 610c, and the third \( \Sigma \Delta \) discriminator 630c) illustrated, for example, in FIG. 6A. The inductance and DCR values of the inductor measured by the readout circuit can be used to fine tune the digital controller coefficients in the PID controller 700.

According to one embodiment, the IIR transfer function is:

\[
y = \frac{a_0z^2 + a_1z + a_2}{b_0z^2 + b_1z + b_2} x
\]

This IIR transfer function determines the phase and amplitude margin, hence the stability conditions of the system. The parameters that determine the un-compensated response of the system are switching frequency, load inductor, capacitor, and their DCR and ESR respectively. Once these component values are determined, one can use open loop phase margin multiplied by the compensator response, and modify the IIR coefficients so that the system is stable. Also, the DCR value may be used to normalize and to measure the load current. In harsh environment applications where the characteristics of external components can degrade (such as in automotive applications or in outer space), the controller can update these coefficients to compensate for the change or degradation of the external components.

FIG. 8 is a flowchart illustrating a method of operating a DC-DC converter according to one embodiment of the
While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

What is claimed is:

1. A DC-DC converter configured to generate a DC output voltage, the DC-DC converter comprising:
   - a digitally controlled pulse width modulator configured to control a switching power stage to supply a varying voltage to an inductor; and
   - a digital voltage feedback circuit configured to control the digitally controlled pulse width modulator in accordance with a feedback voltage corresponding to the DC output voltage, the digital voltage feedback circuit comprising:
     - a first voltage controlled oscillator configured to convert the feedback voltage into a first frequency signal and to supply the first frequency signal to a first frequency discriminator;
     - a second voltage controlled oscillator configured to convert a reference voltage into a second frequency signal and to supply the second frequency signal to a second frequency discriminator;
     - a digital comparator configured to compare digital outputs of the first and second frequency discriminators and to output a digital feedback signal; and
     - a controller configured to control the digitally controlled pulse width modulator in accordance with the digital feedback signal.

2. The DC-DC converter of claim 1, further comprising:
   - a triangular current source coupled to the inductor; and
   - a read-out circuit for measuring a voltage across the inductor, the read-out circuit comprising:
     - a low-pass filter having a first terminal coupled to a first end of the inductor and a second terminal coupled to a second end of the inductor, the low-pass filter supplying an inductor voltage corresponding to the voltage across the inductor; and
     - a third voltage controlled oscillator configured to convert the inductor voltage into a third frequency signal and to supply the third frequency signal to a third frequency discriminator, the third frequency discriminator being coupled to the digital comparator to compare the digital output of the second frequency discriminator and a digital output of the third frequency discriminators discriminator;

   wherein the controller is configured to measure an inductance of the inductor based on a magnitude of a voltage waveform of the inductor voltage, the voltage waveform being generated when a triangular current waveform is applied to the inductor, and

   wherein the controller is further configured to control the digitally controlled pulse width modulator in accordance with the measured inductance.

3. The DC-DC converter of claim 2, wherein the controller is further configured to measure a resistance of the inductor based on a slope of the voltage waveform of the inductor voltage.

4. The DC-DC converter of claim 3, wherein the controller is further configured to compute a magnitude of a current flowing through a load coupled to the DC output voltage, the magnitude of the current being computed in accordance with the voltage across the inductor and the measured resistance of the inductor.
5. The DC-DC converter of claim 2, wherein the low-pass filter is a first order low pass filter.

6. The DC-DC converter of claim 5, wherein the low-pass filter comprises:
   an op-amp; and
   a first feedback resistor and a first feedback capacitor coupled in parallel between an output of the op-amp and an inverting input of the op-amp.

7. The DC-DC converter of claim 6, further comprising a DC-offset control circuit, the DC-offset control circuit comprising:
   a second feedback resistor and a second feedback capacitor coupled in parallel between a reference voltage source and a non-inverting input of the op-amp.

8. The DC-DC converter of claim 2, wherein the low-pass filter is a Sallen-Key or Tow-Thomas biquad filter.

9. The DC-DC converter of claim 1, wherein the DC-DC converter is a buck converter, a boost converter, or a buck-boost converter.

10. The DC-DC converter of claim 1, further comprising a CIC decimator coupled between the digital comparator and the controller and configured to decimate the digital feedback signal received from the digital comparator and to supply the decimated digital feedback signal to the controller.

11. The DC-DC converter of claim 1, further comprising a plurality of CIC decimators, each of the CIC decimators being coupled between a corresponding one of the frequency discriminators and the digital comparator and configured to decimate the digital outputs received from the frequency discriminators and to supply the decimated digital outputs to the digital comparator.

12. The DC-DC converter of claim 1, wherein the digitally controlled pulse width modulator is configured to have an output duty cycle controlled by a plurality of most significant bits and a plurality of least significant bits, and wherein the digitally controlled pulse width modulator comprises:
   a counter configured to supply the most significant bits; and
   a delay locked loop configured to supply the least significant bits.

13. A method of operating a DC-DC converter comprising an inductor, the method comprising, during power up of the DC-DC converter:
   supplying a triangular current to the inductor;
   measuring a voltage waveform across the inductor;
   computing an inductance of the inductor based on a magnitude of the voltage waveform;
   computing a resistance of the inductor based on a slope of the voltage waveform; and
   configuring a controller to apply driving waveforms to the inductor in accordance with the computed inductance and the computed resistance.

14. The method of claim 13, wherein the measuring the voltage waveform across the inductor comprises:
   low-pass filtering an inductor voltage measured across the inductor;
   converting the filtered inductor voltage to a first frequency signal corresponding to the inductor voltage;
   converting the first frequency signal into a first digital signal corresponding to a frequency of the first frequency signal;
   converting a first reference voltage to a second frequency signal corresponding to the first reference voltage;
   converting the second frequency signal into a second digital signal corresponding to a frequency of the second frequency signal; and
   comparing the first digital signal to the second digital signal to produce the measured voltage waveform across the inductor.

15. The method of claim 14, further comprising decimating the first digital signal and the second digital signal, wherein the comparing the first digital signal to the second digital signal comprises comparing the decimated first digital signal and the decimated second digital signal.

16. The method of claim 14, further comprising decimating the measured voltage waveform.

17. The method of claim 13, further comprising, during operation of the DC-DC converter:
   converting an output voltage of the DC-DC converter to a third frequency signal corresponding to the output voltage;
   converting the third frequency signal to a third digital signal corresponding to a frequency of the third frequency signal;
   converting a second reference voltage to a fourth frequency signal corresponding to the second reference voltage;
   converting the fourth frequency signal into a fourth digital signal corresponding to a frequency of the fourth frequency signal; and
   comparing the third digital signal to the fourth digital signal to produce a digital feedback signal.

18. The method of claim 13, further comprising, during operation of the DC-DC converter:
   measuring a current sense voltage across the inductor; and
   computing a load current flowing through a load coupled to an output of the DC-DC converter in accordance with the measured current sense voltage and the computed resistance.