The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for FY15 and Beyond

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NASA/GSFC
http://nepp.nasa.gov

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Open Access
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMOLED</td>
<td>Active Matrix Organic Light Emitting Diode</td>
</tr>
<tr>
<td>CBRAM</td>
<td>Conductive Bridging Random Access Memory</td>
</tr>
<tr>
<td>CGA</td>
<td>Column Grid Array</td>
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<tr>
<td>CIGS</td>
<td>Copper Indium Gallium Selenide</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<tr>
<td>COTS</td>
<td>Commercial Off The Shelf</td>
</tr>
<tr>
<td>DDR4</td>
<td>Double Data Rate Four</td>
</tr>
<tr>
<td>DNA</td>
<td>Deoxyribonucleic Acid</td>
</tr>
<tr>
<td>DoD</td>
<td>Department of Defense</td>
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<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
</tr>
<tr>
<td>EEE</td>
<td>Electrical, Electronic, and Electromechanical</td>
</tr>
<tr>
<td>EPC</td>
<td>Efficient Power Conversion</td>
</tr>
<tr>
<td>ESL</td>
<td>Electronic System Level</td>
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<tr>
<td>FeRAM</td>
<td>Ferroelectric RAM</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FY</td>
<td>Fiscal Year</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>Gen</td>
<td>Generation</td>
</tr>
<tr>
<td>GSFC</td>
<td>Goddard Space Flight Center</td>
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<tr>
<td>HALT</td>
<td>Highly Accelerated Life Test</td>
</tr>
<tr>
<td>HAST</td>
<td>Highly Accelerated Stress Testing</td>
</tr>
<tr>
<td>HEMTs</td>
<td>High-electron-mobility transistors</td>
</tr>
<tr>
<td>HP Labs</td>
<td>Hewlett-Packard Laboratories</td>
</tr>
<tr>
<td>HW</td>
<td>Hardware</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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</table>

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<thead>
<tr>
<th>Acronym</th>
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</thead>
<tbody>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>IR</td>
<td>Infrared</td>
</tr>
<tr>
<td>IR/Infineon</td>
<td>International Rectifier/Infineon Technologies</td>
</tr>
<tr>
<td>LCoS</td>
<td>Liquid-Crystal-on-Silicon</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro Electrical-Mechanical System</td>
</tr>
<tr>
<td>MOSFETS</td>
<td>Metal Oxide Semiconductor Field Effect Transistors</td>
</tr>
<tr>
<td>MRAM</td>
<td>Magnetoresistive Random Access Memory</td>
</tr>
<tr>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
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<tr>
<td>NAVY</td>
<td>Naval Surface Warfare Center, Crane, Indiana</td>
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<tr>
<td>NEPP</td>
<td>NASA Electronic Parts and Packaging</td>
</tr>
<tr>
<td>Occam</td>
<td>Open Conditional Content Access Management</td>
</tr>
<tr>
<td>OLED</td>
<td>Organic Light Emitting Diode</td>
</tr>
<tr>
<td>PBGA</td>
<td>Plastic Ball Grid Array</td>
</tr>
<tr>
<td>R&amp;D</td>
<td>Research and Development</td>
</tr>
<tr>
<td>RERAM</td>
<td>Resistive Random Access Memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SEE</td>
<td>Single Event Effect</td>
</tr>
<tr>
<td>SERDES</td>
<td>Serializer/Deserializer</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
</tr>
<tr>
<td>SOC</td>
<td>Systems on a Chip</td>
</tr>
<tr>
<td>TI</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>TRL</td>
<td>Technology Readiness Level</td>
</tr>
<tr>
<td>VNAND</td>
<td>Vertical NAND</td>
</tr>
<tr>
<td>WBG</td>
<td>Wide Band Gap</td>
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</table>
Technology Selection Criteria for NEPP Investigation

• The technologies should satisfy all or most of the following criteria:
  – Wide applicability,
  – Product level or in productization, and,
  – No distinction: COTS to hi-reliability aerospace.

• Partnering arrangements with other organizations preferred.

• In general, we avoid:
  – Laboratory technologies, e.g., <TRL3,
  – Limited application devices with certain exceptions (critical application or NASA center specialization).
Technology assurance efforts are not explicitly included except on “Small Missions” chart.

Guidelines are a product of many technology evaluation tasks.

Only major product categories shown.

Technology areas not on Roadmap but under consideration include:

- Electro-optics (fiber optics),
- Advanced analog and mixed-signal devices,
- Imaging sensors,
- Modeling and simulation,
- High-speed communication (SERDES, fast data switches), and,
- Adjunct processors (e.g., graphics, signal processing)

Note 1: Advanced CMOS technologies not explicitly included:

- NEPP leverages samples from ongoing DoD and/or commercial sources.
- 14nm is current target.

Note 2: “Reliability testing” may include product and/or package testing.
Gartner Hype Cycle Concept

- **Technology Trigger**
- **Peak of Inflated Expectations**
- **Trough of Disillusionment**
- **Slope of Enlightenment**
- **Plateau of Productivity**

- **On the Rise**
  - Supplier proliferation
  - Mass media hype begins
  - Early adopters investigate
  - First-generation products, high price, lots of customization needed
  - Startup companies first round of venture capital funding
  - R&D

- **At the Peak**
  - Activity beyond early adopters
  - Supplier consolidation and failures
  - Second/third rounds of venture capital funding

- **Sliding Into the Trough**
  - Negative press begins
  - Second-generation products, some services

- **Climbing the Slope**
  - Methodologies and best practices developing
  - Third-generation products, out of the box, product suites

- **Entering the Plateau**
  - High-growth adoption phase starts: 20% to 30% of the potential audience has adopted the innovation
Gartner Hype Cycle for Electronics 2013

Source: Gartner (July 2013)
### NEPP and Gartner Electronics Hype Cycle 2013

<table>
<thead>
<tr>
<th>Benefit</th>
<th>Transformational</th>
<th>High</th>
<th>Moderate</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>Years to adopt:</td>
<td>less than 2 years</td>
<td>2 to 5 years</td>
<td>5 to 10 years</td>
<td>more than 10 years</td>
</tr>
<tr>
<td>Moderate</td>
<td>Resistance Phase-Change Memory Through Silicon Vias</td>
<td>Resistance Polymer Memory Through Silicon Vias</td>
<td>Holographic Storage for Consumer Electronics</td>
<td></td>
</tr>
<tr>
<td>Low</td>
<td></td>
<td></td>
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**Future NEPP Area or Tracking Developments**

**NEPP Task Area**

*After Gartner 2013 Electronics Hype Cycle*

 Deliverable to NASA Electronic Parts and Packaging (NEPP) Program to be published on nepp.nasa.gov originally presented by Kenneth LaBel at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015.
Field Programmable Gate Arrays (FPGAs)

Trusted FPGA
- DoD Development

Altera
- Stratix 5 (28nm TSMC process commercial)
- Max 10 (55nm NOR based commercial – small mission candidate)
- Stratix 10 (14nm Intel process commercial)

Microsemi
- RTG4 (65nm RH)

Xilinx
- 7 series (28nm commercial)
- Ultrascale (20nm commercial – planar)
- Ultrascale+ (16nm commercial - vertical)
- Virtex 5QV (65nm RH)

TBD – (track status)

Radiation Testing
Reliability Testing
Radiation and Reliability Testing
Package Reliability Testing

FY14 FY15 FY16 FY17

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Xilinx Zynq UltraScale+ Multi-Processor System on a Chip (MPSoC) family

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Advanced Processors

Next Generation Space Processor (NGSP)
- Joint NASA-AFRL Program for RH multi-core processor
- TBD architecture/process

RH Processor
- BAE Systems RAD5510/5545
- Replacement for RAD750

Intel Broadwell Processors
- 14nm FinFET commercial
- 1st high-performance sans heatsink (lower power for performance)

Freescale P5020/5040
- Commercial 45nm network processor
- Preparation for RH processor

TBD – (track status)

Radiation Testing
Reliability Testing

FY14 FY15 FY16 FY17

Note: Future considerations under discussion include automotive “self-driving” processor options.

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Preliminary Radiation testing of 14nm Intel with Navy Crane
Microcontrollers and Mobile Processors (Small Missions)

TBD – other
- Atmel AT91SAM9G20, and TI Sitara AM3703,
- ARM (Snapdragon), Intel Atom mobile

TI MSP430
- Popular CubeSat microcontroller
- Several varieties

Freescale MPC56XX
- 90nm on-shore fab
- Automotive Grade
- Being used for both part and board level testing

Radiation Testing (limited)
Reliability Testing

FY14 FY15 FY16 FY17
Commercial Memory Technology

Other
- MRAM
- FeRAM

Resistive
- CBRAM (Adesto)
- ReRAM (Panasonic)
- ReRAM (Tezzaron)
- TBD (HP Labs, others)

DDR 3/4
- Intelligent Memory (robust cell twinning)
- Micron 16nm DDR3
- TBD – other commercial

FLASH
- Samsung VNAND (gen 1 and 2)
- Micron 16nm planar
- Micron Hybrid memory Cube
- TBD - other commercial

TBD – (track status)

FY14 FY15 FY16 FY17

TBD – (track status)

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation Testing

Reliability Testing

TBD – (track status)

TBD – (track status)

TBD – (track status)
Small Missions

EEE Parts Guidelines
- Small missions (Class D, CubeSat – 2 documents)
- System on a chip (SOC) single event effects (SEE) guideline

Commodities evaluation
- See commodities roadmaps for processors, power
- CubeSat Star Tracker

Automotive grade electronics
- Multiple classes of electronics (passives, actives, ICs)
- Testing by NASA and Navy Crane

Alternate test – board level
- Freescale MPC56XX
- Automotive Grade
- Both part and board level reliability testing

FY14 FY15 FY16 FY17

Guideline development
Radiation Testing Reliability Testing
Reliability Testing
Reliability Testing
Radiation Testing
Automotive Processors and Systems for Self-Driving Cars?

From Freescale.com
Wide Band Gap (WBG) Technology

GaN Class V development
- Microsemi with EPC

GaN Enhancement Mode HEMTs
- EPC Gen 2-3, 200 V - 600 V
- GaN Systems 100 V, 650 V
- Panasonic 600 V (target)
- IR/Infineon 600 V (target)

SiC MOSFETs
- Cree Gen 1-2 1200 V - 1700 V
  Gen 3- narrower neck
- STMicro baseline SEE test
- Rohm Trench design

SiC Diodes
- Manufacturer X SEE baseline and hardening efforts

SiC ICs
- Ozark IC
- Manufacturer X

FY14 FY15 FY16 FY17

TBD – (track status)

Radiation and Reliability Testing
Radiation Testing Reliability Testing

TBD – (track status)

Radiation Testing

TBD – (track status)

Radiation Testing

TBD – (track status)

Radiation Testing
Silicon Power Devices

MOSFETs – Rad Hardened
- Microsemi i2MOS
- Infineon superjunction 100 V, 600 V (target)
- IR/Infineon R8 trench 20 V

Schottky Diodes
- Multiple vendors, reverse voltage ratings, and forward current ratings

Radiation Testing
 Radiation Testing
 Radiation Testing
 Radiation Testing
 (track status)

FY14 FY15 FY16 FY17

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Packaging Technologies (1 of 2)

High Density, Non-hermetic Column Grid Array (CGA)
- Xilinx CN/Kyocera Daisy Chain
- Microsemi Daisy Chain
- Materials analysis, long term stress, root cause failure

HALT Methodology/Qualification
- HALT/HAST comparison
- Plastic BGA matrix

Area Array Column
- Selection guide

Thermal Interface Materials
- Selection guide

PBGA Thermal Cycle Evaluation

Reliability Testing
Guideline development
Reliability Testing
Guideline development
Reliability Testing

FY14 FY15 FY16 FY17

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Bump Reliability
- Technology review
- Test vehicle options

3D Packaging Technologies
- Technology review
- Test vehicle options

QFN package reliability
- Reliability/Qualification metrics

FY14  FY15  FY16  FY17

Guideline research
Guideline research
Reliability Testing
And Just When You Think Your Roadmap is Set, New Parts are Released

- **Examples**
  - More complex processors
    - TI Multicore DSP+ARM KeyStone II System-on-Chip (SoC)
  - Integrated “instruments”
    - TI DLP2010NIR – near IR sensing and controller
Summary and Comments

• NEPP Roadmaps are constantly evolving as technology and products become available.
  – Like all technology roadmaps, NEPP’s is limited to funding and resource availability.
  – Not shown are TBD passives and connector roadmaps under development.
  – NEPP is working to develop preliminary plans on interfacing to the NASA Reliability and Maintainability Program and its work on Model Based System Engineering (MBSE) approaches.

• We look forward to further opportunities to partner.

https://nepp.nasa.gov