Using Classical Reliability Models and Single Event Upset (SEU) Data to Determine Implementation Schemes for Triple Modular Redundancy (TMR) in SRAM-based Field Programmable Gate Array (FPGA) Devices

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Abstract: Space applications are complex systems that require intricate trade analyses for optimum implementations. We focus on a subset of the trade process, using classical reliability theory and SEU data, to illustrate appropriate TMR scheme selection.

Multiple Redundancy (TMR)

TMR schemes ([5, 6]) are defined by which portion of the circuit is replicated and where the various replicated copies are placed:

- Strong TMR implementation will replicate all data paths and apply separate power and clock to each path.
- Weak TMR implementation will replicate only portions of the data paths.
- Partial TMR implementation will replicate only portions of the data paths and apply separate power and clock to each path.

Tradeoff: TMR is typically used when the cost overhead and complexity are not prohibitive.

Reliability for TMR-based systems is dependent on the component failures and the priority of the system, as well as whether the system is active or is in a standby state. This is to be expected, as this system is not intended to operate outside the framework of a large, complex, space-based system.

Table 1: Comparison of SRAM-Based FPGA Technologies: Strengths and Weaknesses

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<thead>
<tr>
<th>Technology</th>
<th>Strengths</th>
<th>Weaknesses</th>
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<tbody>
<tr>
<td>TMR</td>
<td>Redundant components for high reliability</td>
<td>Increased cost and complexity</td>
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<tr>
<td>LBMR</td>
<td>Lower cost and complexity than TMR</td>
<td>Reduced reliability due to single point of failure</td>
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<tr>
<td>BTMR</td>
<td>Combination of TMR and LBMR</td>
<td>Increased cost and complexity</td>
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References