**Using Classical Reliability Models and Single Event Upset (SEU) Data to Determine Optimum Implementation Schemes for Triple Modular Redundancy (TMR) in SRAM-based Field Programmable Gate Array (FPGA) Devices**

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**Abstract:** Space applications are complex systems that require intricate trade analyses for optimum implementations. We focus on a subset of the trade process, using classical reliability theory and SEU data, to illustrate appropriate TMR scheme selection.

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**Introduction**

This study investigates mitigation performance and the architecture for a variety of mitigation design strategies. The motivation is to provide a means for analyzing and optimizing for critical applications, risk is measured by analyzing reliability afforded time using classical reliability models and measured single event upset (SEU) data.

In this study, reliability is also analyzed across particle fluence by converting classical reliability models [1] from the time domain into the space domain. As a benefit, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As a result, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As a benefit, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As a result, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As well as determining which mitigation technique (e.g., scrubbing) can be an effective technique.

**TMR Redundancy (TMR)**

TMR schemes [2-3] are defined by which portion of the circuit is a voter. A voter is a simple boolean logic block that can provide the output (1) if at least one of its inputs is (1). A voter block may have some complex inputs or outputs.

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**Triple Modular Redundancy (TMR) Models**

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**SRAM-Based FGPAs and TMR:**

Because configuration SEU is the dominant component faults in an unmitigated design [SRAM-based FPGAs (BMR) and (L)TMR is an attractive option to mitigate configuration SEUs but not all SEUs are configuration SEUs. With the use of multiple SEU data sets obtained from previous work, this study will further investigate using a variety of SEU data.

**Distributed TMR (DTMR)**

DTMR schemes [2-3] are defined by the voter location. At the voter, the outputs of complex blocks.

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**DTMR: Voting is only performed at the voter outputs of complex blocks.**

**Application Domain**

Space applications are complex systems that require intricate trade analyses for optimum implementations. We focus on a subset of the trade process, using classical reliability theory and SEU data, to illustrate appropriate TMR scheme selection.

**Figures and Tables**

- **Figure 1:** Block diagram of DTMR in an SRAM-based FPGA. With scrubbing, it is possible to achieve desired performance to the fluence domain. As a result, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As a benefit, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As a result, analyzing mitigation in the fluence domain provides the ability to better determine the ability to achieve desired performance to the fluence domain. As well as determining which mitigation technique (e.g., scrubbing) can be an effective technique.

- **Table 1:** Table of classical reliability models over time

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**Conclusion**

The conclusion presented above indicates that a variety of mitigation techniques are used to mitigate SEU effects. This is because the predictions from the fluence domain are not the same as the predictions from the space domain. The reason is that the predictions from the fluence domain are not the same as the predictions from the space domain. The reason is that the predictions from the fluence domain are not the same as the predictions from the space domain. The reason is that the predictions from the fluence domain are not the same as the predictions from the space domain. The reason is that the predictions from the fluence domain are not the same as the predictions from the space domain. The reason is that the predictions from the fluence domain are not the same as the predictions from the space domain.

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**References**

This study was supported by the National Aeronautics and Space Administration. Additional support was provided by NASA-Goddard Space Flight Center, Laurel, MD 20707. The authors would like to acknowledge the contributions of the following individuals: Melanie Berg, J. Pellish, J. Purvis, and M. Campola.