Using Classical Reliability Models and Single Event Upset (SEU) Data to Determine Optimum Implementation Schemes for Triple Modular Redundancy (TMR) in SRAM-based Field Programmable Gate Array (FPGA) Devices

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Abstract: Space applications are complex systems that require intricate trade studies for optimum implementations. We focus on a subset of the trade process, using classical reliability theory and SEU data, to illustrate appropriate TMR scheme selection.

This study investigates mitigation performance and the methodology for a variety of mitigation design strategies. The triad is to provide a means for analyzing and comparing strategies for critical applications. Risk is assessed by analyzing reliability across time using classical reliability models and measured single event upset (SEU) data.

In this study, reliability is also analyzed across particle fluence by transforming reliability results [1] from the time domain into the fluence domain. As a benefit, analyzing mitigation in the fluence domain provides the analysis necessary to provide a direct path to the ability to make direct comparisons to accelerated radiation test (data SEU) data. Design SEU data is obtained from the TEMPEST K7 Serial [20] device and implemented in the Xilinx Kintex-7 FPAG device (0.1” pitch) with a single technology. SEU data was obtained by performing heavy-ion testing at Texas A&M Cyclotron Facility.

Introduction

SEU Errors and Fault Correction

Equation (1) describes the four categories of SEUs in [21].

\[
\text{SEU} = \text{Single Event Functional Interrupt (SEFI)} + \text{Single Event Latch Up failure} + \text{Single Event Latch Up transient} + \text{Single Event Soft Error (SESE)}
\]

A trade is performed to determine the TMR scheme that requires the lowest amount of area and silicon while meeting project requirement.

SEU Test Methodology

The primary design under investigation (DUI) was the Counter Array [2] as illustrated in Figure 7. Variations of the DUI were created, each independent module (counters) and one large flushable structure (snap-shot copy). Each variation of the DUI was created with Triple Modular Redundancy (TMR) with and without partitioning.

SEU Test Methodology

The traditional approach to SEU data analysis and characterization is to convert SEU data to error-rates. However, during the conversion process (from the fluence (\(\Phi\)) domain to the time (\(t\)) domain), important information in the lower LET region is lost. Referring to Figure 10, the SEU data for the pure counting circuitry (counter 0) is presented. For the SEU test, the MEV process was employed to provide a high SEU rate environment for testing the circuitry. Although the SEU data in Figure 10 shows an apparent variation, the traditional approach of converting SEU to error-rate results in a rather noisy data set.

Table 1: Classical reliability model one-time

<table>
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<th>Type</th>
<th>Reliability</th>
<th>Availability</th>
<th>Mean Time To Failure</th>
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<tr>
<td>NMR</td>
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<tr>
<td>NR</td>
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<tr>
<td>BTMR</td>
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References

To be presented by Melanie Berg at the Institute of Electrical and Electronic Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC), Boston, Massachusetts, July 13-17, 2015.