

# Dynamic Emulation of NASA Missions for IV&V

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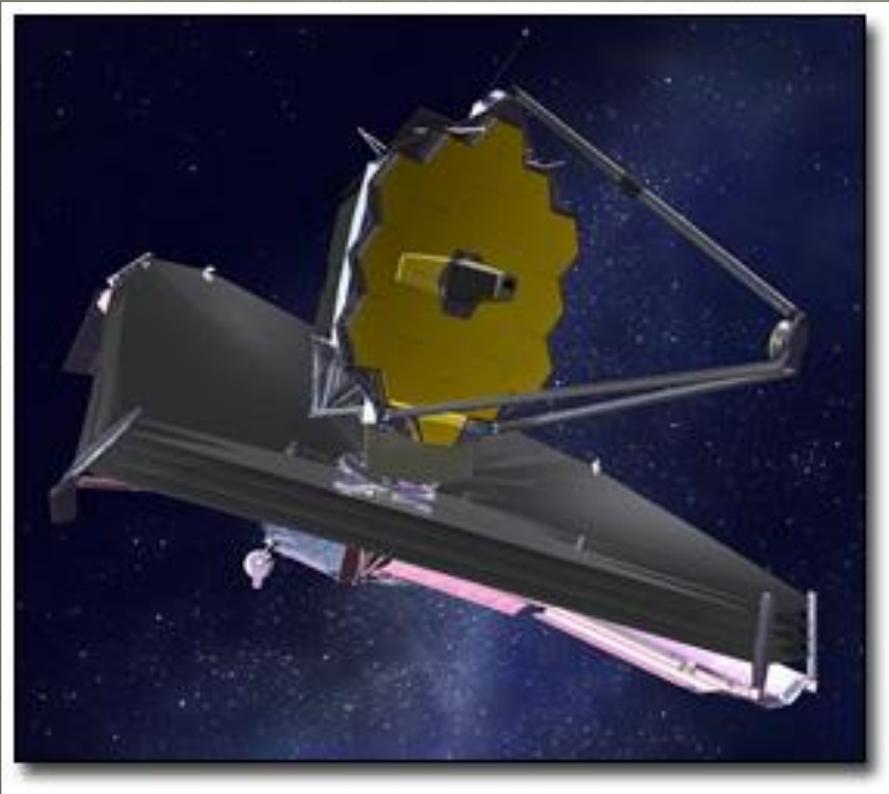
A case study of JWST and SLS

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# Focus Missions:

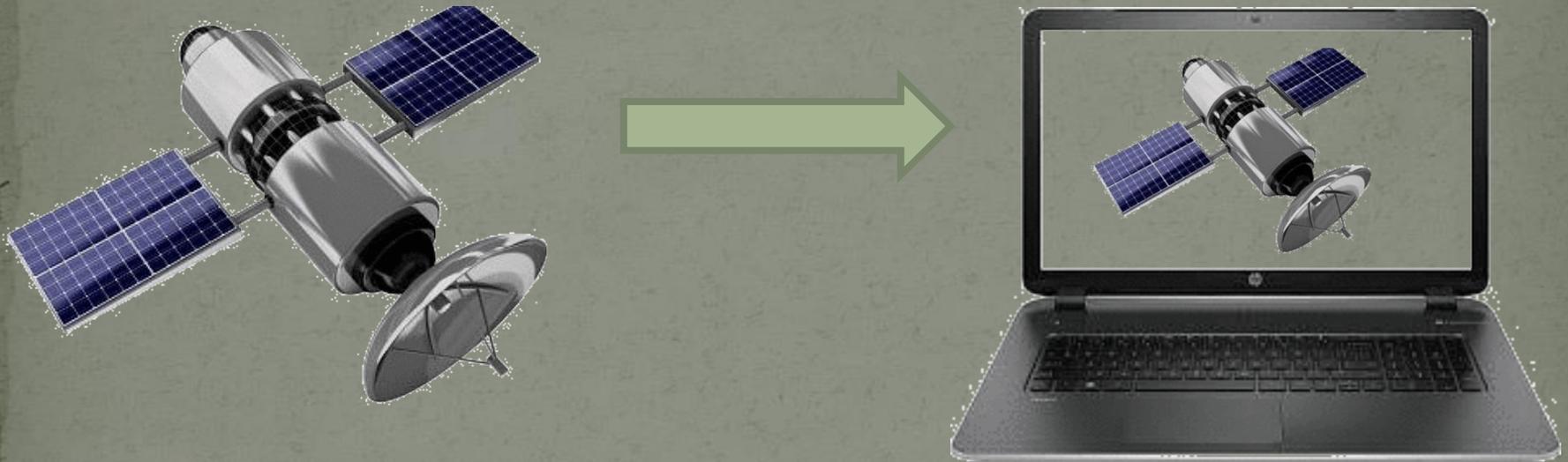


# Who we are?

- Independent Test Capability (ITC)
  - develop, maintain and operate adaptable test environments for the IV&V program that enables the dynamic analysis of software behaviors for multiple NASA missions



# What is Dynamic Emulation?



- Entire Flight “System” condensed to a Laptop
  - Sensors/Actuators are Simulated
  - Flight Computer Hardware is Emulated.
  - Flight Software binaries executed as delivered.
  - Ground Operations Integrated.

# Why we do it...

- Fault Injection
- Flexible Time
- Source Level Debugging
- Measureable V&V
- Unlimited Simulation Resources



# How we do it...

- Execute
  - Emulation software
    - assemble engine
- Construct
  - Device Modeling Language (DML)
    - registers, memory, interrupts, buses
- Connect
  - NOS Engine
    - ITC middleware product
- Integrate
  - Vendor's models and dynamics
  - Ground system software

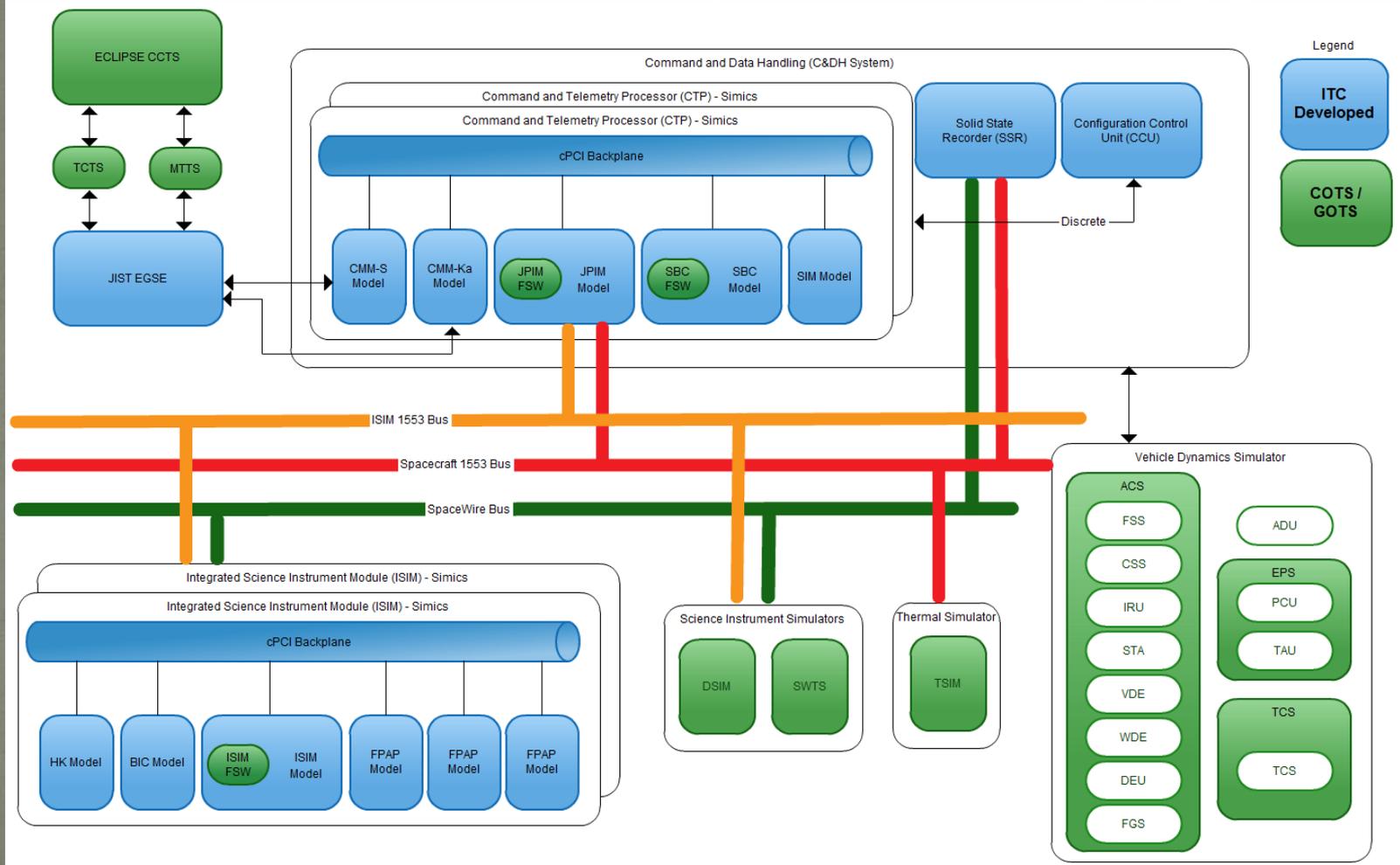


# JWST Integrated Simulation and Test

## JIST



# JIST → Architecture

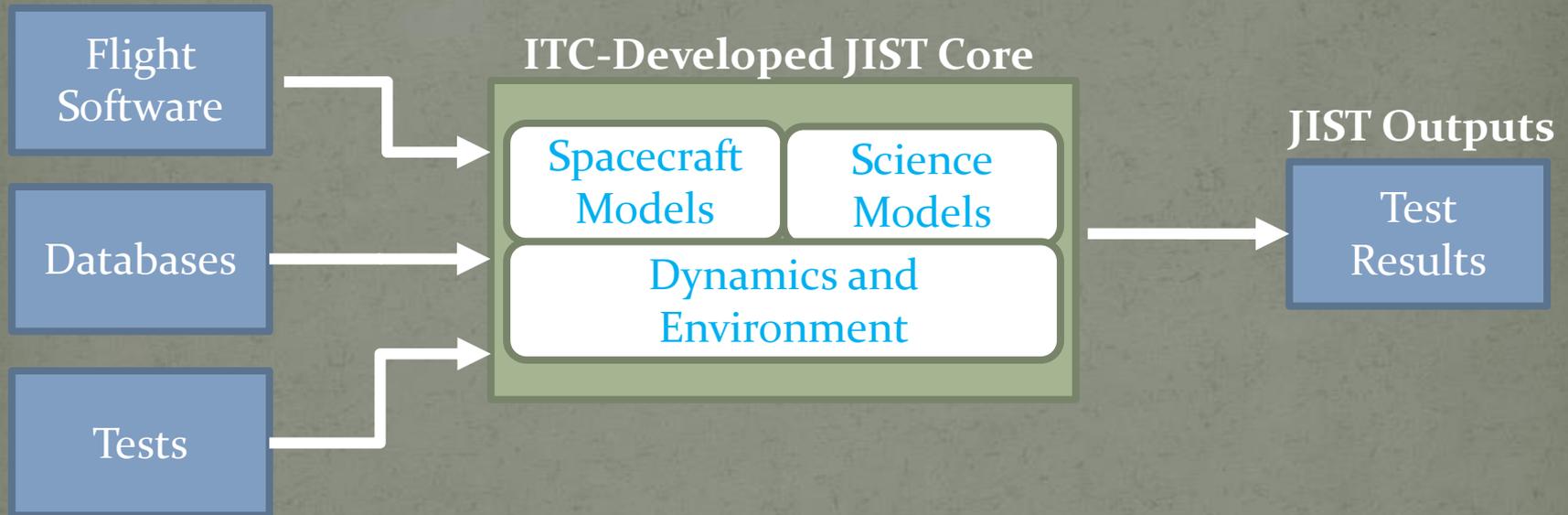


# JIST → Project Unique Abilities

- Only integration of Science and Spacecraft FSW
- Faster than real-time
- Flexible hardware configurations
- Hardware fault injection
- Source-line debugging
- Complete control of all memory states

# JIST → Test Cycle

## User-Supplied Inputs to JIST



# JIST Ground System Software

**HMI (CCTS\_A\_IVWCCTSECLIPSE OPS Spacecraft JW1 Area: DEFAULT, Phase: DEFAULT, Role: Operations)**

File Edit View Window Help

Primary Time: 2015:064:18:18:44 | Status: HWI Hrt Beat | VCID: 0 | Apid: 1070 | ForcePub: 26 | Mstr Alm: Enable | Suppress: Disable | Timeout: TIMEOUT 1 | #AlmRed: 285 | #UnackRed: 285 | #AlmYel: 138 | #UnackYel: 138 | Control: IVWCCTSECLIPSE

SITE: local | FEP: 1 | TLM: Connected | TLM Port: 3011 | Command: Connected | CMD Port: 4011 | CLCW: Connected | CLCW Port: 7011 | CFDP: Conn Err | CFDP Port: 0

CMD Mode: Single | Uplink Rate: 16 | Randomize: Disable | Raw Commanding: Enabled | Hex CMD MESS: Level 1 | PLOP Queue: 0

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**Central Command**

Command Status

TBT: Disabled

VCID: SC (0) ACTIVE | FOP-1 State: [v] | Validation: Enabled | Bypass: Disabled | GFSN: 132 | FSN: 132

ICDH (1) ACTIVE | FOP-1 State: [v] | Validation: Enabled | Bypass: Disabled | GFSN: 0 | FSN: 0

CECIL Information

Status	Wait (Sec)	Master Proc	Currently Executing Proc	Line
Completed	0	acs_tis200_lv_sep.pro		

Console

```

Post-config capture-----
NA
-----
Completed acs_mode_config SCO#: 0.
The current time is 2015:063:19:47:36.582
Time remaining: 90 seconds
Time remaining: 60 seconds
Time remaining: 30 seconds
Time remaining: 0 seconds
Test complete.
*****
* Writing Log Files... *
*****
Writing RT log (acs_tis200_lv_sep_rtLog_2015-03-04_19_49_36.rpt)...
Writing telemetry report (acs_tis200_lv_sep_ppTlm_2015-03-04_19_49_36.rpt)...
Writing telemetry FOF report ...
Logs saved.
End of proc.
                    
```

Debugger Proc Browser Ignore Resend Skip Suspend Go Abort Abort All

DEFAULT\_CBP

TDisplay QuickPlot CMD TSCMD Start Proc

**Workbook - [NEW]**

	A	B	C
1	Online SBC Current Spacecraft Time	2010:365:00:47:27.168	
2	<b>SPACECRAFT</b>		
3	S/C Minor Cycle Count	52896	
4	Online SBC CMM-S Interleave Depth		
5	RT Selected Packet List	7	
6	Critical Data Packet List	1	
7	Engineering Data Packet List	1	
8	ISIM Data Packet List	0	
9	CLCW -- lockout	OK	
10	VC0 - CLCW - FSN	132	
11	VC0 - CLCW - GSN	132	
12	VC0_FOP_STATE	ACTIVE	
13	VC1 - CLCW - FSN	0	
14	VC1 - CLCW - GSN	0	
15	VC1_FOP_STATE	ACTIVE	
16	CLCW Status Field	No Fault Detected	
17	CLCW FARM-B Counter (0-3)	0	
18	CLCW -- retransmit	OK	
19	CMD Auth Ground Non-Contact Timer	1323035	
20	Online SBC Invalid Transfer Frame Flag	x'0'	
21	<b>COMMAND COUNTERS</b>		
22	SBC ML Accept Counter	0	
23	SBC ML Reject Counter	0	
24	G->S/C SBC Cmd Acpt Cntr	22	
25	G->S/C SBC Cmd Rjct Cntr	0	
26	G->S/C Pkt Accept Cntr	132	
27	G->S/C Pkt Reject Cntr	0	
28	SCS Cmd Accept Counter	1	
29	SCS Cmd Reject Counter	0	
30	SCS -> JPIM Accept Count	0	



# JIST → Memory Analysis

Memory Monitor

Server Connection Status: **Connected**

Memory Space: clpA.sbc.phys\_mem

Address	Type	Symbol
0x0013af70	R	romfsImage
0x0013af70	R	romfsImageEnd
0x0013b2cc	R	ACS
0x0013b2e4	R	ACS_Actor::ACS_MODE_TRANSITIONS
0x0013b78c	R	ACS_Actor::rtg_class

Monitors (4)

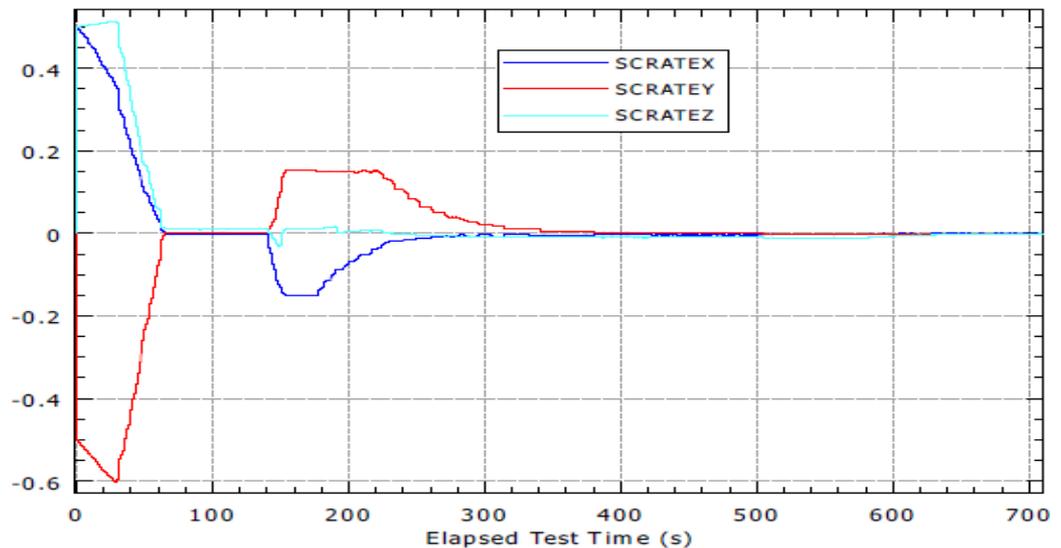
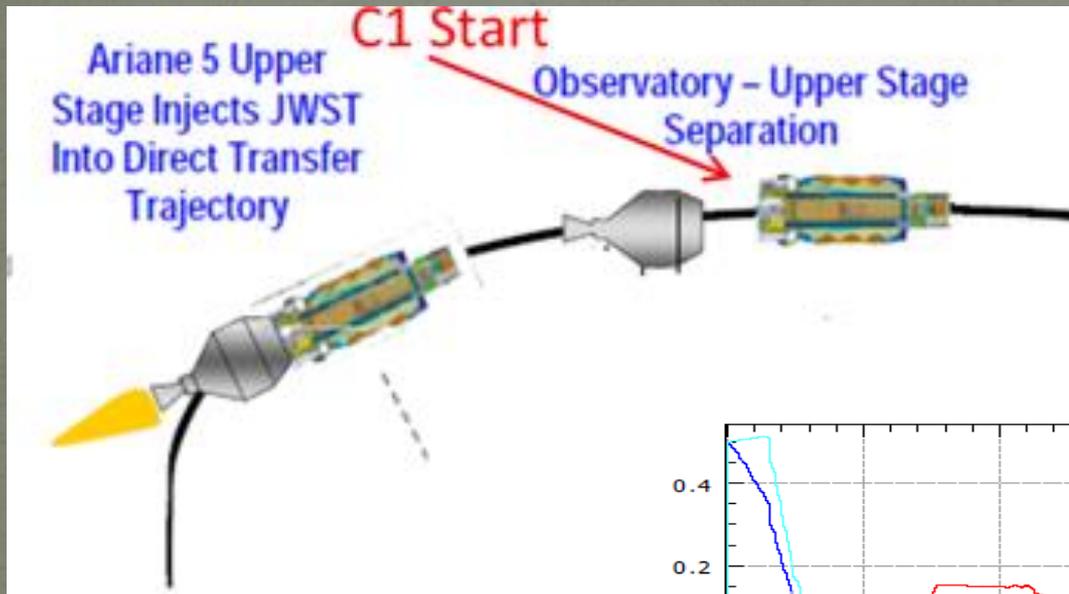
Address	Name
0x0080dca0	ACSScheduler::mcCount
0x0080dca0	ACSScheduler::mcCount
0x0080e190	ACSTim::saZIRUSCRT (X)
0x0080e190	ACSTim::saZIRUSCRT (Y)

Legend:

- ACSTim::saZIRUSCRT (Blue)
- ACSTim::saZIRUSCRT (Orange)
- ACSTim::saZIRUSCRT (Green)



# JIST → Orbit Scenarios



# JIST → Utilizations

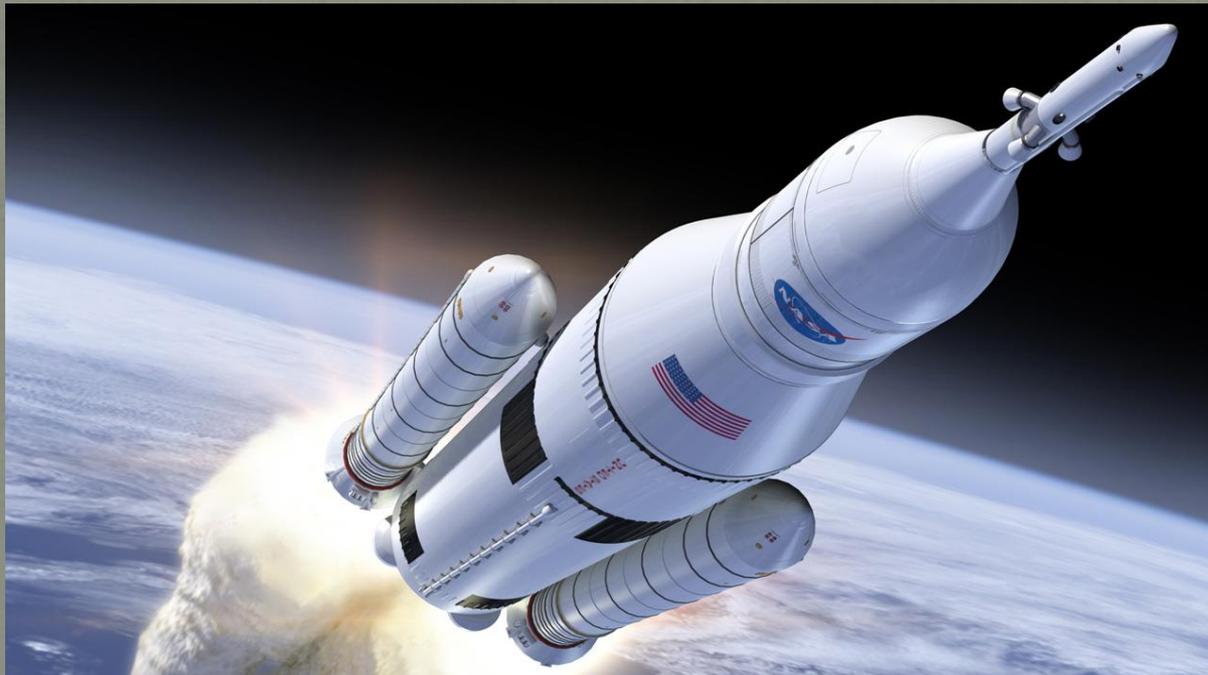
- 30 day test
- Fine-Guidance Sensor Closed-loop
- Training
- Stored Command Procedure validation
- Stuck Thruster
- PPC fault injection (Instruction faults, etc.)
- Primary/Backup Swapping
- SUROM testing

# JIST → Findings

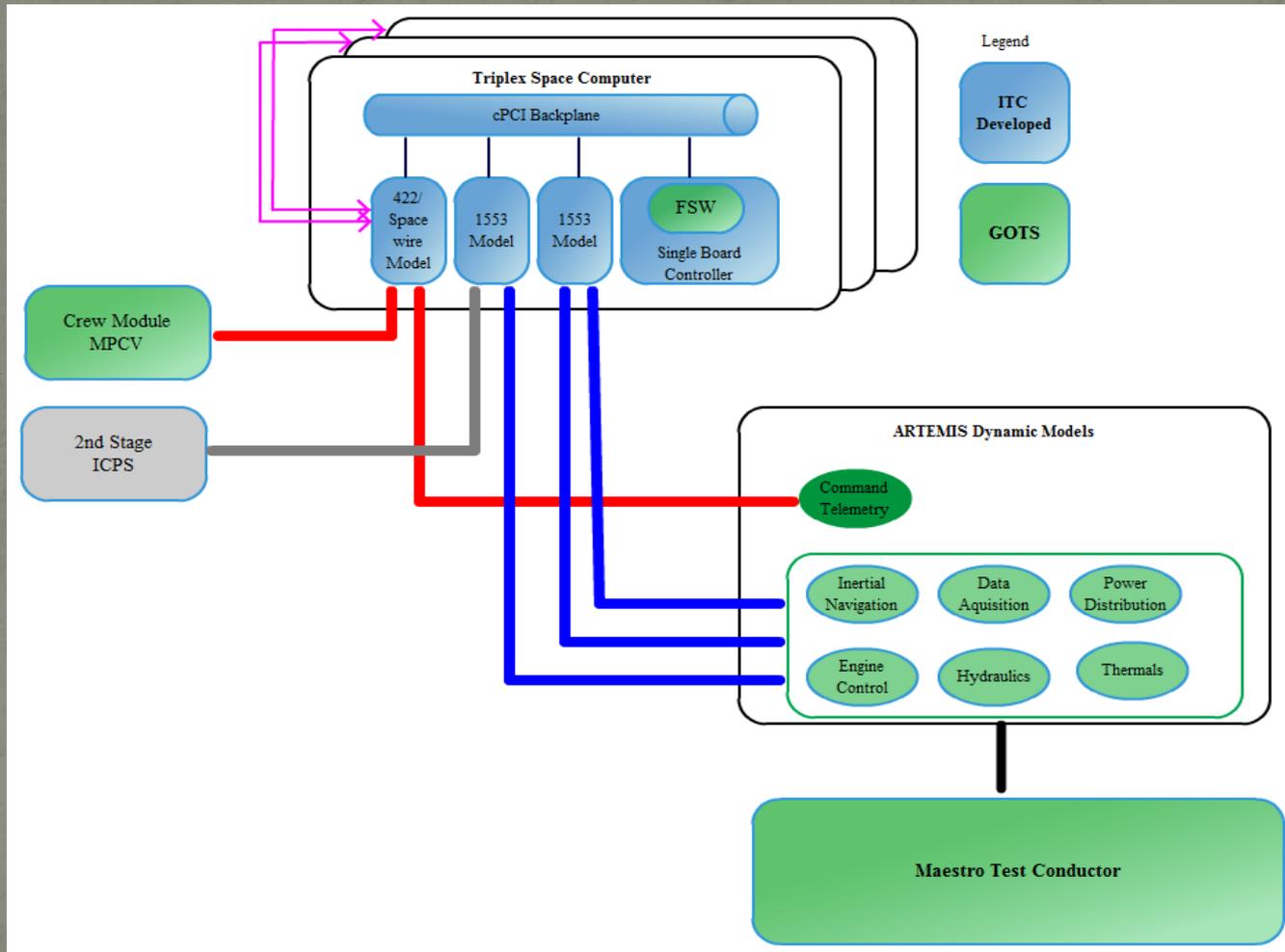
- Severity 1 issue found in Attitude Control
  - Loss of mission
- Multiple issues found in telemetry formats and processing
- Multiple issues found in test drivers when integrating them with JIST

# SLS Software-only Simulation

S3



# S3 → Architecture



# S3 → Overview

- Rolling out now to SLS IV&V Team
- Triplex Synchronization
- Integrates ARTEMIS models and dynamics
- Runs same qualification test as MSFC (Maestro)
- Similar capabilities to JIST
- Future goals:
  - Integrate GSDO and MPCV software simulators for full system simulation.

# S3 → Maestro Test Scenarios

The screenshot displays the Maestro Test Scenarios software interface, which is divided into several panels:

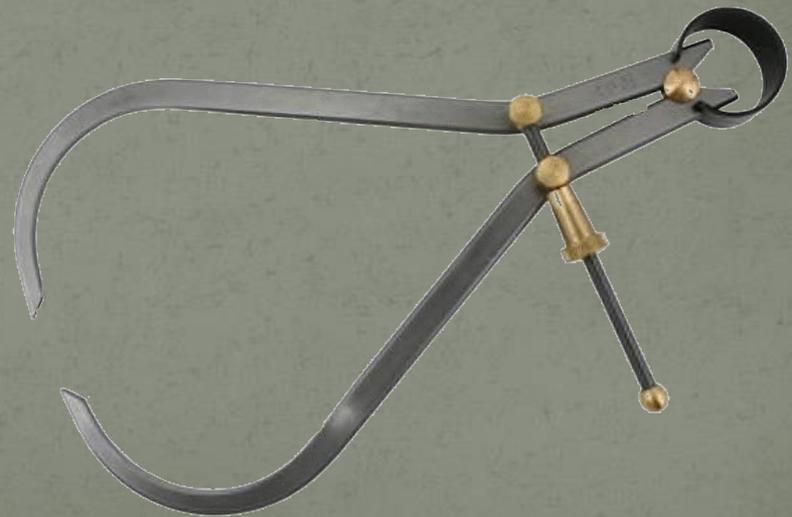
- Current Test Info:** Shows details for the selected test case, "FC2 Clear AF Chain".
  - Description: No description provided
  - Content ID: 65281
  - Slot ID: 0x0000
  - FC IDs: FC2
  - Transmission Rate: 0x0000
  - Bus IDs: AF
  - Minor Frame: 0x0000
  - Command Word: 0x0000
- Test Case Control:** A panel for managing test cases, showing a table of Test Case IDs and their status.

Test Case IDs	Run	Publish	Status
CA_SINGLEBOX_SIMICS_ITC_SLS	<input checked="" type="checkbox"/>	<input type="checkbox"/>	Running
- Message Viewer:** A log window showing system messages and test execution progress.

```
20150917 15:47:42.078 | [testers] (testers, IO_LAYER, IOLayer) INFO 0: Dev_1553,testers, ##### Simulated RT Configuration for Bus - AF-3 #####
20150917 15:48:11.861 | [testers] Waiting for "INITIALIZE" is taking a long time. Timeout occurring in "270" seconds.
20150917 15:48:16.685 | [testers] (testers, MODELS, CoreSim_SLS) INFO 0xb10: CoreSim_SLS,ARTEMIS sim start (countdown clock) -70.0000 sec
20150917 15:48:16.689 | [testers] (testers, MODELS, CoreSim_SLS) INFO 0xb11: CoreSim_SLS,ARTEMIS sim start (simulation time) 2017-12-14T09:43:37.58002Z
20150917 15:48:16.690 | [testers] (testers, MODELS, CoreSim_SLS) INFO 0xb12: CoreSim_SLS,ARTEMIS sim start (wall clock) 2015-09-17T19:48:16.68015Z
20150917 15:48:16.733 | [testers] (testers, IO_LAYER, IOLayer) INFO 0: Dev_GigE,testers, Device eth2 has IRQ: 16
20150917 15:48:16.879 | [testers] (testers, IO_LAYER, IOLayer) INFO 0: Dev_GigE,testers, Device eth2 has IRQ: 16
20150917 15:48:17.137 | [testers] Successful initialize!!
20150917 15:48:17.142 | [test_conductor] Successfully initialized ARTEMIS.
20150917 15:48:17.146 | [test_conductor] Successfully initialized ground emulator.
20150917 15:48:17.386 | [testers] Successfully issued get_io_layer command
20150917 15:48:20.549 | [testers] Entering the startTest command
```
- Summary:** A bar at the bottom showing counts for different severity levels: Fatal (0), Critical (0), Advisory (2), Info (574), Debug (0), and Removed (0).

# S<sub>3</sub> → IV&V Through Construction

- S<sub>3</sub> presented challenges due to insufficient hardware documentation
- Extensive reverse engineering of FSW was necessary to build emulator
  - Negative – Fidelity of hardware model
  - Positive – Code exposure



# S3 → Findings

- No specifics allowed ☹
- 6 issues found in Board Support Package
  - Most could only be validated using an all-software emulation
    - Interrupt and timing related
    - Bad states due to hardware failures
  - IV&V is beginning test on application code now



# Concluding...

- There are many ways to validate FSW
- Large NASA missions:
  - Are difficult to fully validate
  - Must work the first time
- ITC brings a unique capability to FSW testing