4H-SiC JFET Multilayer Integrated Circuit Technologies Tested Up to 1000 K

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This report discusses NASA GRC’s internal research effort focus on durable integrated circuits at 500 °C for > 3000 hrs.
Past work with single layer of interconnect

- Differential amplifier made in 6H-SiC operated 6519 hours at 500 °C in air ambient.
- Complexity limited. Only 2 transistors and 3 resistors.
- JFET approach good for minimizing gate leakage and durability at 500 °C.

![Graph showing input and output signals with a temperature of 500 °C and time in milliseconds.](image)

Process with two levels of metal interconnect

- Gate $N_A > 2 \times 10^{20} \text{ cm}^{-3}$ at 0.17 $\mu$m thick
- n-channel $1 \times 10^{17} \text{ cm}^{-3}$ at ~0.5 $\mu$m thick
- Lower p material $< 3 \times 10^{15} \text{ cm}^{-3}$ at ~6-8 $\mu$m thick.
Process with two levels of metal interconnect

- Ti/Ni etch mask for gate.
- Self align nitrogen implant of dose $7.0 \times 10^{12}\text{cm}^{-2}$ at 70 KeV.
Process with two levels of metal interconnect

- Ti/Ni mask use to define resistors and channels.
Process with two levels of metal interconnect

- Si mask was used for box implant of $1.6 \times 10^{15}$ cm$^{-2}$ while heated to 873 K.
- Capped and annealed at 1633 K for 4 hours in N$_2$. 
Process with two levels of metal interconnect

- Thermal and deposited oxide.
Process with two levels of metal interconnect

- Dry and wet etch of via 1.
Process with two levels of metal interconnect

- Bake out and sputter deposition of metal 1.
Process with two levels of metal interconnect

- Dry etch of metal 1.
Process with two levels of metal interconnect

- Deposited oxide 2.
Process with two levels of metal interconnect

- Dry etch of via 2.
Process with two levels of metal interconnect

- Bake out and sputter deposit of metal 2.
Process with two levels of metal interconnect

- Dry etch metal 2.
Process with two levels of metal interconnect

- Deposit oxide 3.
- Dry and wet etch of via 3 (not shown and only used for bond pads).
Process with two levels of metal interconnect

- Bake out and deposit of metal 3
Process with two levels of metal interconnect

• Dry etch of metal 3.
Two levels of metal interconnect

Processing enhancements for conformal processing on topology.

- Proximity sputtering of TaSi$_2$ (21mm target to substrate spacing).
- LPCVD tetraethyl orthosilicate (TEOS) deposited 993 K.
- Design rules for thick dielectrics and metal traces.

Enables crisscrossing traces and on chip capacitors. Now 4H not 6H
Sapphire

- 50 mm sapphire wafer was used as a “package” for testing.
- 1 µm thick Au traces with 3.175mm spacing
- Conductive die attach paste was lead oxide based with 1 µm diameter Pt particles.
We did not use the new 32 pin package. Was not finished yet.

- A new 32 pin package and circuit board was developed by Dr. Liangyu Chen for testing.
- 13 devices were tested at 737 K for duration and reported at ICSCRM 2015 last week. Ring oscillator last 3000 hours at 737K (500 °C).
Oven test

• Thermocouple (TC) was directly above die in addition to the oven’s internal TC.

• Chip pads were Au ball bonded with 25 µm wires.

• 250 µm Au wire in glass fiber insulation connected the sapphire to a terminal strip.

Note: Ring oscillator has to drive long wires to terminal strip which is not optimal for high frequency or low noise measurements.
Test thermal profile

- The wafer was at 1000 K for ~ 10 hours during processing.
- 250 µm Au wire was attached to the sapphire substrate with Au paste that was cured at 1073 K before the die was attached.
- Die attached dried at 423 K for 25 minutes then cured at 773 K for 2.5 hours.
- Electrical Data was taken to 1085 K.
- It took 7 minutes to determine the device had failed and turn off the oven at 1150K.
TLM test structure

- Larger contacts than the standard 6x6 μm via size for all other devices were used to characterize sheet resistance.
- The TLM structure and dimensions are shown.

\[ \delta = 3 \, \mu m \quad Z = 46.5 \, \mu m \quad W = 52.5 \, \mu m \quad L = 22.5 \, \mu m \]

\[ d1 = 13.5 \, \mu m \quad d2 = 67.5 \, \mu m \quad d3 = 127.5 \, \mu m \]
TLM results

• Sheet resistance derived from the 3 resistor TLM measurements.

• Follows approximately $T^2$ power law behavior except a small offset during the 21 hour 773K “burn in.”

• Specific contact resistance was $4 \times 10^{-4}$ $\Omega \text{cm}^2$ throughout the test.
Capacitor

- On chip 15 pf capacitor with an area of 0.5mm².
- Below 500K < ~1nA leakage.
- 378 µA leakage peak occurred at 686K during ramp.
- 773K “burn in” resulted in more than 5 orders of magnitude reduction in leakage current.
- Significant leakage increased above 990K.
JFET structure

• Gate length of 6 µm and width of 12 µm.
• The channel was ~ 0.4 µm thick.
• Source, drain, and gate all were the standard ~6x6 µm via.
• All traces were in metal 1.
• Device is buried under multiple TEOS layers.
JFET results

• When normalized, the on-state current ($I_{\text{MAX}}$) and the transconductance ($g_m$) matched each other as a function of temperature.

• RDS drop during the 773K “burn in” period.
JFET IV curves

- 60 Hz Digitizing curve tracer.
- At 1000K the JFET had low looping and a turn off voltage of ~ -5 V.
- As the temperature increased the looping became worse.
- Consistent with loss of back side bias contact.
3-Stage ring oscillator

• 3-stage ring oscillator was comprised of 12 JFETS and 30 resistors. Includes 2-stage output buffer.

• The output amplitude was 114mV and a frequency of 5.24 MHz at room temperature.

• VSS, VDD, and ground supplied via bus lines using the two layers of interconnect.
3-Stage ring oscillator burn in measured waveforms

- During the 21 hour 773 K “burn in” the amplitude increased from 90 mV to 120 mV.
- Also the frequency increased from 0.71 MHz to 0.86 MHz.
3-Stage ring oscillator

• The “burn in” effects can be seen on the far left.

• The frequency and amplitude decreased with increasing temperature.
3-Stage ring oscillator failure waveforms

- At 991K the waveform is still nicely shaped, but small amplitude.
- At 1037K the ring oscillator fails.
- The JFET and ring oscillator failed at nearly the same time and temperature, believed due to the loss of the back side bias contact.
- Oven was turned off at 1150K after 7 minutes of addition data acquisition.
JFET & ring osc (a) pre (b & c) post

- (b) is reflected light.
- (c) is transmitted light.
- Au trace on sapphire, backside metal of TaSi2/Pt/Ir/Pt/Au (~2 µm), and die attach material is now transparent.
- JFET is transparent
Optical and SEM of Die

• (a) front (b) is back side images of die post testing.

• Box shows were SEM (c) is imaged after die removal.

• XPS indicates all areas are lead oxide / tin oxide surfaces except the top most right corner.
SEM sample turned 180°

- Areas that look like fibers are tin oxide rich, but are predominately lead oxide.
- Au wire remains in lower left was connected to the ground pad of the ring oscillator.
- This Au wire is same wire as in slide 32 which was not connected to the bond pad after testing.
SEM closer image

• Due to the continued heating to 1150K, sequence of failure is hard to determine.

• Where did the Pt and Au (backside metal, die attach, and Au trace) go?

• Does the lead oxide flow over the Au and the Au wire before or after 1000K? 1150K?
Summary

• Pursuing circuit designs to higher temperatures has to be balanced with pursuing improved resistance thermal cycling and durability at the lower intended operating temperature of 773K.

• Short-term high-temperature electrical demonstrations are the first steps along the technical path to development of mature high temperature ICs. 1000K has been demonstrated.

• Mature technology must include a robust packaging system that can survive thermal cycling, heat soaks, vibration testing, and electrical biases, all in oxidizing environments.

For now the upper short-term peak temperature limits of SiC JFET technology remains yet to be experimentally ascertained. **It is greater than 1000K.**
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