

Printed Circuit Board Quality: Copper Wrap

NASA WORKMANSHIP STANDARDS PROGRAM

OFFICE OF SAFETY AND MISSION ASSURANCE

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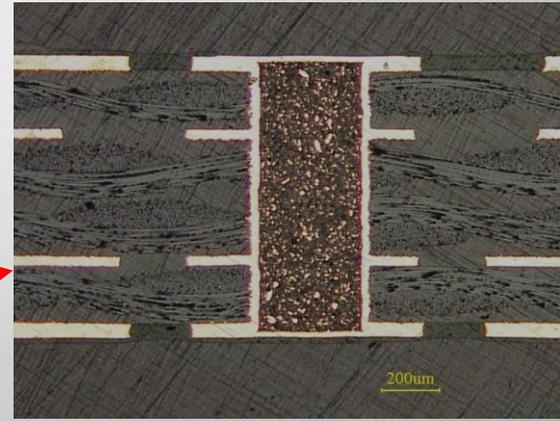
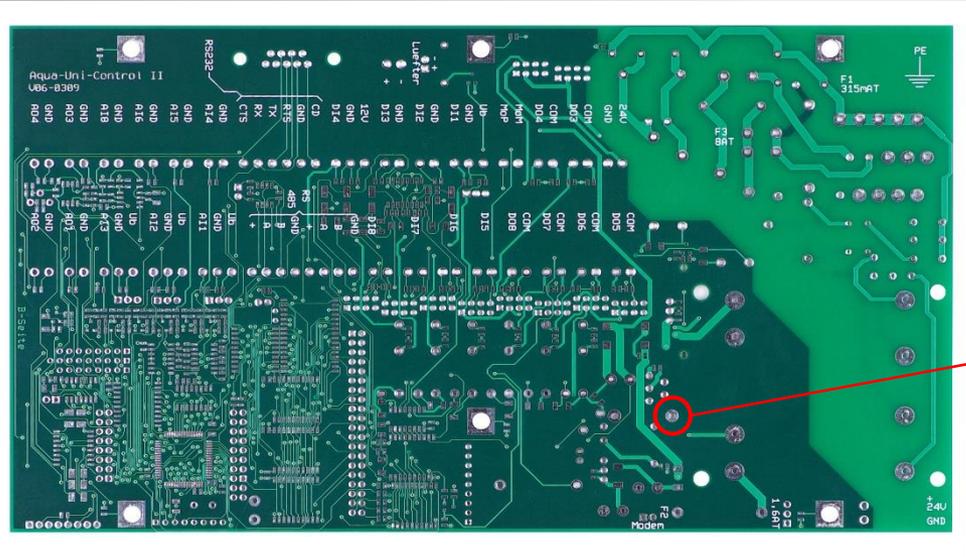
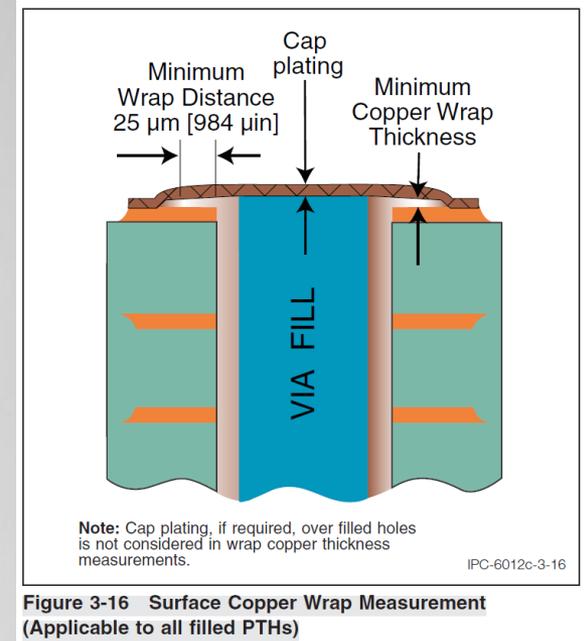
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Outline

- ▶ Motivation and introduction
- ▶ Requirements in Standards, issues
- ▶ Experimental verification
- ▶ Simulation assisted evaluation
- ▶ Lessons learned



Motivation

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High reject rates for PCBs due to specification non-conformances

Multiple rebuilds causing impactful schedule delays

- Copper Wrap
- Etchback
- Wicking
- Annular Ring

PCB Design:

IPC-2221, IPC-2222, IPC-2223,
IPC-2225

Are rejected boards unreliable?

What are PCB quality requirements for?

- Reliability: fewer cycles-to-failure?
- Manufacturability: define threshold of modern manufacturing capability?

Manufacturing Quality:

IPC-6011, IPC-6012, IPC-6012_S,
IPC-6013, IPC-6018

Who are PCB quality requirements for?

- Users?
- Buyers?
- Designers?
- Manufacturers?



What is Copper Wrap?

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The electrolytic hole plating, extending onto the surface from a plated via structure.

In certain PCB fabrication processes a planarization process reduces the wrap thickness.

Wrap Plating

The electrolytic hole plating deposition continuously extending onto the surface from a plated via structure. (See Figure W-1.)

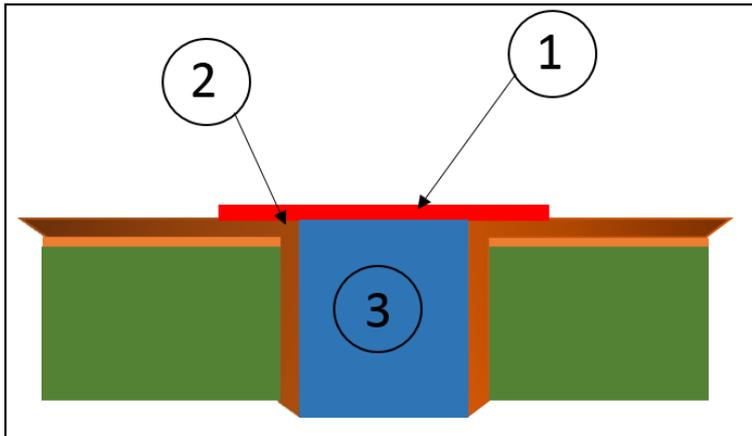


Figure W-1 Wrap Plating

1. Cap Plating
2. Wrap Plating
3. Via Fill

Butt Plating Joint (Wrap Plating)

The consequent via structure of a surface interconnect termination with the absence of wrap plating. (See Figure B-15.)

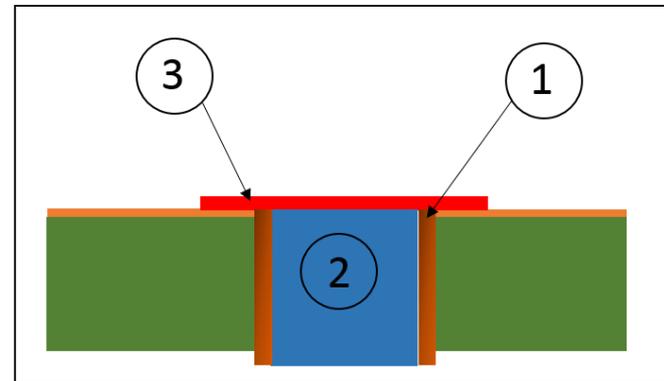


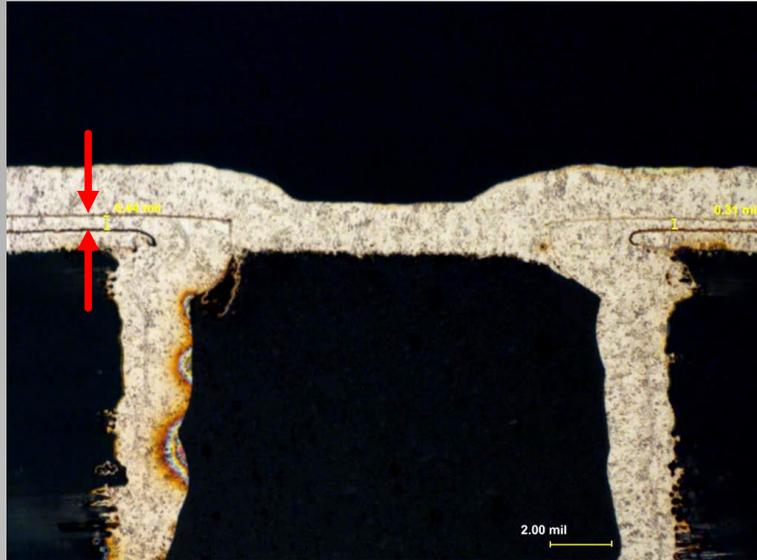
Figure B-15 Butt Plating Joint (Wrap Plating)

1. Butt Plating Joint
2. Via Fill
3. Cap Plating

Figures and text are adapted from IPC-T-50.



Minimum Wrap Thickness Requirement



Per IPC-6012 for through-holes:

| | |
|-------------------------|--|
| Class 1 | AABUS |
| Class 2 | 5 μm [197 μin] |
| Class 3 & DS | 12 μm [472 μin] |

AABUS = As Agreed Between User and Supplier

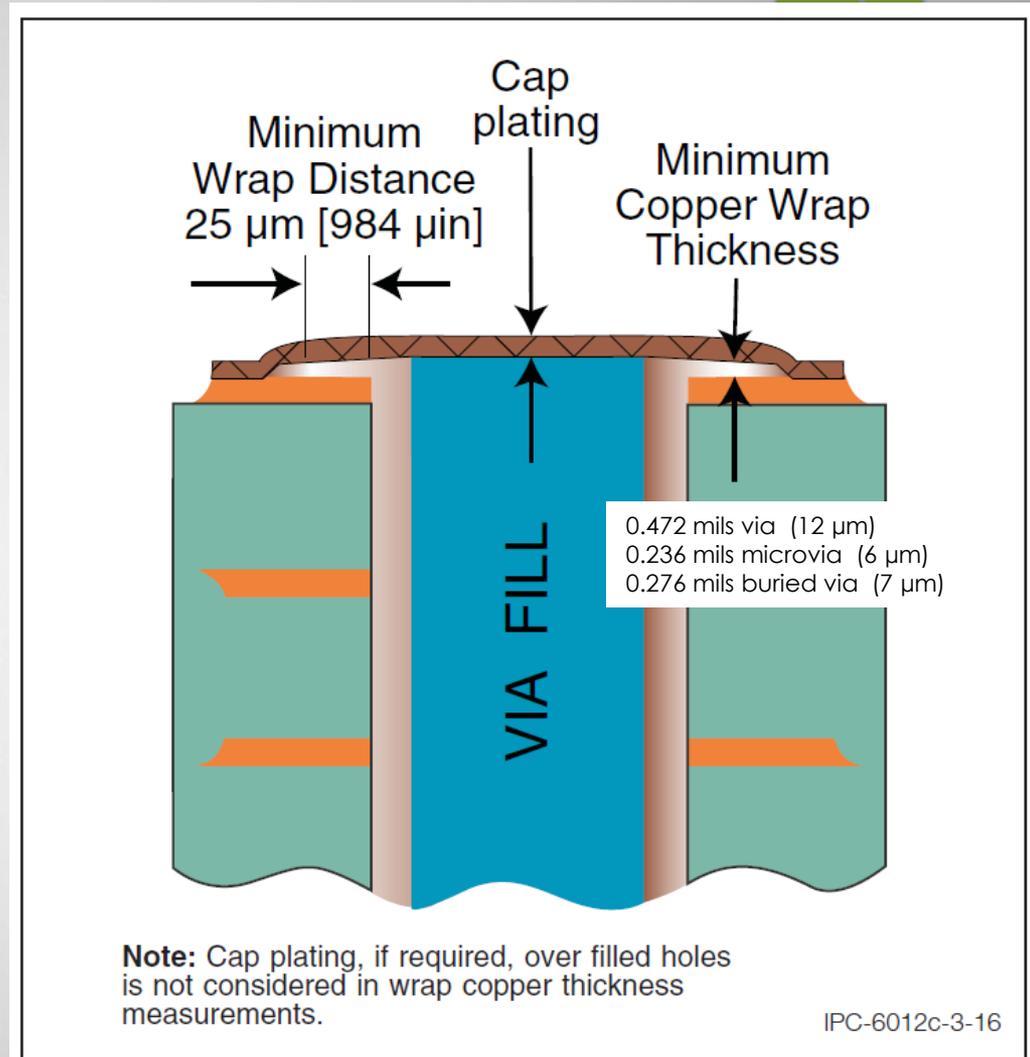


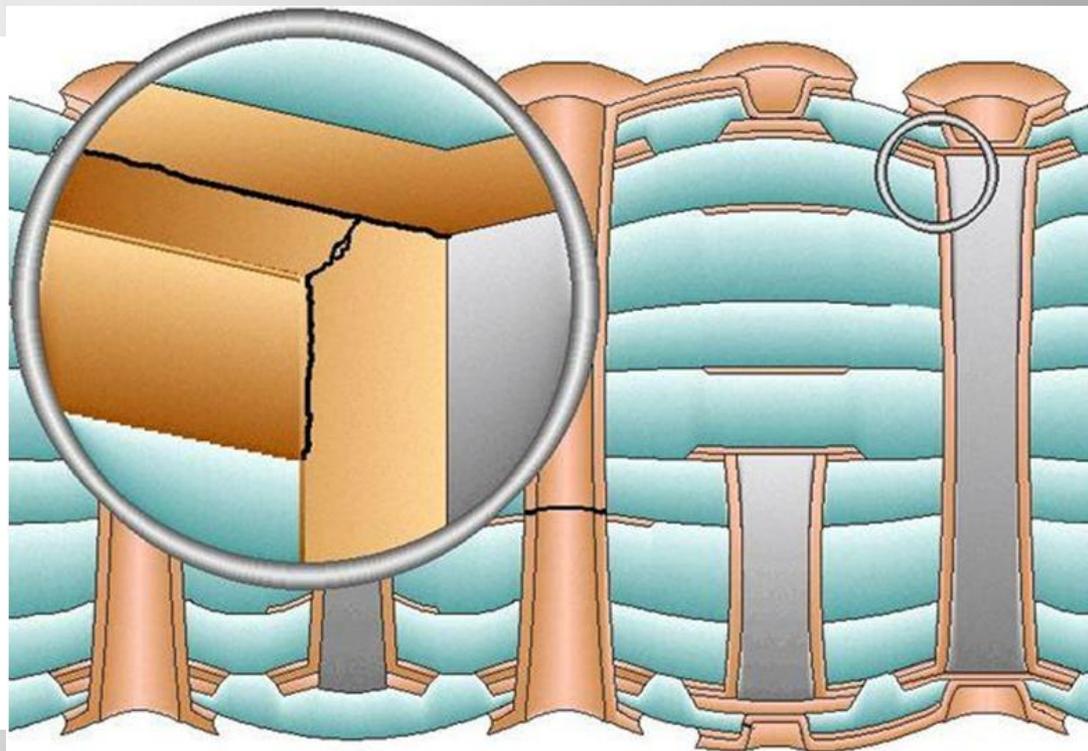
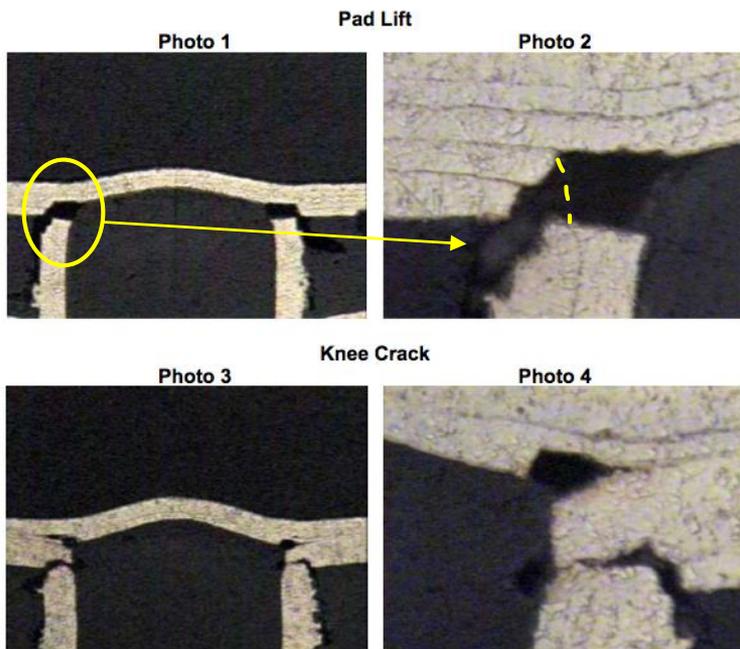
Figure 3-16 Surface Copper Wrap Measurement (Applicable to all filled PTHs)

Concern addressed with Copper Wrap: Knee Crack

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Expansion mismatches with thermal cycles creates stress on plating, fill materials and laminate interfaces.

Magnitude of mismatch is a function of temperature, CTE of the materials and number of layers.



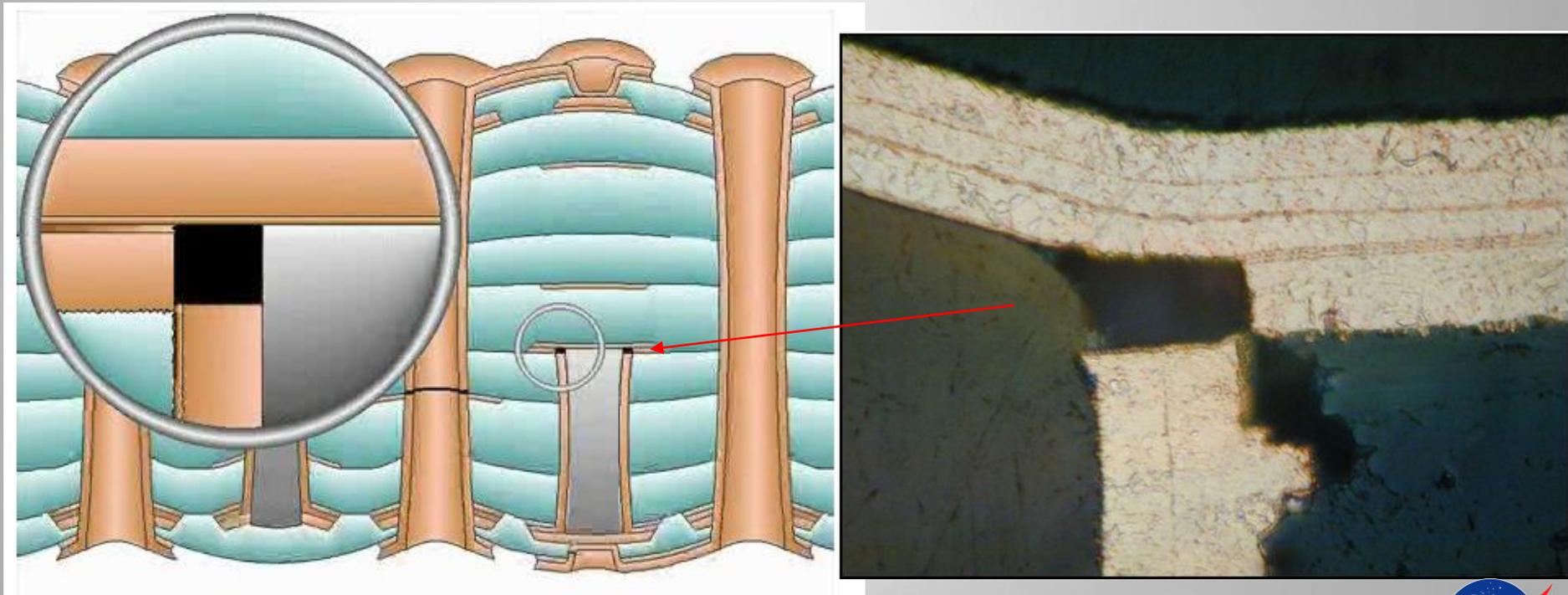
Still shot from animation of a buried via wrap crack failure
mode by PWB Interconnect Solutions Inc.

Concern addressed with Copper Wrap: Butt Joint Failures

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Expansion mismatches with thermal cycles creates stress which will adhesively separate the hole barrel plating from cap plating and other conductors

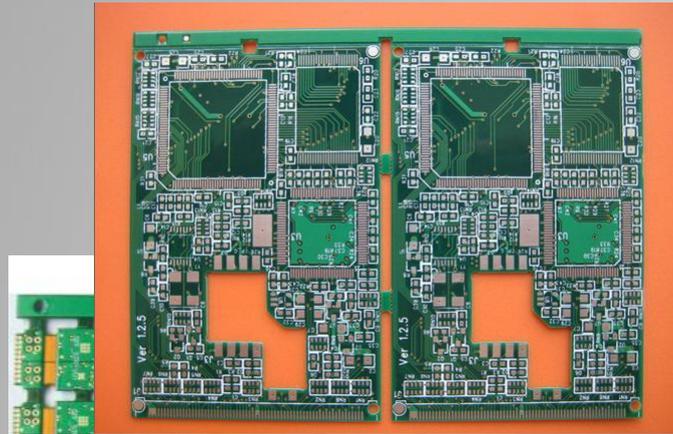
This causes intermittent open circuit failures as the board “flexes” with thermal excursions from ambient.



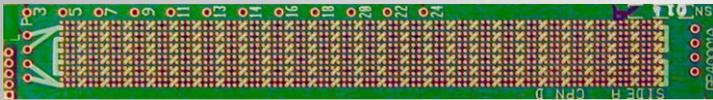
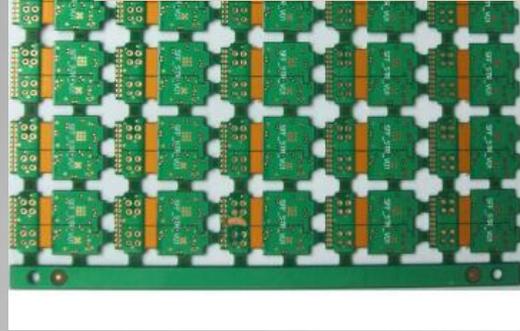
Animation available at: http://pcb.icconnect007.com/reed/reed_fig10.htm



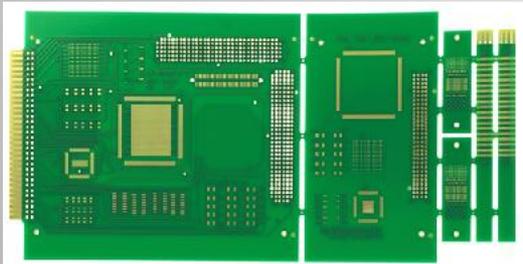
PCB Coupons



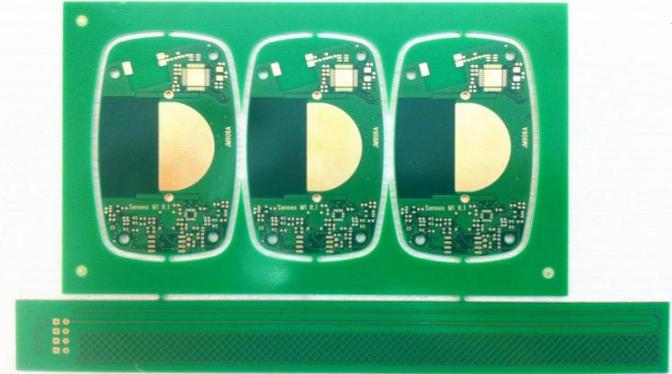
A PCB Panel may contain ≥ 1 PCBs



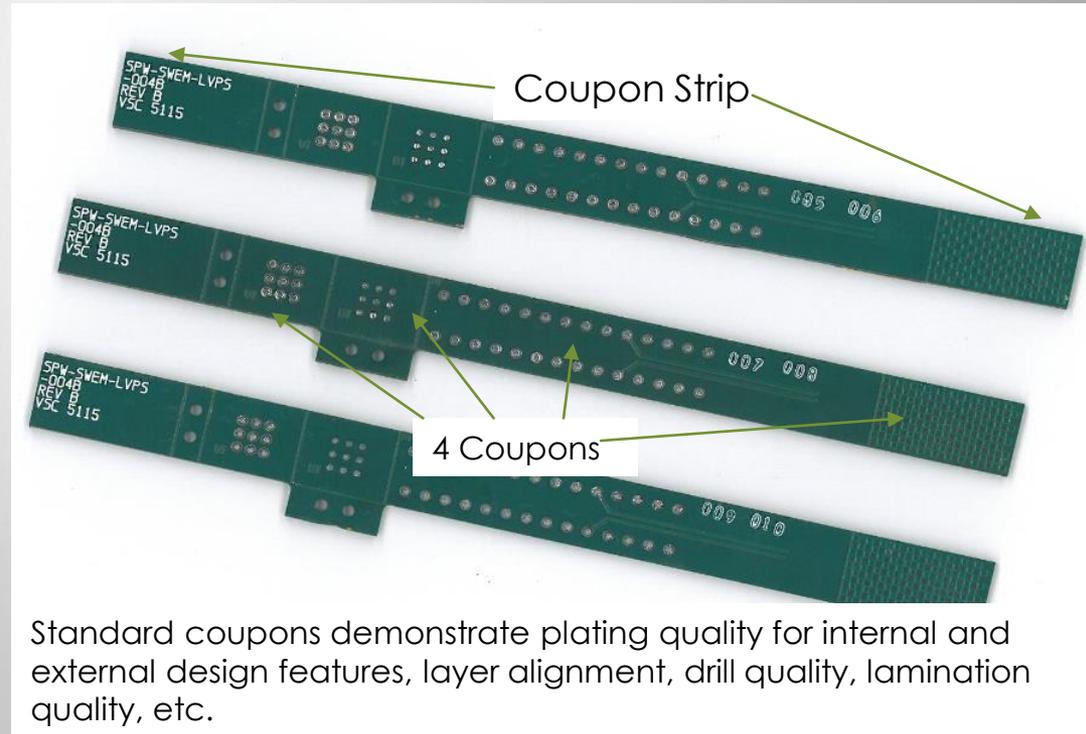
Interconnect Stress Test Coupon



IPC B52 soldering process qualification panel (multiple test coupons)



Test coupons are a part of the panel and are representatives of the quality of the boards in the panel.



Standard coupons demonstrate plating quality for internal and external design features, layer alignment, drill quality, lamination quality, etc.

Issues with requirement

0.472 mils via (12 μm)
0.236 mils microvia (6 μm)
0.276 mils buried via (7 μm)

Requirement was introduced to IPC with minimal data

- “Better” than butt joint
- 50% or 30% of Barrel plating thickness: “good enough”.

Wrap planarization process can vary the thickness by ± 0.3 mils

Wrap length of 0.985 mils cannot be achieved at required thickness for designs with tight line-width spacing and/or with multiple lamination/plating steps

No wrap requirement in ESA’s spec ECSS-Q-ST-70-11C

- Will be introduced in new “Rev 1”, projected for summer 2016



GSFC Mission Case Study

A structural integrity coupon analysis showed that the represented boards/panels did not meet the IPC-6012B Class 3/A wrap copper requirement (minimum 0.472 mils).

A detailed examination of the original microsections and additional spare coupons indicated that the wrap copper varied as follows:

1. top vias - 0.00 to 0.17 mils, bottom vias – 0.00 mils
 2. top vias - 0.00 to 0.11 mils, bottom vias – 0.29 ± 0.16 mils
 3. top vias - 0.00, bottom vias – 0.29 ± 0.15 mils
- 16 top vias and 16 bottom vias were examined from each board/panel

The detailed examination found no evidence of poor bonding between the copper foil and plating.

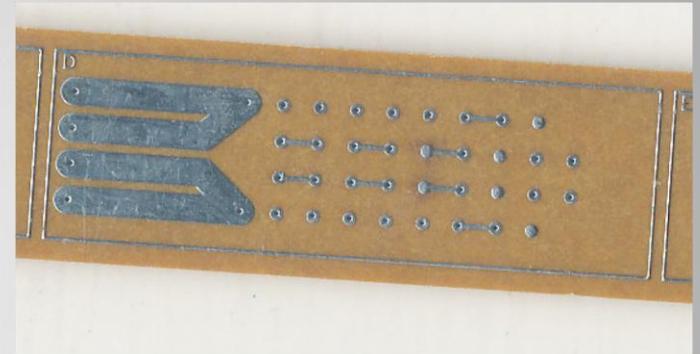
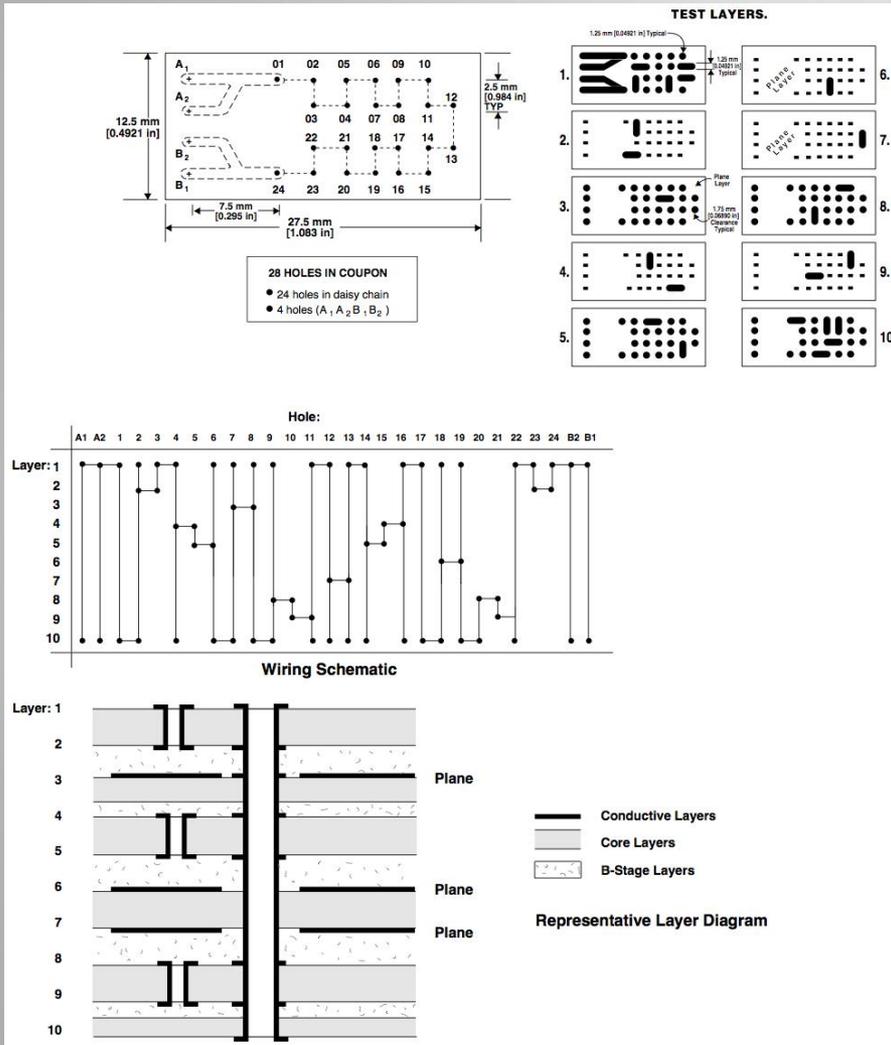
These boards were built to ECSS-Q-ST-70-11C, which does not address wrap copper.

Articles written by Paul Reid (PWB Interconnect Solution Inc.) state that *“One study showed that a wrap that is $5.0 \mu\text{m}$ [0.2 mils] thick is robust where as a wrap of less than $5.0 \mu\text{m}$ is prone to early failure.”*

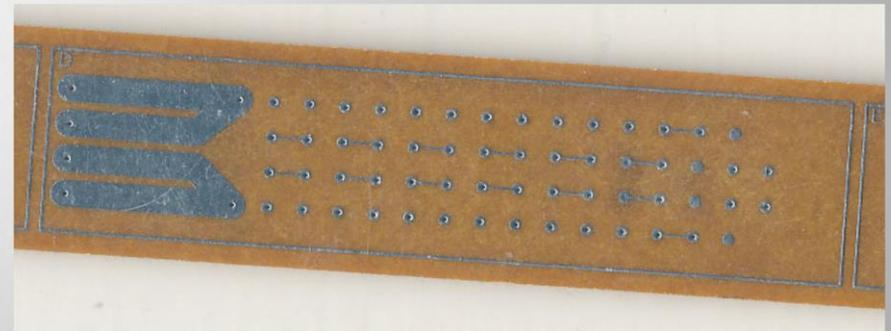
D coupons from suspect panels were thermal cycled for life testing.



D coupon for Thermal Cycling

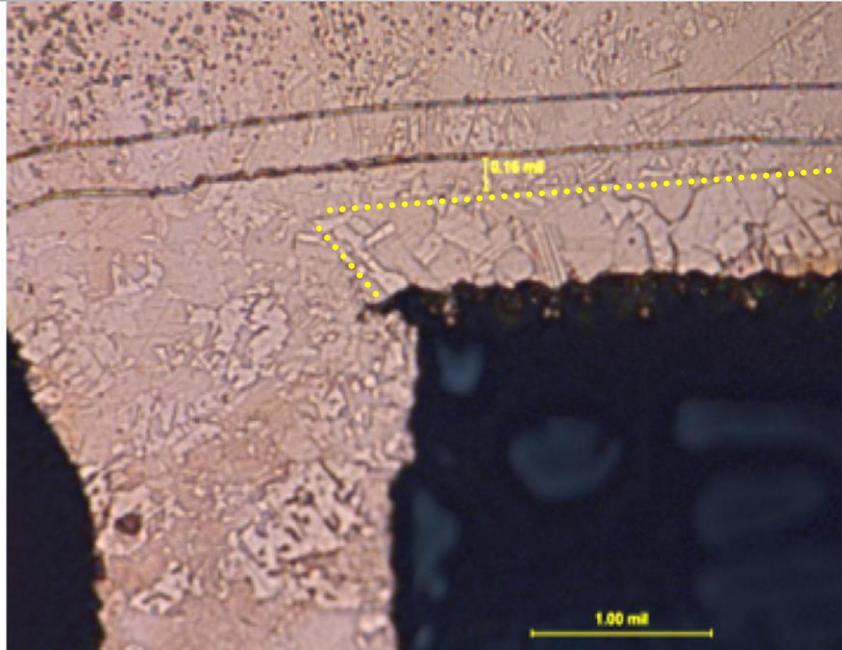


Part number SMC-00556-02

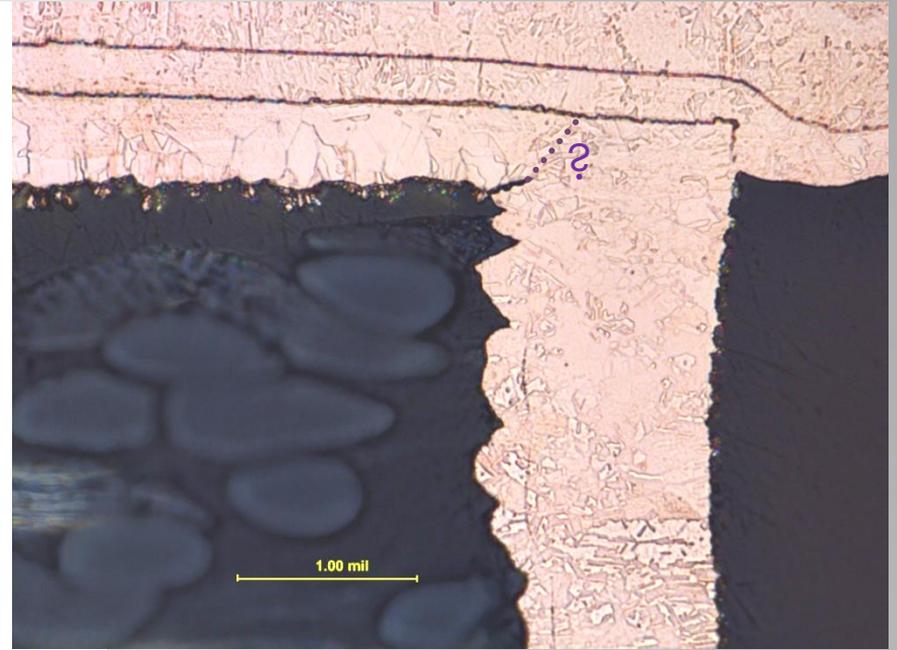


Part number SMC-00587-05

Examples of Wrap Copper Findings



Wrap copper of 0.16 mils from a micro-section for SMC-00587-05, s/n F1-1



No wrap copper from a micro-section for SMC-00587-05, s/n F1-3

Life Test Implementation



Assembly process simulation: IPC Std test method, simulate reflow soldering (+230 °C), simulate hand soldering (+288 °C) with cooling in between.

Ground testing and flight simulation thermal cycling extremes:

- IPC Std test method, 0 to +70 °C to stay close to mission conditions

More than 16,000 temperature cycles (160 mission lives):

- The first 1078 cycles: thermal shock
- The remaining 14,922+ cycles: thermal cycling

No observed trends in the absolute value of the resistance of the coupons during any of the cycling.

The applied stress conditions and cycles exceed the expected mission life.



Interconnection Stress Test (IST)

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Introduction

IST test: Applied DC current to a test coupon, the current causes a temperature rise at various conductors located in the coupon. Rapid cycling of the current is experienced as thermal cycling.

The test coupon contains a combination of heating circuits, test and monitoring nets.

IST test can simulate solder reflow temperatures (up to 260°C) and thermal cycling from ambient to 210°C.

Typically a set number of solder simulation cycles are performed followed by temperature cycles to failure.

Cycles to failure provides a figure of merit for design validation.



Copper wrap evaluation using IST

Coupons: 3 sets of vias, 14 layers, polyimide

- Through vias, blind vias open to top surface, blind vias open to bottom surface

Three copper wrap scenarios were seeded: 0.0 mils (no wrap) , 0.2 mils, 0.5 mils.

Construction, wrap thickness confirmed prior to testing using microsectioning

Soldering simulation precondition: 245°C

Temperature cycling: 25°C and 210°C

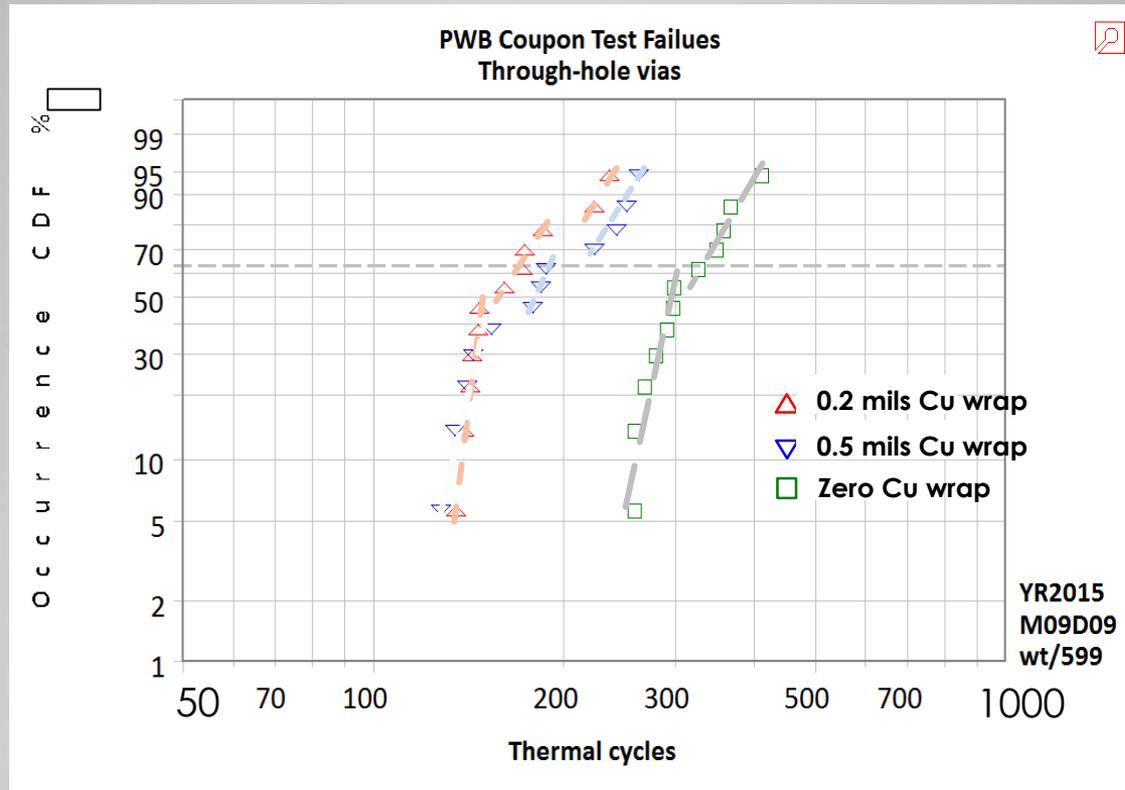
First failure: 128 cycles, through-hole via

Failures were observed in the PTH barrel of through-hole vias, a smaller number on the blind vias, and a single failure on the one layer vias.



IST Tests – Data Analysis

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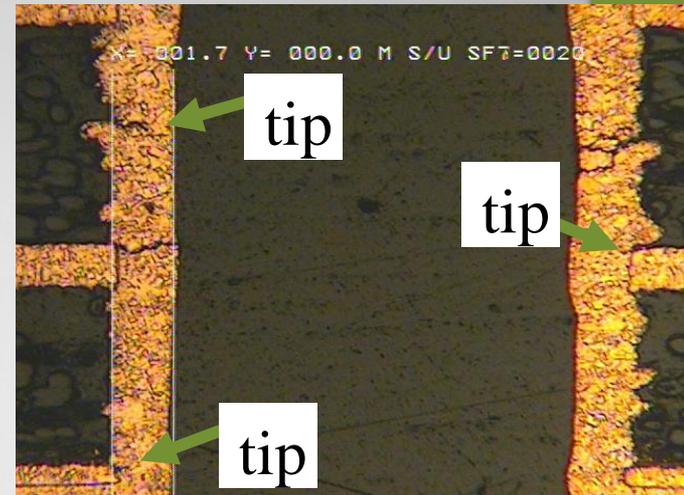
Comparison of failure distributions of PWB coupon Through-hole vias.

- The test was successful in causing failures.
- Zero copper wrap failure times were significantly greater in accelerated thermal cycle testing.
- 0.2 and 0.5 mils copper wrap coupons were not significantly different (at 90% confidence).

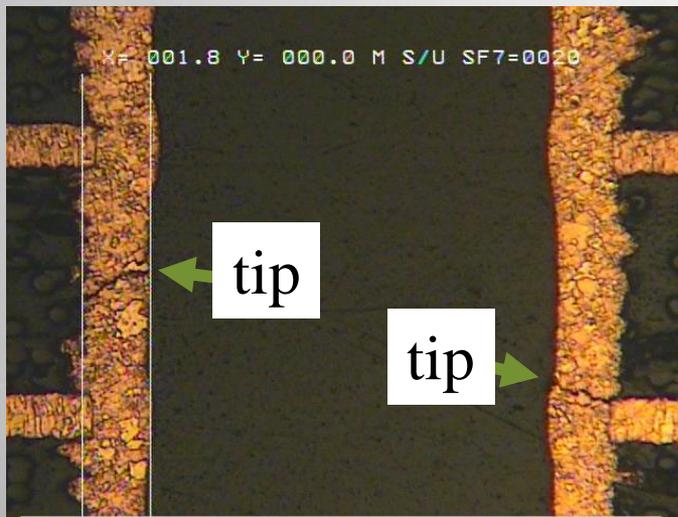


IST Test Coupons – Post Test DPA

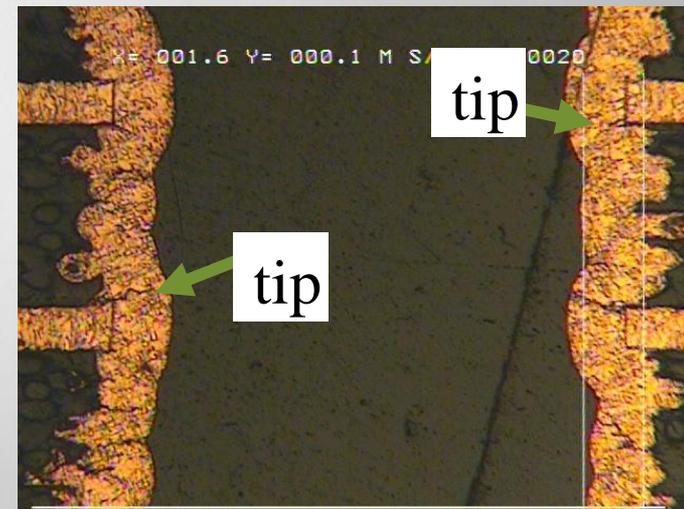
- The DPA of the IST test coupons suggests that the failure sites are at the copper barrel and not at the copper wrap as projected.
- The arrows in the images point to the crack tips. Cracks appear to be caused by fatigue, induced due to the differential in CTE between the organic PCB material and the copper barrel.



0.000 mils Copper Wrap



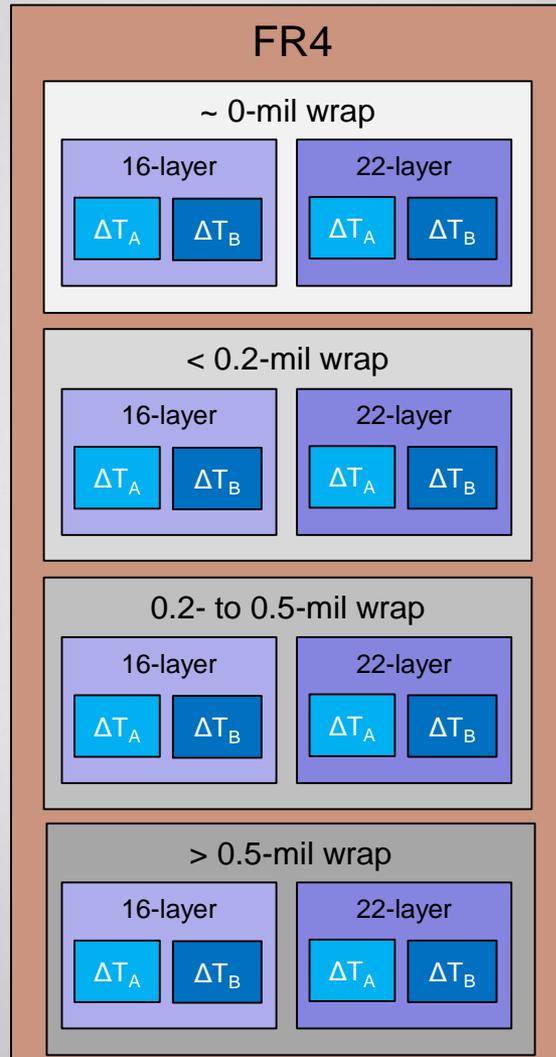
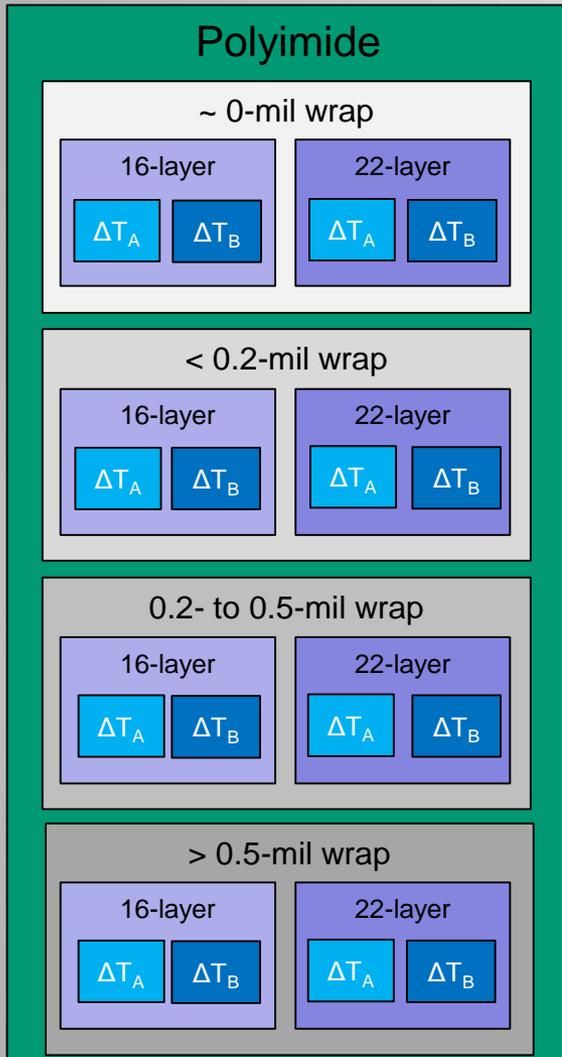
0.500 mils Copper Wrap



0.200 mils Copper Wrap

OVEN-BASED THERMAL CYCLING LIFE TEST OF COPPER WRAP

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16 unique configurations
(material, wrap, and design)

Wrap confirmed prior to test

Precondition: simulated reflow,
2X (to include rework), 216°C
peak

Thermal cycles: 500X
 $T_{A1} = -10$ to 50 °C
 $T_{B1} = -10$ to 75 °C

Thermal cycles: 200X
 $T_{A2} = 25$ to 125 °C
 $T_{B2} = -55$ to 125 °C

Electrical continuity used to find
failures during test

Microsection after testing

Results of Thermal Cycling in a Chamber for a variety of copper wrap thicknesses

No failures after 500 cycles at T_{A1} and T_{B1}

No failures after 200 additional cycles at T_{A2} and T_{B2}

No failures found by microsection.

No reliability model resulted

A wide range of wrap plating thicknesses are reliable for withstanding significant thermomechanical stress compared to typical robotic mission use environments.



Finite Element Modeling to Understand Effects of Copper Wrap

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Utilized finite element analysis (FEA) through COMSOL Multiphysics software to model plated-through-holes under thermal stress.

A steady state analysis was used, applying a 190°C boundary condition to the ambient article.

IST test samples were simulated:

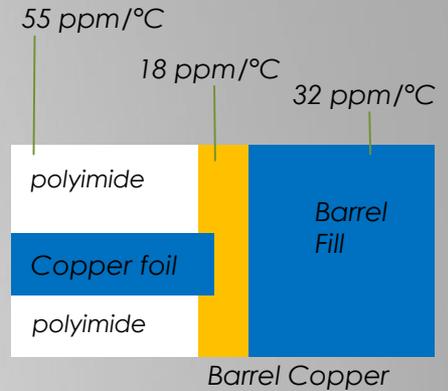
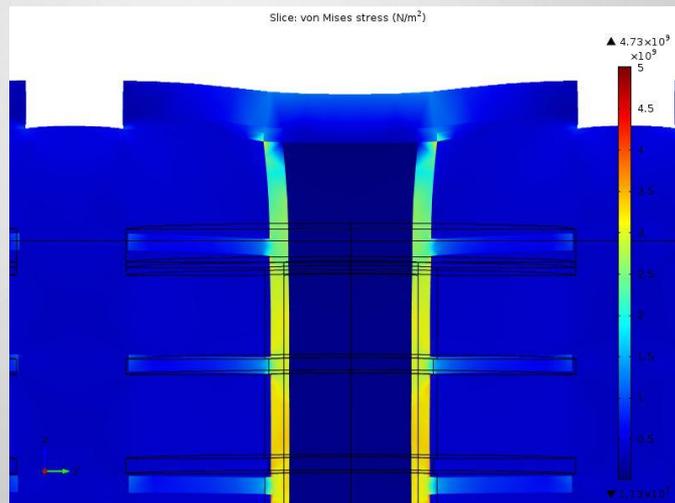
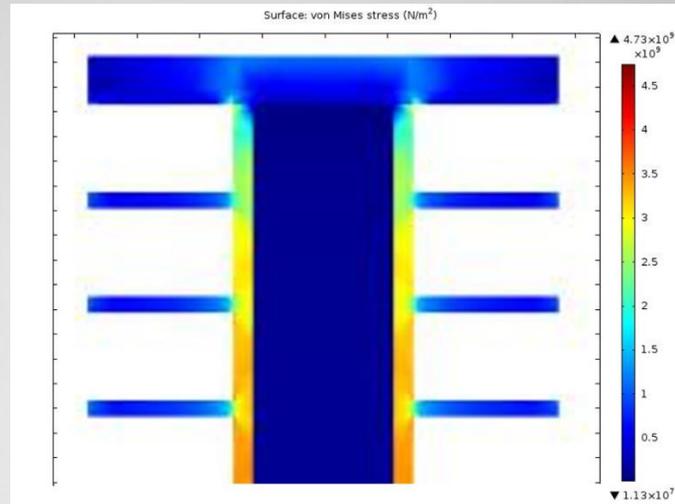
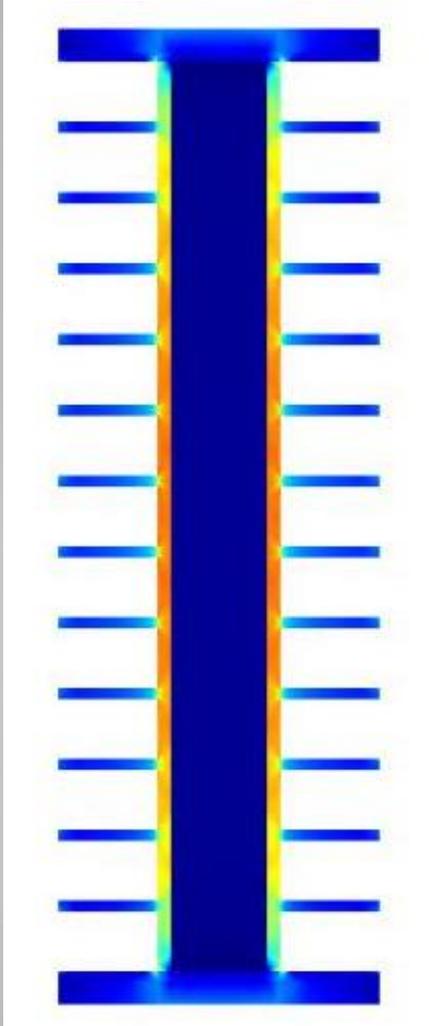
14 layers, polyimide laminate, epoxy material fill, Class 3/A quality limits

FEA modeling assumes perfect quality; effects of defects like voids or plating separations or off-nominal conditions not evaluated.



Copper Wrap Model

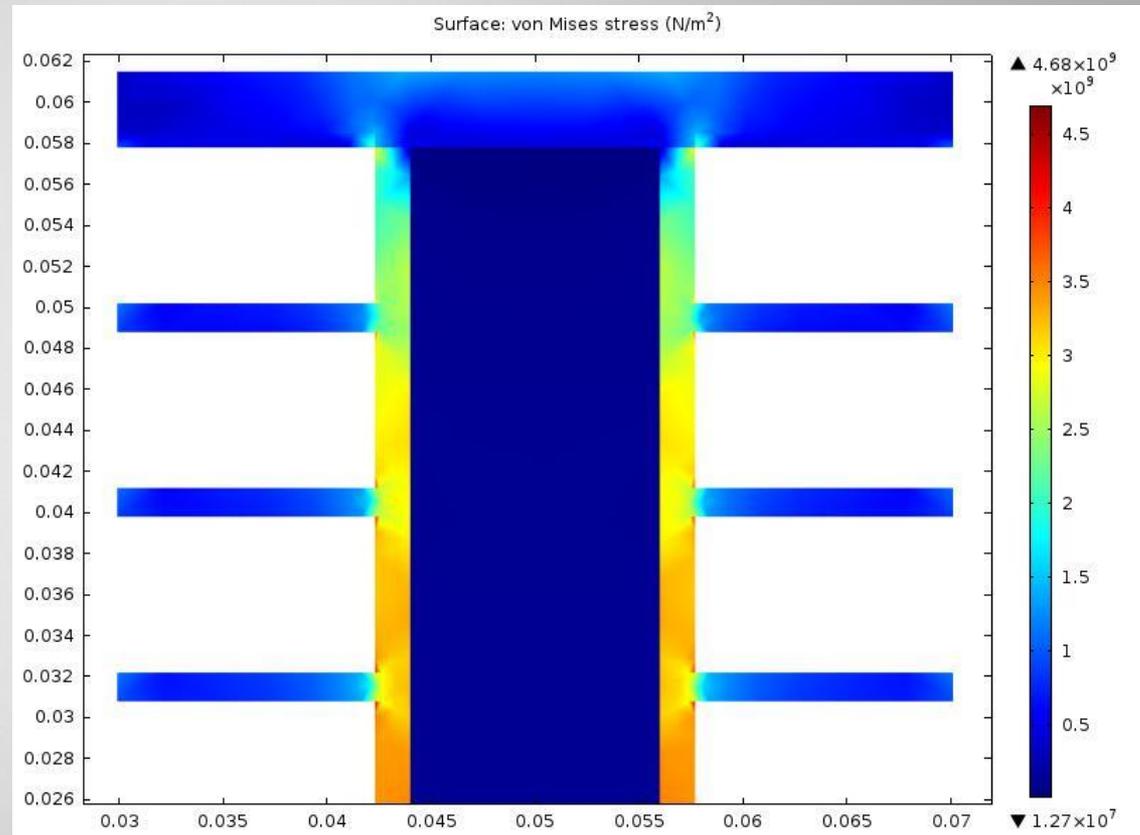
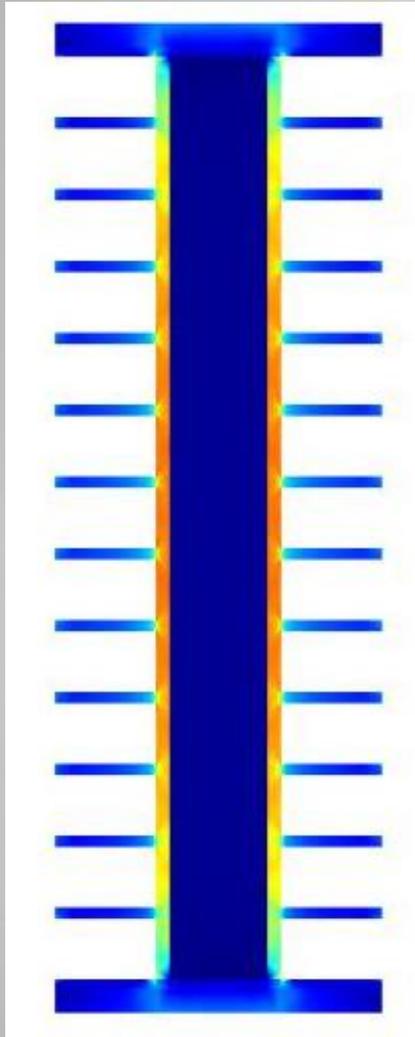
21



Shows deformation due to material expansion.

Butt Joint Model (no wrap)

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CONCLUSIONS FROM MODELING



Higher stress was seen towards the center of the PTH barrel

Copper wrap locations see less stress

The positive etchback condition creates a stress riser in the barrel

Model of no wrap did not present significant change in stress magnitude

Failure is expected to occur at the barrel, as was observed in the microsectioned test samples.

The FEA methodology allowed for identification of stress risers along the PTH geometry.



COPPER WRAP QUALITY ASSESSMENT

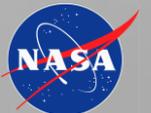


16 panels, 4 different wrap thicknesses.

Difficult to fabricate to precise targets due to large variation from planarization process

Extra microsection coupons were fabricated to characterize panel variations

4 or 7 coupons examined per panel, 8 measurements per coupon, 2 holes each



*Values in mils (1 mil = 0.001 in = 25.4 microns)

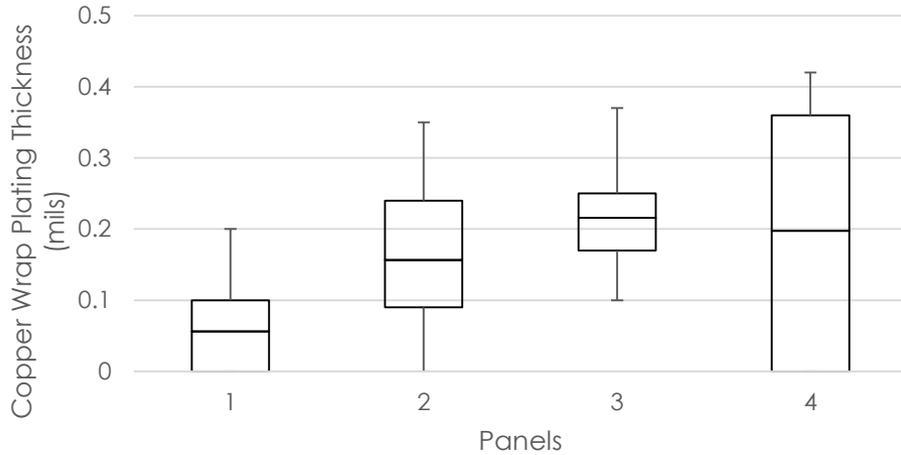
Measured Wrap Across Panel



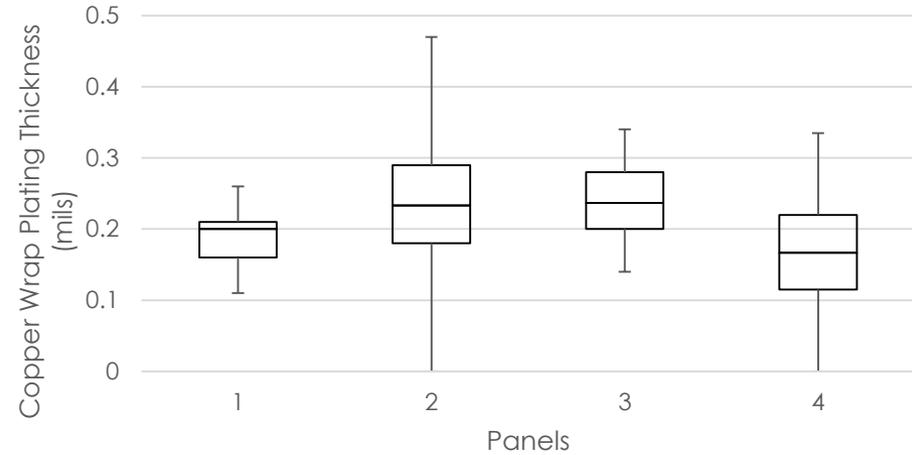
Box-and-Whisker Plots of Wrap Thickness

26

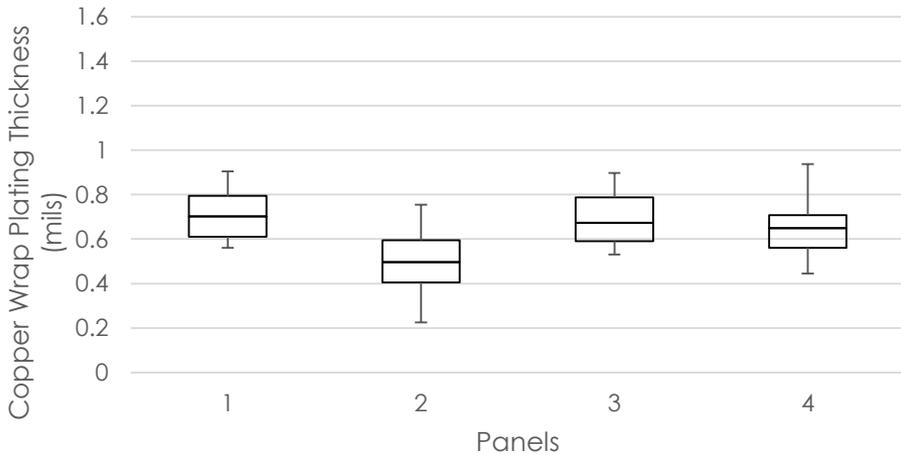
Manufactured as 0 wrap



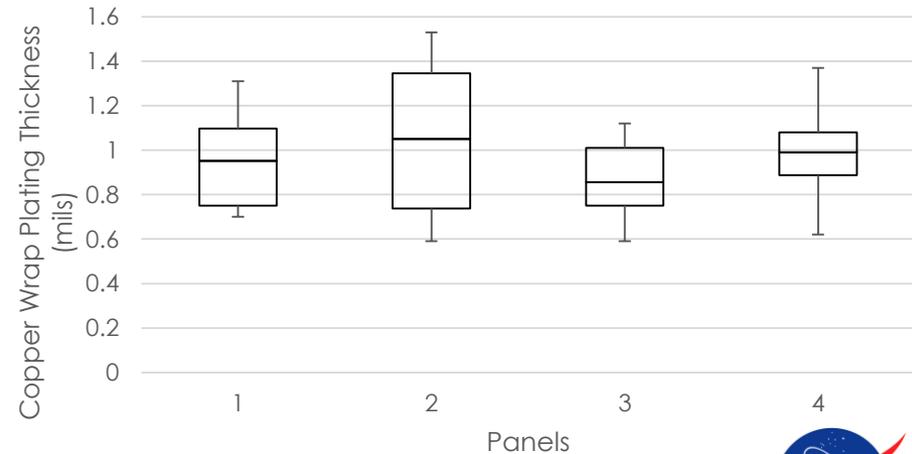
Manufactured as 0 to <0.2 mil wrap



Manufactured as 0.2 to 0.5 mil wrap



Manufactured as >0.5 mil wrap



Observations from Copper Wrap Thickness Quality

There is significant variation in the wrap thickness across each panel. The smallest observed range was 0.2 mils, and the largest was 0.94 mils.

A gradient in thickness exists across the board from top to bottom and side to side.

Despite an emphasis on controlling wrap thickness, it was difficult to achieve.

Localized variation in wrap thickness for adjacent coupons is likely minimal, while the variation from corner to corner can be large.



Correlation Between Studies

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PCBs without copper wrap were identified during coupon inspection. Experimental and simulation work was performed to understand the reliability implications of the observed condition.

Temperature cycling and thermal shock tests on coupons fabricated with polyimide and FR4 materials suggest that copper wrap location is not a dominant failure site in PTH geometries. No failures were observed in either of the studies.

DPA of IST test coupons suggests that the failure sites are located away from the copper wrap location. The earliest failure occurred at 128 cycles at a test temperature of 210°C. Comparatively, for standard polyimide, 100 cycles at 170°C is considered the acceptable limit by industry for design validation.

Software simulation confirms the IST test observations. Von Mises stress concentrations are observed along the PTH barrel when elevated temperature is applied at the boundary conditions. A periodicity in the von Mises stresses suggests that the geometry and number of annular rings plays a dominant role in the stress concentration along the plated through hole barrel.



Summary

Though copper wrap was sought as a better alternative to butt joints between barrel plating and copper foil layers, manufacturability is challenging.

Experimental and simulation work presented in this study indicates that the standard requirements for copper wrap are not contributing to overall board reliability.

PCB procurement requirements that specify minimum limits for wrap plating may drive up scrap rates and lead times by reducing manufacturability.

Experimental results corroborated by modeling indicate that the stress maxima are internal to the barrels rather than at the wrap location.

This work did not investigate the role of wrap plating in extending cycle-life for through-hole vias filled with materials that are poorly CTE-matched to the laminate. This is considered a worst case scenario for a butt joint or zero wrap condition and an unreliable design.