Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C

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Abstract. This work reports a theoretical and experimental study of 4H-SiC JFET threshold voltage as a function of substrate body bias, device position on the wafer, and temperature from 25 °C (298K) to 500 °C (773K). Based on these results, an alternative approach to SPICE circuit simulation of body effect for SiC JFETs is proposed.

Introduction

Over the past few years, significant progress has been made in the development of increasingly capable very high-temperature integrated circuits (ICs) that could benefit a variety of aerospace, automotive, and energy production systems. For example, elsewhere at this conference it is reported that a 4H-SiC Junction Field Effect Transistor (JFET) IC with two levels of metal interconnection has demonstrated 500 °C electrical operation in excess of 3000 hours [1]. Increasingly accurate and accessible IC design and simulation tools for such extreme temperatures are clearly relevant to further technology development and application adoption. Towards this end, this work reports a theoretical and experimental comparison study of 4H-SiC JFET threshold voltage ($V_T$) as a function of substrate body bias ($V_S$) and temperature (T) from 25 °C (298K) to 500 °C (773K).

Experiment

Fig. 1 schematically depicts the cross-section of the long-channel (gate-length $L_G = 6\mu$m) 4H-SiC epilayer JFET structure studied. Key structural terms illustrated in Fig. 1 include gate and substrate pn junctions, n-channel epilayer thickness $t_c$ and doping $N_{DC}$, and sub-channel epilayer doping $N_{AS}$. Experimental procedures used for device fabrication, pre-dicing wafer probe mapping of JFET $V_T$, and high temperature packaging and testing are described in [1,2].

Theory. Under one-dimensional depletion approximation [3], the depletion depth $x_n$ on the n-side of a pn step-type junction with built-in voltage $V_{bi}$ under applied pn junction bias $V_A$ is:

$$x_n = \frac{2\varepsilon_s}{q} \left( \frac{N_A}{N_D(N_A+N_D)} \right) (V_{bi} - V_A) = K_n \sqrt{V_{bi} - V_A}$$

(1)

$N_A$ and $N_D$ are junction p-type and n-type layer doping densities, $\varepsilon_s$ is 4H-SiC dielectric constant, $q$ is the electron charge constant, and junction n-side depletion constant $K_n$ defined as:

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Fig. 1. JFET Cross-sectional diagram.
\[ K_n = \sqrt{\frac{2\varepsilon_s}{q}} \left( \frac{N_A}{N_D(N_A+N_D)} \right) \]  

(2)

When the JFET gate bias \( V_G \) is at threshold voltage \( V_T \), the gate and substrate pn junction depletion depths extending into the n-channel \((x_{nG} \text{ and } x_{nS})\) merge together to effectively remove carriers (electrons) from the entire doped n-channel thickness beneath the p\(^+\) gate. At threshold therefore, the sum of the gate and substrate junction n-side depletions approximates the n-channel thickness \( t_c \): 

\[ t_c \approx x_{nG} + x_{nS} = K_{nG}\sqrt{(V_{biG} - V_T)} + K_{nS}\sqrt{(V_{biS} - V_S)} \]  

(3)

where \( V_S \) is the applied substrate junction bias. Solving Eq. 3 for \( V_T \):

\[ V_T = V_{biG} - \left( \frac{t_c}{K_{nG}} \right)^2 + \left( \frac{2t_cK_{nS}}{K_{nG}^2} \right) \sqrt{V_{biS} - V_S} - \left( \frac{K_{nS}}{K_{nG}} \right)^2 (V_{biS} - V_S) \]  

(4)

By defining \( V_{T0} = V_T \) at \( V_S = 0 \), Eq. 4 can be re-expressed as:

\[ V_T = V_{T0} + \left( \frac{2t_cK_{nS}}{K_{nG}^2} \right) \left( \sqrt{V_{biS} - V_S} - \sqrt{V_{biS}} \right) + \left( \frac{K_{nS}}{K_{nG}} \right)^2 V_S \]  

(5)

**Measured Results.** Consistent with results from our previous study of a different 4H-SiC JFET IC wafer [2], the magnitude of \( V_T \) on this wafer increased proportional to the square of radial distance \( r \) from the wafer center (Fig. 2, blue). Secondary Ion Mass Spectroscopy (SIMS) analysis was performed (by Evans Analytical Group, www.eag.com) on two diced 3mm x 3mm die taken from differing radial wafer locations with significantly different measured JFET \( V_T \). The Fig. 3 SIMS results indicate that n-epilayer thickness variation is primarily responsible for the wafer position variation of \( V_T \). Given position-invariant 1.0 x 10\(^{17}\) cm\(^{-3}\) n-channel epilayer doping \( N_{DC} \) evidenced by Fig. 3 SIMS data, Eq. 3 can extract n-epilayer thickness \( t_c \) as a function of \( r \) (Fig. 2, red), which like \( V_T \) exhibits \( y = a*r^2 + b \) general behavior. However, it should be noted that variation in p-type sub-channel doping \( N_{AS} \) at/below SIMS aluminum detection floor (~ 3 x 10\(^{15}\) cm\(^{-3}\)) could slightly affect \( V_T \) (~2 V, as seen in Fig. 4). A JFET diced from a different wafer location was custom-packaged for high temperature oven electrical testing [2].

**Comparison with Theory.** Fig. 4 plots theoretical \( V_T \) vs. \( V_S \) curves (lines) calculated via Eq. 4 using both Fig. 3 SIMS profiles assuming three different sub-channel doping densities \((N_{AS} = 1, 2, \text{ and } 3 \times 10^{15} \text{ cm}^{-3})\). Good agreement with \( V_T \) experimentally measured on corresponding JFETs (plotted as symbols) is obtained. Fig. 5 compares measured (symbols) and theoretical (lines) \( V_T \) at \( V_S = 0V, -15V, \text{ and } -25V \) from 25 °C to 500 °C from the high-temperature packaged JFET. The \( V_T \) temperature dependence arises from junction built-in voltage \( V_{biG} \) and \( V_{biS} \) temperature dependence. Fig. 5 theoretical \( V_T \) approximations fall within 15% of measured \( V_T \), which is reasonable agreement considering uncertainty in \( N_{AS} \) and \( t_c \) for this device that was not SIMS profiled.

**SPICE Model.** As SPICE [4,5] is the most broadly available electrical circuit simulation/design program, it is important to implement reasonably accurate and accessible SPICE models for 4H-SiC JFET electrical behavior. To ensure that such models can run on all variants of SPICE software,
this modeling should be implemented using baseline-version SPICE device models. However, the baseline SPICE NMOS model makes no provision whatsoever for body bias effect. Therefore, the baseline SPICE NMOS model, which importantly includes body bias effect, is instead chosen for first-order SPICE modeling of 4H-SiC JFET electrical behavior. It is important to note that this NMOS modeling approach is only valid so long as gate and substrate junctions do not become forward biased (which would draw substantial gate/substrate junction current in a physical JFET not accounted for in the NMOS SPICE model). While this general approach was previously used for 6H-SiC JFET SPICE modeling [6], this previous work did not study body bias effect. Eq. 6 shows the baseline SPICE NMOS body effect model formula for $V_T$ as a function of $V_S$ in terms of baseline SPICE NMOS model parameters PHIB, VTO, and GAMMA [4,5].

$$V_T = VTO + GAMMA(\sqrt{2 \cdot PHIB - V_S} - \sqrt{2 \cdot PHIB})$$  \hspace{1cm} (6)

Comparison of Eq. 5 to Eq. 6 readily reveals that they have the same mathematical form except for the linear $V_S$ term residing at the end of Eq. 5. For SiC epitaxial JFET IC designs of interest (i.e., those that approximate Fig. 1 with $|V_S| < 50$V), the linear $V_S$ term is numerically the smallest term of Eq. 5.

Table 1 shows two proposed mappings for substituting 4H-SiC JFET physical parameters directly into the Eq. 6 SPICE NMOS body effect model. Parameter Map #1 is obtained by directly mapping Eq. 5 terms into obviously corresponding Eq. 6 terms while completely neglecting the linear $V_S$ term at the end of Eq. 5. Map #2 features a mathematically adjusted GAMMA that approximates the impact of the linear $V_S$ term at the end of Eq. 5 within the form of Eq. 6. The $V_T$ vs. $V_S$ plots of Fig. 6 compare
Table I. Parameters for SiC JFET body effect modeling.

<table>
<thead>
<tr>
<th>SPICE NMOS Parameter [4]</th>
<th>JFET Parameter Map #1</th>
<th>JFET Parameter Map #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>VT0</td>
<td>V\textsubscript{T0}</td>
<td>V\textsubscript{T0}</td>
</tr>
<tr>
<td>PHIB</td>
<td>0.5 V\textsubscript{biS}</td>
<td>0.5 V\textsubscript{biS}</td>
</tr>
<tr>
<td>GAMMA</td>
<td>\frac{2t\textsubscript{c}K\textsubscript{nS}}{K\textsubscript{nG}^{2}}</td>
<td>\frac{K\textsubscript{ns}}{K\textsubscript{ng}^{2}}(2t\textsubscript{c} - K\textsubscript{nG})</td>
</tr>
</tbody>
</table>

these two SPICE Eq. 6 approximations against the full Eq. 5 body effect theory for the two Fig. 3 SIMS devices. As seen in Fig. 6, improved agreement with Eq. 5 is obtained for Parameter Map #2.

It is important to note that the NMOS model will crash baseline-version SPICE software when the SPICE TEMP (temperature) parameter exceeds \~300 °C. This fact precludes direct use of TEMP=500 °C simulations with baseline-version SPICE to simulate 500 °C JFET behavior starting from a 27 °C (SPICE default TEMP) NMOS model [6]. Therefore, a different/unique “500 °C” NMOS model (with parameters adjusted to match 500 °C JFET behavior) must be run with TEMP=27 to carry out baseline-version SPICE simulations of 500 °C circuits. This approach to SPICE modeling the full characteristics of 4H-SiC JFETs and circuits for temperatures up to 500 °C will be presented in more detail in future work.

Summary

This work has derived and experimentally verified equations for modeling the body/substrate bias effect of 4H-SiC n-channel epilayer JFETs over a wide range of temperature and substrate bias. Parameters for using the baseline-version SPICE NMOS transistor model for simulating 4H-SiC JFET body bias behavior have been described. This study has also ascertained that n-channel epilayer thickness variation (not doping variation) is responsible for the observed increase in V\textsubscript{T} as a function of the radial distance from the center of the experimental 76mm diameter wafer.

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