Heavy Ion Irradiation Fluence Dependence for Single-Event Upsets of NAND Flash Memory

Dakai Chen, Edward Wilcox, Raymond Ladbury, Hak Kim, Anthony Phan, Christina Seidleck, and Kenneth LeBel

1. NASA Goddard Space Flight Center, code 561, Greenbelt MD, 20771 2. ASRC Space and Defense, Greenbelt, MD, USA 20771

Abstract: We investigated the single-event effect (SEE) susceptibility of the Micron 16 nm NAND flash and found the single-event upset (SEU) cross section across geometry with fluence. The SEU cross section decreases with increasing fluence, and the change in SEU cross section is in line with the SEU sensitivity. We attribute these behaviors to the increase in the radiation hardness of the NAND flash memory as a function of increasing fluence. We did not take into account the variability in the error-rate in fluence. Therefore, heavy ion-induced SEU can be reduced with variable upset sensitivity distribution using typical fluence levels may underestimate the cross section and on-orbit event rate.

INTRODUCTION

NAND Flash memories are currently the electron-maintained storage technology in the commercial market, and this is finding that it is their space systems. The technology's high density and low cost [1]NASA and other government agencies as well as academia have devoted significant resources to further develop its materials and processes. Smartphones, tablets, and other commercial vendors, including the Micron and Samsung, are incorporating NAND memories into their products. The growing usage of this device in the defense sector as well as the continued shrinking of the memory cell area has introduced new challenges for next-generation applications.

Existing single-event effect (SEE) test standards include the JESD77, IEEE 1528, and ECDSS 2010-05-25 [2]. These test standards provide test protocols that can be used to assess SEE susceptibility of the NAND flash memory, but we provide a more detailed and practical test guideline specific to current NAND memory devices. However, the current test methodologies need to be continuously updated with new findings.

For this study, we present the methodology for the test protocol with the results of the experiments. The detailed test procedures are predicated on the assumptions that the SEE cross section remains constant with fluence. If the device upset rate in space is constant over time, then logical, typical SEE cross section. In this investigation, we observed the cross section values vary with the fluence level, which we attribute to the differences in SEU sensitivities of the individual memory cells.

DEVICE DETAILS

The MT2F91260C8DBC83 is a 16 nm NAND flash memory built on Micron’s 16 nm NAND process technology. The device is designed with a 128 Gb device is available in a plastic encapsulated ball grid array (PGA) package.

Figure 1 shows a photograph of the device. Two of the four devices in the circuit are shown in the figure. The device has four separate circuitry areas, the array circuitry, a control logic, an interface circuitry, and a temperature sensor. The array circuitry is the core of the device and the largest of the four sections. The array circuitry contains the memory cells to store the data. The control logic circuitry contains the power management and timing circuits that control the operation of the device. The interface circuitry contains the input/output (I/O) circuits that allow the device to interact with the host system. The temperature sensor circuitry contains the circuits that monitor the temperature of the device.

Figure 2 shows a photograph of the array circuitry. The array circuitry is the core of the device and the largest of the four sections. The array circuitry contains the memory cells to store the data. The memory cells are organized into blocks, and each block is divided into pages. The pages are further divided into sectors.

Figure 3 shows the single-event upset cross section as a function of the effective LET for the NAND flash. We found that the single-event upset cross section decreases with increasing effective LET for the NAND flash. The black curve represents the entire distribution of the device, and the red curve represents the number of exposed cells for irradiations with fluences of 10^8 and 10^10 cm^-2, respectively.

RESULTS

Figure 4 shows the SEU cross section across for various LETs. The black curve shows the entire distribution of the device, and the red curve represents the number of exposed cells for irradiations with fluences of 10^8 and 10^10 cm^-2, respectively.

The black curve shows the entire distribution of the device, and the red curve represents the number of exposed cells for irradiations with fluences of 10^8 and 10^10 cm^-2, respectively.

The black curve shows the entire distribution of the device, and the red curve represents the number of exposed cells for irradiations with fluences of 10^8 and 10^10 cm^-2, respectively.

CONCLUSION

The phenomenon raises serious questions regarding current test standards and conventional test methodologies with implications for future design strategies. The inverse dependence of the SEE cross section suggests that a space system carrying such a device can potentially experience a higher upset rate earlier in the mission than later in the mission. The traditional test methodology of irradiating to a fluence of 10^10 cm^-2 to lead to understanding the upset cross section and on-orbit error rate. Therefore, we may need to systematically test for various fluence levels and correlate with the mission environment. This would apply for any device with variable upset sensitivity of its sensitive volumes. It is worthwhile to include SEU flash memory technologies, because of the known variable distribution of cell upset sensitivities in flash. This can be achieved by that we can continue to reduce the fluence, the intrinsic errors will begin to overwhelm the device. With that said, the enhancement in the upset rate from 10^10 cm^-2 is not significant for this device. It is expected that a basic error correction technique such as sector-division will be sufficient to handle this. However, a critical question/concern is how will technology address this effect.

The results show how introduce a novel problem in radiation testing of a high density memory device with a non-constant upset rate. If the error rate is high enough that they cannot be corrected via error correction code, then this phenomenon will become even more critical. It is important to have an additional approach for single-event effect testing of flash devices.

ACKNOWLEDGEMENT

This work was funded by the NASA Electric Power and Propulsion (EP2) Program at NASA's Marshall Space Flight Center (MSSC) with funding provided by the United States Department of the Air Force.

REFERENCES
