Heavy-Ion Testing of the Freescale Qorivva 32-bit Automotive-Grade MCU

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Acronyms

- ADC – Analog to Digital Converter
- COTS – Commercial Off The Shelf
- CPU – Central Processing Unit
- DRESET – Destructive Reset
- DSPI – Deserial Serial Peripheral Interface
- ECC – Error Correcting Code
- EDAC – Error Detection and Correction
- eDMA – Enhanced Direct Memory Access
- HW – Hardware
- ISR – Interrupt Service Routine
- LBNL – Lawrence Berkeley National Laboratory
- LET – Linear Energy Transfer
- LQFP – Low Profile Quad Flat Pack
- MCU – Microcontroller Unit
- POR – Power on Reset
- RTC – Real Time Clock
- SEE – Single Event Effects
- SEFI – Single Event Functional Interrupt
- SEL – Single Event Latchup
- SEU – Single Event Upset
- SRAM – Static Random Access Memory
- SW – Software
Objective

• Evaluate single-event effect radiation response of inexpensive COTS automotive-grade parts, specifically a 32-bit microcontroller
  • Wider temperature range (-40°C to +125°C)
  • Guaranteed product longevity/availability
  • Built-in hw/sw safety features (ECC SRAM & Flash, Clock monitors, low-voltage detection, fault collection and reporting)

• Develop/improve internal SEE test flow for inexpensive automotive-grade microcontrollers

• Determine feasibility of test vehicle for low-cost, low-reliability apps (CubeSATS, etc) \(\rightarrow\) low-power

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Key Questions

• Does this device perform “well-enough” under heavy-ion irradiation to be recommended for ultra-low cost missions or instruments (CubeSATS and the like)?
  • Not qualification, but a starting-point for system design
  • It’s going to upset, but what are the common error signatures?

• What results can we derive from heavy-ion testing using a commercially-available evaluation system for this microcontroller?

• What considerations do we need for testing (especially with limited time and money)?

• What issues may arise with automotive-grade parts in general?
Device Under Test

- Freescale MPC56xx Family
  - 32-bit Power Architecture MCU
  - Automotive/Industrial applications
  - Specific Part: SPC5606B (S prefix = “automotive-qualified”)
    - 90nm Power Architecture e200z0 core
    - 1 MB Flash memory
    - 80 KB ECC SRAM
    - 64 MHz Processor Core
    - 144 LQFP (plastic)
    - Temperature Range -40 to +125 °C
- Commercial Evaluation Board
Test Considerations

• Assume choice of automotive microcontroller driven largely by cost
  • Limits ability to test in application-specific manner (testing isn’t cheap…)

• But, any microprocessor or microcontroller is a complex part...

• Large number of complex elements each capable of affecting radiation response (power, memory, core, peripherals, interrupts, timers, etc)

Test Software Components

- **DSPI** (Deserial/Serial Peripheral Interface) – loopback test of communications peripheral.
- **eDMA** (enhanced Direct Memory Access) – Moves block of data in SRAM using software handshaking and interrupt-driven error-detection.
- **Memory EDAC** – Uses internal ECC module (single-bit correct, double-bit detect) to report bit upsets in SRAM and flash memory, as well as bus access issues (flash stall/abort).
- **Math** – Prime number testing to load-test arithmetic units
- **ADC** – Interrupt-driven test of ADC peripheral reports if analog value departs expected range. Reports back number of successful conversions.
- **Software Watchdog** – Serviced by Periodic Interval Timer (ISR). If service routine fails to reset watchdog (CPU is locked up or program execution stops) board is automatically reset. Software will report any resets.
- **Reset Generation Module** – Board will be functionally reset by software if other test modules’ counters fail to increment for some reason.
- Individual test programs to characterize **low-power sleep mode** performance and to focus on individual items from above list as necessary.
- Additionally, there is built-in **low-voltage detection** for the 1.2V core supply that will reset the device. Any POR, whether intentional or due to low-voltage event, will be logged.
Radiation Test Conditions

- Testing at LBNL 88” Cyclotron
  - Ion Species Used: B, O, Ne, Si, Ar, Cu, Kr, Ag @ 10MeV/AMU tune
  - Nominal LET Range: 0.89 to 48.15 MeV*cm²/mg
  - Angular Testing up to 45 degrees (effective LET 68.09 MeV*cm²/mg)
  - Room temperature exposures in vacuum

![BASE Ion List](http://cyclotron.lbl.gov)
Test Setup

• Customized self-test software (C code) running on target MCU during irradiation
• Data output via RS232 to PC (one-way monitoring only)
• Power supply logs of main +12V power to motherboard
Summary of Results

• Testing started with lowest LET available and gradually increased

• At low LET (<1 MeV*cm²/mg) we only recorded:
  • Single-bit SRAM upsets (low cross-section – 3.3x10⁻⁷ cm², automatically corrected by EDAC)
  • Rare CPU reset events *not* associated with increased power consumption (we’ll call these SEFIs)

• As LET increased we saw increasing single-bit upset cross-section (and eventually disabled logging of that event), occasional double-bit errors, and rare peripheral errors, but *reset events (now associated with high current) began to dominate the test*

• No parts were rendered inoperable during testing. Processor lockups were often self-recovered when high current caused an undervoltage condition.
SEL & SEFI Cross-Section

- DRESET ("destructive" reset) is an error flagged by the MCU as it comes out of an unexpected reset.

- At higher LET these were associated with recovery from a high-current state (SEL).

- But at low LET (<~8 MeV*cm²/mg) no high-current events were noted (SEFIs)

Curve shape hints at two separate curves overlaid – low-threshold/low-saturation and high-threshold/high-saturation
High-CURRENT Events (SEL)

• Supply current to motherboard is a single +12V line
  • Current limited, but typical “high-current” event did not reach supply’s limit
• But, +12V supply is internally regulated on-board and on-chip:
  • $V_{DD_{LV}}$ is 1.2V core voltage, with maximum specified output current of 150 mA
    • This closely relates to the peak seen during high-current events
Low-LET SEFI Events

• Runs at lower LET (\(<\sim 8 \text{ MeV*cm}^2/\text{mg}\)) showed processor resets that were not associated with high-current spikes.

• Critically, these were NOT sufficient to induce automatic reset due to overcurrent and internal watchdog timer did not always function → an external watchdog is recommended to reliably initiate POR.
Breakdown of Reset Events (SEL/SEFI)

- Two distinct responses – low-current resets at low LET, high-current resets at high LET
- No high-current events below LET of 8 MeV*cm²/mg, but above 20 they dominate all other events.
Low Power Standby Mode

• Microcontroller can be put into a powered-down standby mode to conserve power (<100 uA) while monitoring for external interrupt signal

• Two tests performed:
  1. Device in standby with periodic wake-up from internal RTC
  2. Device in standby with external interrupt wake-up

• Even with low LET (3.49 MeV*cm²/mg) the device can get stuck in a sleep mode where it could not wake itself – occasionally this was accompanied by a power increase

• External interrupt-driven wakeup was more reliable.
Low Power Standby Mode Examples

Run 15 (LET 3.49 MeV*cm²/mg)

- Unexpected reset events during standby
- Normal wake-up/sleep cycles (driven by RTC)
- High current and MCU unresponsive (req. ext. POR)

Run 19 (LET 6.09 MeV*cm²/mg)

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Other Error Events

• Events noted at low LET where resets were far enough apart to allow full self-test loops to consistently complete:
  • Single bit errors in SRAM common, threshold < 0.89 MeV*cm²/mg
  • Double bit errors in SRAM, threshold < 3.10 MeV*cm²/mg
  • Single bit flash errors, threshold < 3.10 MeV*cm²/mg
    • Note: no uncorrectable flash errors
  • One ADC readback error, threshold < 3.10 MeV*cm²/mg

• Other events noted at higher LET (frequency of resets made it difficult to complete self-test loops):
  • DMA transfer errors
  • Possible UART hits
  • DSPI halt

Insufficient data on any of these events to provide cross-section (or really even a good threshold).
Summary

• Internal ECC functionality helps reduce (but not eliminate) soft-errors in program memory

• As expected, SEFI and SEL dominate the device response
  • May recover on its own if onboard voltage regulator limits exceeded
  • May not recover from SEFI (even with internal watchdog enabled)
  • Not immune from events during low-power sleep modes

• May be useful as an inexpensive off-the-shelf part, but far from a “rad-hard” part → Could use app-specific testing to better define expected performance, and on-board mitigation needed to recover from certain events

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