A multi-step silicon etching process has been developed to fabricate silicon-based terahertz (THz) waveguide components. This technique provides precise dimensional control across multiple etch depths with batch processing capabilities. Nonlinear and passive components such as mixers and multipliers waveguides, hybrids, OMTs and twists have been fabricated and integrated into a small silicon package. This fabrication technique enables a wafer-stacking architecture to provide ultra-compact multi-pixel receiver front-ends in the THz range.

18 Claims, 6 Drawing Sheets
OTHER PUBLICATIONS


* cited by examiner
FIG. 11

Port 'b'

OMT and Twist

Port 'a'

11.5mm

FIG. 12

Insertion Loss (dB)

Frequency (GHz)
MULTI-STEP DEEP REACTIVE ION ETCHING FABRICATION PROCESS FOR SILICON-BASED TERAHertz COMPONENTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of U.S. provisional patent application Ser. No. 61/812,097, filed Apr. 15, 2013, which application is incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY FUNDED RESEARCH OR DEVELOPMENT

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT

Not applicable.

INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

Not applicable.

FIELD OF THE INVENTION

The invention relates to silicon wafer fabrication methods in general and particularly to fabrication methods that employ deep reactive ion etching (DRIE). 

BACKGROUND OF THE INVENTION

THz instruments are being proposed as highly sensitive instruments for remote sensing of planetary atmospheres on Mars, Venus, Jupiter, Saturn and Saturn’s moon Titan. For these long-term planetary missions, severe constraints are put on the mass and power budget for the payload instruments. For example V. M. Lubecke, K. Mizuno, G. M. Rebeiz, “Micromachining for terahertz applications”, IEEE-MTT, pp. 1821-1831, 1998. Conventional approaches which package the receiver components in CNC machined metal waveguide blocks are too massive and expensive for multi-pixel instruments that fit within these tight budgets. Several different micromachining techniques exist for fabrication of terahertz circuits. One process forms the waveguide and device structures directly from permanent resists such as SU-8, as is described in J. Stancee and N. Barker, “Fabrication and integration of micromachined submillimeter-wave circuits,” Microwave and Wireless Components Letters, IEEE, vol. 21, no. 8, pp. 409-411, August 2011. This technique, while requiring a minimum of processing tools, suffers from significant process instabilities and delamination issues between the thick resist and carrier wafer.

LIGA-based processes use thick resists to form a mold for electroplating, as described in C. H. Smith, H. Xu, and N. Barker, “Development of a multilayer SU-8 process for terahertz frequency waveguide blocks,” Microwave Symposium Digest, 2005 IEEE MTT-S International, pp. 439-442, June 2005. This has the advantage of producing a metal structure and is therefore easier to couple to standard metal waveguide components. However, both of these processes suffer from non-uniformity issues that require an additional processing step, such as lapping, to planarize the final device.

There is a need for ultra-compact receiver architectures to reduce the mass and size of the receiver while increasing the circuit density of the device.

There is a need for fabrication methods that will permit the accurate fabrication of such devices in silicon.

SUMMARY OF THE INVENTION

According to one aspect, the invention features a method of manufacturing a terahertz waveguide circuit element. The method comprises the steps of providing a silicon wafer having a surface; providing a SiO$_2$ layer having an initial thickness on the surface; etching a plurality N of SiO$_2$ patterns in the SiO$_2$ layer; and performing a silicon etch simultaneously on all of the plurality N of SiO$_2$ patterns having a respective thickness representing a respective depth of etching into the silicon wafer, the respective thicknesses being different from one another, where N is an integer greater than one; and repeating the total of N times in succession the two steps of performing an SiO$_2$ etch simultaneously on all of the plurality N of SiO$_2$ patterns to expose a respective region of the surface of the silicon wafer beneath the thinnest remaining one of the plurality N of SiO$_2$ patterns; and performing a silicon etch simultaneously on the silicon wafer below all of the exposed respective regions of the surface of the silicon wafer.

In one embodiment, the step of providing a SiO$_2$ layer on the surface is performed by plasma-enhanced chemical vapor deposition.

In another embodiment, the step of providing a SiO$_2$ layer on the surface is performed by thermal growth of SiO$_2$.

In yet another embodiment, the initial thickness of the SiO$_2$ layer is sufficient to provide a safety margin after the plurality of patterns are etched in the SiO$_2$ layer.

In still another embodiment, the step of performing a SiO$_2$ etch is done using an inductively coupled plasma.

In a further embodiment, the step of performing a silicon etch is done using deep reactive ion etching.

In yet a further embodiment, the deep reactive ion etching is performed using SF$_6$.

In an additional embodiment, the deep reactive ion etching is followed by a step comprising exposing the silicon wafer to C$_4$F$_8$ gas.

In one more embodiment, a final etch depth is controlled to within 2% of a depth target.

According to another aspect, the invention relates to a terahertz waveguide circuit element manufactured according to the methods previously enumerated.

In one embodiment, the terahertz waveguide circuit element has a cross section of the waveguide that is rectangular.

In another embodiment, the terahertz waveguide circuit element has a final etch depth that is controlled to within 2% of a depth target.

The foregoing and other objects, aspects, features, and advantages of the invention will become more apparent from the following description and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the invention can be better understood with reference to the drawings described below, and the claims. The drawings are not necessarily to scale,
emphasis instead generally being placed upon illustrating the principles of the invention. In the drawings, like numerals are used to indicate like parts throughout the various views.

FIG. 1A is a plan view that illustrates resist spinning on a wafer.

FIG. 1B is a cross section view of a wafer that illustrates the resist coverage prior to DRIE using conventional methods.

FIG. 1C is a cross section view of a wafer that illustrates the results after DRIE using the resists of FIG. 1B. Due to thin resist coverage at the edges, the pattern is overetched (indicated by 102) and holes are etched at the bottom of a waveguide due to bad resist protection inside an already etched channel (indicated by 104).

FIG. 2 is an image that shows holes etched at the bottom of the patterns illustrated in FIG. 3.

FIG. 3 is an image that shows over-etched patterns.

FIG. 4 is an image of the same double-depth pattern as in FIG. 3 with the addition of a mask of SiO₂. The SiO₂ clearly provides patterns that are better defined in shape and size.

FIG. 5 is an illustration showing a mask layout of an OMT design.

FIG. 6 is an image showing extreme over-etching around the edges of the patterns of the design of FIG. 5 after only 3 etch patterns were processed.

FIG. 7 is a diagram that illustrates a predefined SiO₂ pattern of a waveguide twist.

FIG. 8 is an SEM image of a waveguide twist after completion of all the etch steps using the multi-step DRIE process.

FIG. 9 is a diagram that illustrates a predefined SiO₂ pattern of an OMT.

FIG. 10 is an SEM image of an OMT after completion of all the etch steps using the multi-step DRIE process.

FIG. 11 is an image of a silicon micromachined waveguide test feature highlighting the waveguide OMT and twist.

FIG. 12 is a graph showing the results of insertion loss measurements vs. frequency for a simulation (curve 1202) a wafer fabricated using the multi-step DRIE process (curve 1204) and a wafer fabricated using the first process with a SiO₂ hard mask (curve 1206). The insertion loss shown is between ports ‘a’ and ‘b’ shown in FIG. 11, so the signal passes through both the OMT and twist.

DETAILED DESCRIPTION

Fabrication Methods

One approach for fabricating highly integrated and compact millimeter receiver front-ends is to make all the RF elements in silicon where the power amplifiers, multipliers, and mixer chips can be integrated in a single silicon micromachined block.

We describe semiconductor-based fabrication techniques that allow the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration. This architecture shrinks the heterodyne receiver front-end elements into such a small footprint that allows the integration of passive and active components into such a stacked silicon wafer configuration.
PECVD deposited SiO₂ films. As an illustration, FIG. 6 presents the SEM picture of a 6-depth OMT design (see for example A. Dunning, S. Srikanth and A. R. Kerr, `A Simple Orthomode Transducer for Centimeter to Submillimeter Wavelengths', International Symposium on Space Terahertz Technology, ISSTT 2009), with extreme over-etching problems despite a thick SiO₂ protective mask of 4 µm. Moreover, as the SiO₂ is only present on the top surface of the wafer, it does not solve the resist coverage issue at the bottom of an etched pattern. Therefore, the process in which each pattern was individually etched to its desired depth would not work for the fabrication of complicated THz circuits.

### Multi-Step DRIE Process

In the new fabrication process, we avoid the use of photore sist in DRIE. This solves the through-wafer etch issue. We use only SiO₂ as the hard mask. Instead of etching each pattern individually to its desired depth, we etch only the depth difference between each pattern, as presented in Table 1. For example, rather than etching, 200 µm then 150 µm, 105 µm and so on, we will only etch 50 µm, then 45 µm, then 40 µm, and so forth. Every pattern is gradually etched down with the next one until all the patterns are completed to their final depth target.

#### TABLE 1

<table>
<thead>
<tr>
<th>Example for 5-etch pattern, where each depth difference is highlighted by underlining.</th>
<th>200</th>
<th>150</th>
<th>105</th>
<th>60</th>
<th>10</th>
<th>SiO₂ Thickness</th>
</tr>
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<tbody>
<tr>
<td>200</td>
<td>50</td>
<td>95</td>
<td>135</td>
<td>180</td>
<td>200</td>
<td>340 nm</td>
</tr>
<tr>
<td>150</td>
<td>45</td>
<td>85</td>
<td>140</td>
<td>150</td>
<td>300</td>
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<td>10</td>
<td>70</td>
<td>70</td>
<td>70</td>
<td>70</td>
<td>70 nm</td>
</tr>
</tbody>
</table>

Prior any DRIE etching, each etch depth pattern is masked by UV photolithography. Using the DRIE recipe SiO₂/Si selectivity and the depth difference between each step, the thickness of SiO₂ needed for each pattern can be calculated, as presented in Table 1. As a protection margin of safety, an addition 10-20 nm is added to these numbers in case the selectivity in DRIE fluctuates. The SiO₂ is etched in ICP, with a ~70 nm/min etch rate to ensure precise control over the final thickness. Once all the SiO₂ steps are defined, the first pattern in etched down to the silicon and the DRIE etching can begin. It should be noted that by defining the patterns in SiO₂ before any DRIE is performed, a thin photore sist can be used which offers the best resolution available.

FIG. 7 is a diagram that illustrates a predefined SiO₂ pattern of a waveguide twist.

FIG. 8 is an SEM image of a waveguide twist after completion of all the etch steps using the multi-step DRIE process.

FIG. 9 is a diagram that illustrates a predefined SiO₂ pattern of an OMT. Each segment represents a DRIE etch depth, defined by a specific SiO₂ thickness.

FIG. 10 is an SEM image of an OMT after completion of all the etch steps using the multi-step DRIE process.


Starting from the deepest etch depth, we can now start the DRIE etching, using the predefined SiO₂ as the patterning mask and the depth difference between each step as the pattern depth. Between each etch depth, the SiO₂ must be etched in the ICP to remove the remaining few nm of SiO₂ (from the extra-protection) to expose the silicon for the next pattern. The final step in DRIE will be the shallowest etch depth of the design and will complete all the patterns to their final depth target.

As a comparison, FIG. 6 and FIG. 10 present the same OMT design, fabricated using the old and new processes, respectively. We can see that the multi-step process offers far better results in terms of pattern definition and shape control. In addition, using our multi-step DRIE process provides excellent control over the final depth for each step, achieving tolerances greater than 2% over the final depth target.

Testing Results

While working on the process optimization, various tests features were fabricated to validate each development step. Straight waveguide sections measured show losses comparable to metal machined waveguides. At WR-1.5 (500 to 750 GHz) losses were measured at 0.1-0.08 dB/mm. See T. Reck, C. Jung-Kubiak, J. Gill, and G. Chattopadhyay, "Measurement of silicon micromachined waveguide components at 500 to 750 GHz", IEEE Transactions on Terahertz Science and Technology, 2014, vol. 4, pp. 33-38.


These structures only tested single etch depth devices, so to characterize the electromagnetic performance of the multietch step process a significantly more complex device is chosen, the series connection of the waveguide polarization twist shown in FIG. 8 and the orthomode transducer (OMT) shown in FIG. 10. FIG. 11 shows the OMT and twist test device.

FIG. 12 shows measurements results comparing the initial hard mask process to the final multi-etch step process. The insertion loss, or the power lost through the device, is appreciably improved with the use of the multi-etch step process. This improvement is believed to come from a
reduction in waveguide loss by the elimination of the over-etching produced by poor resist coverage. In addition, the waveguide circuit couples more efficiently since the multi-step etch process provides improved patterning accuracy. 

This multi-step DRIE process has also been demonstrated in high frequency circuits where the use conventional machining techniques is not possible, due to the very fine structures needed. We recently demonstrated a 2.55 THz waveguide HEB mixer block, with a DSB receiver noise temperature of $T_{rec}^{DSB}$ of 2000±100 K (Y-factor of 1.9±0.005). See Faouzi Boussaha, Jonathan Kawamura, Jeffery Stern, Cecil Jung, Anders Skolare, and Victor White, “Terahertz-frequency Waveguide HEB Mixers for Spectral Line Astronomy,” Proceedings of SPIE Conference on Telescopes and Astronomical Instrumentation, Amsterdam-Netherlands, July 2012. 

We have described a fabrication process for silicon-based terahertz (THz) waveguide components. This technique uses a predefined SiO$_2$ hard mask and a DRIE etching process, in which the difference between each pattern is etched, to gradually form a complex multi-depth structure. This technique provides precise dimensional control across multiple etch depths with batch processing capabilities. Nonlinear and passive components such as mixers and multipliers have been fabricated and integrated into a small silicon package. This fabrication technique enables a wafer-stacking architecture to provide ultra-compact multi-pixel receiver front-ends in the THz range. The fabricated silicon parts are extremely well defined and the final etch depths are controlled to within 2% of a depth target. Tests validate the use of silicon for THz waveguides, hybrids, OMTs and twists have been fabricated and integrated into a small silicon package. This fabrication technique enables a wafer-stacking architecture to provide ultra-compact multi-pixel receiver front-ends in the THz range.

DEFINITIONS

Unless otherwise explicitly recited herein, any reference to an electronic signal or an electromagnetic signal (or their equivalents) is to be understood as referring to a non-transitory electronic signal or a non-transitory electromagnetic signal.

Any patent, patent application, patent application publication, journal article, book, published paper, or other publicly available material identified in the specification is hereby incorporated by reference herein in its entirety. Any material, or portion thereof, that is said to be incorporated by reference herein, but which conflicts with existing definitions, statements, or other disclosure material explicitly set forth herein is only incorporated to the extent that no conflict arises between that incorporated material and the present disclosure material. In the event of a conflict, the conflict is to be resolved in favor of the present disclosure as the preferred disclosure.

While the present invention has been particularly shown and described with reference to the preferred mode as illustrated in the drawing, it will be understood by one skilled in the art that various changes in detail may be affected therein without departing from the spirit and scope of the invention as defined by the claims.

What is claimed is:

1. A method of manufacturing a silicon waveguide circuit element, comprising the steps of:
   providing a silicon wafer having a surface comprising a flat surface;
   providing a SiO$_2$ layer having an initial thickness on said surface;
   etching a plurality N of patterns in said SiO$_2$ layer, to form a plurality N of SiO$_2$ patterns having a respective thickness representing a respective depth of etching into said silicon wafer, said respective thicknesses being different from one another, where N is an integer greater than one; and
   repeating a total of N times in succession the two steps of:
   (1) performing an SiO$_2$ etch simultaneously on all of said plurality N of SiO$_2$ patterns to expose one or more respective regions of said surface of said silicon wafer beneath a thinnest remaining one of said plurality N of SiO$_2$ patterns; and
   (2) performing a silicon etch simultaneously on said silicon wafer beneath said said exposed respective regions of said surface of said silicon wafer, wherein said exposed respective regions are etched down by a depth comprising a difference between said respective depths, associated with said thinnest remaining one of said plurality N of SiO$_2$ patterns, and said respective depth associated with a next thinnest remaining one of said plurality N of SiO$_2$ patterns; wherein:
   each of said plurality N of patterns are etched down into said silicon wafer to their respective depth of etching, and a multi depth structure in said silicon wafer is formed.

2. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein the step of providing said SiO$_2$ layer on said surface is performed by plasma-enhanced chemical vapor deposition.

3. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein the step of providing said SiO$_2$ layer on said surface is performed by thermal growth of SiO$_2$.

4. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein said initial thickness of said SiO$_2$ layer is sufficient to provide a safety margin after said plurality N of patterns are etched in said SiO$_2$ layer.

5. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein said step of performing an SiO$_2$ etch is done using an inductively coupled plasma.

6. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein said step of performing said silicon etch is done using deep reactive ion etching.

7. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein said step of performing said silicon etch is done using deep reactive ion etching is followed by a step comprising exposing said silicon wafer to CF$_4$ gas.

8. The method of manufacturing said silicon waveguide circuit element of claim 7, wherein deep reactive ion etching is followed by a step comprising exposing said silicon wafer to C$_4$F$_8$ gas.

9. The method of manufacturing said silicon waveguide circuit element of claim 1, wherein said respective depths etched into said silicon wafer are controlled to within 2% of depth targets for said respective depths.

10. The method of claim 1, wherein said silicon waveguide circuit element is a terahertz silicon waveguide circuit element comprising said multi depth structure.

11. The method of claim 10, wherein said multi depth structure includes a cross section of a waveguide that is rectangular.

12. The method of claim 1, wherein:
   for the first repeating of said two steps, said thinnest remaining one of said plurality N of SiO$_2$ patterns has
said respective thickness representing a deepest of said respective depths of etching into said silicon wafer, and for the final repeating of said two steps, said thinnest remaining one of said plurality N of SiO₂ patterns has said respective thickness representing a shallowest of said respective depths of etching into said silicon wafer.

13. A method of fabricating a silicon waveguide component, comprising:

providing at least one mask on silicon, the at least one mask including a plurality N of patterns, the patterns each:

associated with a different thickness of the mask designed to achieve a different depth of etching into the silicon, where N is an integer; and

indexed with an integer j, wherein 1 ≤ j ≤ N and the jᵗʰ pattern is designed to achieve a deeper depth of etching than the (j+1)ᵗʰ pattern;

performing N etch steps each indexed with an integer k, wherein:

1 ≤ k ≤ N and the etch steps are performed in order of increasing k, and

during the kᵗʰ etch step, the silicon is etched with all the one or more jᵗʰ patterns, wherein j ≤ k, by a depth comprising a difference between the depth associated with the jᵗʰ pattern wherein j = k and the depth associated with the jᵗʰ pattern wherein j = k+1; and wherein each pattern is etched down into the silicon such that the jᵗʰ pattern is etched down to the depth associated with the jᵗʰ pattern and the waveguide component comprising a multi depth structure in the silicon is formed.

14. The method of claim 13, wherein the silicon is etched using deep reactive ion etching.

15. The method of claim 13, wherein the silicon waveguide component is a silicon terahertz waveguide.

16. The method of claim 15, wherein the silicon terahertz waveguide has an insertion loss that is decreased as compared to insertion loss for a silicon terahertz waveguide fabricated using a process wherein structures in the silicon terahertz waveguide are etched to their final depth in the silicon in a single etch step.

17. The method of claim 15, wherein the silicon terahertz waveguide hosts a mixer.

18. A method of fabricating a silicon waveguide component, comprising:

providing a mask including a plurality of patterns;

gradually etching the plurality of the patterns into silicon using a plurality of etch steps, wherein:

the patterns are each etched to an etch depth in the silicon; the patterns are etched in a succession starting with the pattern being etched to a deepest etch depth and ending with the pattern being etched to a shallowest etch depth and such that each of the patterns are etched down with a next one of the patterns, and each etch step etches a depth difference between the patterns until all the patterns are etched to their etch depth.