Experimental Durability Testing of 4H SiC JFET Integrated Circuit Technology at 727 °C

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sic.grc.nasa.gov
SiC Electronics Benefits to NASA Missions

Intelligent Propulsion Systems

“GEER” Venus Test Chamber

Hybrid Electric Aircraft

Venus Exploration

NASA GRC’s internal research effort has been to focus on durable integrated circuits at 500 °C for > 3000 hrs.
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Past work with single layer of interconnect

- Differential amplifier made in 6H-SiC operated 6519 hours at 500 °C in air ambient.
- Complexity limited. Only 2 transistors and 3 resistors.
- JFET approach good for minimizing gate leakage and durability at 500 °C.

8.1 vs past work - Two levels of metal interconnect

Processing enhancements for conformal processing on topology.

- Proximity sputtering of TaSi$_2$ (21mm target to substrate spacing).
- LPCVD tetraethyl orthosilicate (TEOS) deposited 720 °C.
- Design rules for thick dielectrics and metal traces.

Enables crisscrossing traces and on chip capacitors.  

Now 4H not 6H

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8.1 Previous Results Overview

• 3-stage ring oscillator lasted 3000 hours at 500 °C.
• D to A (4-Bit) IC lasted 10 hours at 500 °C.
• Address decoder (4-bit) IC last 120 hours at 500 °C.
• SRAM Cell (3-3) lasted 9.5 hours at 500 °C.

• Initial “ramp” temperature test had JFET and 3 stage ring oscillator demonstrate short term operation to 727 °C as described at ECS 2015. Use a sapphire wafer for “package.” The lead oxide glass based Pt paste die attach material which had been designed for 500 °C operation cause a lost of back side contact.

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Materials Science Forum. 858, pp. 1112-1116 (2016)
8.1 Deficiencies

- Crack formation induced fail-open of top metal interconnect.
- Device resistance degradation.
- Gate-to-channel leakage/short from notching of gate etch mask metal.
- Parasitic circuit imbalance induced by mobile ion contamination.

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8.1 vs 9.2 Both generations were fabricated with the same process sequence using the same lithographic masks, except for the following differences;

- “Gate notching” defects present in 8.1 JFETs were eliminated for 9.2 JFETs by reduced time delay and improved wafer storage between gate and mesa etches.
- Heavily-implanted SiC contact regions were formed using P implantation for 9.2 chips instead of N implantation used for 8.1 chips.
- SiC ohmic contact for 9.2 chips was implemented using a 50 nm sputtered Hf layer instead of the 50 nm sputtered Ti layer used for 8.1 chips.
- The 9.2 process added a 67 nm Si₃N₄ layer between the top two SiO₂ passivation layers.
- Extensive laboratory improvements to mitigate Na contamination were implemented for 9.2 wafer processing.

![Image of 4H-SiC structure with labels for layers and implantation details](image)

9.2 Limited Cracking During Si$_3$N$_4$ LPCVD

- 9.2 had cracks formed from too fast of ramp during LPCVD of stoichiometric Si$_3$N$_4$.
- The deposited Si$_3$N$_4$ held the TaSi$_2$ from splitting upon cooling.
- Only very few places had any cracks. Image right is example of crack free area on same sample.

![Image of die (12,11) and die (12,05) with FIB Mask and various layers of SiO$_2$, Si$_3$N$_4$, TaSi$_2$, and Hf + TaSi$_2$. The images show crack filled with Si$_3$N$_4$.](image-url)
New high-T packaging (32 pins)

- All three tests started with a 500 °C burn-in on the order of roughly 100 hours.
- The 931 chip was subjected directly to a ramp to 700 °C following burn-in while the chips for test 6A2 and 924 were cooled back to room temperature prior to ramping to peak testing temperature.

<table>
<thead>
<tr>
<th>Test #</th>
<th>Design</th>
<th>Si₃N₄</th>
<th>Die Attach</th>
<th>Lid</th>
<th>Hrs @ 500 °C</th>
<th># of Cycles</th>
<th>Test Temp °C</th>
<th>Hrs at Temp</th>
<th>Last Device Hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>6A2</td>
<td>8.1</td>
<td>No</td>
<td>PbOₓ glass-Pt</td>
<td>No</td>
<td>94</td>
<td>2</td>
<td>727</td>
<td>45.45</td>
<td>27.45</td>
</tr>
<tr>
<td>924</td>
<td>9.2</td>
<td>Yes</td>
<td>PbOₓ glass-Pt</td>
<td>No</td>
<td>117</td>
<td>2</td>
<td>700</td>
<td>19.2</td>
<td>16.2</td>
</tr>
<tr>
<td>931</td>
<td>9.2</td>
<td>Yes</td>
<td>Au Paste</td>
<td>Yes</td>
<td>111</td>
<td>1</td>
<td>700</td>
<td>191.5</td>
<td>143.5</td>
</tr>
</tbody>
</table>

PbOₓ glass-Pt

Au Paste
- Before packaging and after testing images of test 6A2.
- Note the amount of lead oxide glass/Pt die attach that has migrated to the area around the bond pads.
- Image (b) also has a lot of particle fallout.
The lead oxide glass/Pt die attach had completely covered the JFET in the upper right corner of image (b).

There is a cracking pattern that is more intense at the label in Metal 1.

The three stage ring oscillator output trace changed color.

3-stage ring oscillator failed before 727 °C testing started.
At 727 °C in air ambient

- NOR4 function 60 hrs.
- AND4 function 32 hrs.
- The JFET lasted 25 hrs.
- 0.5mm² metal-insulator-metal capacitor increased in leakage from 1-2 µA to 10-20 µA gradually over 28 hours.

VSS=-20V, VDD=20V
• Although the temperature was 27 °C lower and the time at test temperature was less, the amount of lead oxide glass/Pt die attach migration was much worse.

• LF, MF, and HF = low, medium, and high frequency. **NO CRACKING.**
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- Plot of frequency and amplitude output of 3 different ring oscillators
- HF lasted the longest possibly since it had the least lead oxide on it.
- LF had an intermittent failure at 10 hours.
- All three the output amplitude first started to drop at 8 hours.

VSS = -20V and VDD = 25V
• No die attach migration or debris fallout - Au paste was used and lid covered the die.

• Circle in red on image (a) are three bond pads that did not show any aging and only near other traces or device was there any cracking. The areas circled in red were no biased or at VSS which was also the same potential as the backside of the die.
• A higher magnification optical micrograph of the top part of die (8,16) in test 931 after electrical testing for 191.5 hours at 700 °C.

• Note the absence of die attach migration or debris fallout since Au paste was used and lid covered the die.

• Only dielectric cracking and TaSi₂ oxidation are evident.

• An even larger view of the JFET area can be seen in the next slide.

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(b) FESEM image of a FIB prepared cross-section of a crack. The crack allowed the TaSi$_2$ to oxidize.

(c) JFET IOFF started shifting at 25 hour but with did not fail like 6A2.
• The LF 3-stage ring oscillator of test 931 started to fail intermittently at 8 hours, similar to the LF 11 stage from 924.

• The three ring oscillators of test 924 and the ring oscillator of test 931 (shown right) all exhibited a shift in amplitude 8 hours into 700 °C testing suggests a possibly common mode/location of failure for these integrated circuits.

VSS = -25V and VDD = 25V
Output high and output low values as functions of time at 700 °C

The input and output waveforms for the HF NOR

MFNOR on 931 also lasted 143.5 hours at 700 °C VSS=-25V and VDD=25V
Conclusion

• Preliminary accelerated IC testing experiments at temperatures above 700 °C indicate that Au paste should be used for die attach at 700 °C instead of the lead oxide glass based Pt paste which had been designed for 500 °C operation.

• The formation of cracks in dielectric (SiO$_2$-Si$_3$N$_4$-SiO$_2$) overlying the IC interconnect, which induced oxidization and cracking of the TaSi$_2$ interconnect, was observed to be a limiting factor in our current 4H-SiC JFET IC process.

• Failure was not observed with $T \geq 700$ °C for the 32 pin package, the SiC 4H-JFET structure, the Hf ohmic contacts, or TaSi$_2$ in regions free of dielectric cracks.

• If process revisions can eliminate overlying dielectric crack formation then highly durable 4H-SiC JFET integrated circuits for temperatures as high as 700 °C may become achievable.
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Fig. 10. (a) Optical image of packaged device with room light illumination. (b) Optical image at 650 °C of packaged device with a large JFET under forward bias of the gate-channel junction resulting in blue light emission. Three ring oscillators and a MF NOT are also operating while the image is taken.
## Integrated circuits in fabrication

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Inputs</th>
<th>Outputs</th>
<th>Transistors, I/O Pads</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-Bit A/D</td>
<td>Analog voltage signal, optional external clock, output type select</td>
<td>4 bit parallel digital latch, pulse width modulated (PWM)</td>
<td>203 JFETs, 23 I/Os</td>
<td>Internal ring-oscillator clock circuit</td>
</tr>
<tr>
<td>4X4 Bit Static RAM</td>
<td>Read, Write, Data Lines, Address Lines</td>
<td>4 bit parallel digital latch, pulse width modulated (PWM)</td>
<td>220 JFETs, 30 I/Os</td>
<td>Address decoder, sense amplifiers</td>
</tr>
<tr>
<td>Source Separation Sensor Signal Transmitter</td>
<td>Capacitive sensor</td>
<td>Frequency modulated with address code</td>
<td>301 JFETs, 20 I/Os</td>
<td>Each sensor signal is tagged with unique address code</td>
</tr>
<tr>
<td>Ring Oscillators</td>
<td>Capacitive sensors</td>
<td>Frequency modulated signals (up to 500 MHz)</td>
<td>10-12 JFETs, 6 I/Os</td>
<td>On-chip large transistors for power amplification</td>
</tr>
<tr>
<td>Binary Amplitude Modulation RF Transmitter</td>
<td>Low power binary signal</td>
<td>High-Power RF signal to antenna</td>
<td></td>
<td>Could connect with PWM from A/D</td>
</tr>
<tr>
<td>Op Amp, 2-Stage</td>
<td>Differential</td>
<td>Voltage gains to 50 w/ on-chip resistors</td>
<td>10 JFETs</td>
<td>For piezoelectric SiC pressure sensors</td>
</tr>
<tr>
<td>4-Bit D/A</td>
<td>4 digital</td>
<td>1 analog</td>
<td>20 JFETs</td>
<td></td>
</tr>
</tbody>
</table>
Process with two levels of metal interconnect

- Gate $N_A > 2 \times 10^{20}$ cm$^{-3}$ at 0.17$\mu$m thick
- n-channel $1 \times 10^{17}$ cm$^{-3}$ at ~0.5 $\mu$m thick
- Lower p material $< 3 \times 10^{15}$ cm$^{-3}$ at ~6-8 $\mu$m thick.
Process with two levels of metal interconnect

- Ti/Ni etch mask for gate.
- Self align nitrogen implant of dose $7.0 \times 10^{12}\text{cm}^{-2}$ at 70 KeV.
Process with two levels of metal interconnect

- Ti/Ni mask use to define resistors and channels.

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Process with two levels of metal interconnect

- Si mask was used for box implant of $1.6 \times 10^{15}$ cm$^{-2}$ while heated to 873 K.
- Capped and annealed at 1633 K for 4 hours in N$_2$. 

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Process with two levels of metal interconnect

- Thermal and deposited oxide.
Process with two levels of metal interconnect

• Dry and wet etch of via 1.
Process with two levels of metal interconnect

- Bake out and sputter deposition of metal 1.
Process with two levels of metal interconnect

- Dry etch of metal 1.
Process with two levels of metal interconnect

- Deposited oxide 2.
Process with two levels of metal interconnect

• Dry etch of via 2.
Process with two levels of metal interconnect

• Bake out and sputter deposit of metal 2.
Process with two levels of metal interconnect

• Dry etch metal 2.
Process with two levels of metal interconnect

- Deposit oxide 3.
- Dry and wet etch of via 3 (not shown and only used for bond pads).
Process with two levels of metal interconnect

- Bake out and deposit of metal 3
Process with two levels of metal interconnect

• Dry etch of metal 3.
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