"An Evaluation of Flash Cells Used in Critical Applications"

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Introduction and Agenda

• Collaborative Effort Between NASA and DoD/DMEA
• Test Methods and Protocols
• Key Parameter: Threshold Voltage ($V_T$)
• DUT: Microsemi (Actel) A3P250L FPGA
  – Common Technology Between spaceflight electronics and DoD fuze control circuitry.
• Long-Term “Engineering Run” at +25 °C and +150 °C (6 DUTS)
• Threshold Voltage Distribution: Large Population (~1,000 DUTS)
  – Part-to-Part Variability
  – Outliers
• Results: Environmental Tests
  – Temperature (+25 °C, +125 °C, and +150 °C)
  – Electromagnetic (EM) Susceptibility
  – Neutron Irradiation Susceptibility
  – Electrostatic Discharge (ESD) Susceptibility
• Future Testing (in-process and planned; this is a work in progress)
• Additional Material and Data in the On-line Version of This Talk
Threshold Voltage ($V_T$)

Microsemi A3PL FPGA Flash Cell

- Quantity of electrons stored on floating gate modifies the threshold voltage ($V_T$).
- Threshold voltage is the “turn on” voltage for the transistor.

Figure courtesy of Microsemi Corp.
Stress Induced Leakage Current (SILC)

Electrons can tunnel at low bias if Traps line up at a spacing of 3 nm or less.

Chart courtesy of Microsemi Corp.
Sample $V_T$ Distribution in an FPGA

A3P250L FPGA $V_T$ Distribution
S/N CK002, 6,048 Hours @ 150 °C, June 1, 2015

Counts

$V_T$ (volts)

Erased
Programmed
Reference
Experiment Goals

• The primary objective is to determine the probability of extrinsic flash cells in the population and to determine how that will limit the device’s lifetime.

• A secondary objective is to track the intrinsic populations lifetime which is a function of storage temperature.

• A third objective is to measure the flash cells’ susceptibility to other environmental stresses.
  – Electromagnetic (EM) radiation
  – Neutron irradiation
  – Electrostatic Discharge (ESD)
  – Heavy Ion Irradiation (total dose tests have been conducted)
  – Other (please suggest)
Description of DUTs

• **Microsemi (Actel) A3P250L FPGA**
  – Relatively small FPGA
  – PBGA (Plastic Ball Grid Array) Package (FG144)
  – Single Foundry for all DUTs
  – Most parts from one wafer lot (QLWY8)
    – Small number of DUTs from a second wafer lot (QLG10)

• **9 Logic Designs Used**
  – No artificial test structures
  – Logic blocks designed by different authors and styles (including macro generators)

• **10 Erase-Program-Verify Cycles for Each Device**
  – Realistic stress for our applications.
  – Manufacturer’s rating: 500 cycles

• **Complements and Extends work by Sandia National Labs**
  – Sandia is a Department of Energy organization that has previously investigated flash cell reliability. See references at the end of this presentation.
Test Station for A3P250L FPGA
Long-Term “Engineering Run”

• **Goals**
  - Develop and refine test methods, procedures, and analysis tools and techniques
  - “Look ahead” at device response and behavior of intrinsic population

• **DUTS: 6 A3P250L FPGAs (3 each from two lots)**
  - 4 DUTs baked at 150 °C
  - 2 DUTs kept at room temperature (control samples)

• **11,592 hours (~1.3 years) at 150 °C**
Erased: Engineering Run

A3P250L FPGA Average Erased $V_T$
11,424 Hours @ 150 °C, March 26, 2016
A3P250L FPGA Average Programmed $V_T$
11,424 Hours @ 150 °C, March 26, 2016
Effects of 150 °C Bake on Flash-based FPGA

V_T Delta After 11,424 Hours @ 150 °C: S/N RK003

Counts vs. V_T (volts)

- Red line: 0 Hours
- Blue line: 11,424 Hours @ 150 C

May 3, 2016
59th Annual Fuze Conference
### Erased Cell Data Retention at 150 °C

#### Performance vs. Specification

<table>
<thead>
<tr>
<th>Tj (°C)</th>
<th>Spec Life (years)</th>
<th>6,000 Hour Data Life (years)</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>102.7</td>
<td>306.8</td>
</tr>
<tr>
<td>85</td>
<td>43.8</td>
<td>131.1</td>
</tr>
<tr>
<td>100</td>
<td>20.0</td>
<td>60.0</td>
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<tr>
<td>105</td>
<td>15.6</td>
<td>46.9</td>
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<tr>
<td>110</td>
<td>12.3</td>
<td>36.9</td>
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<tr>
<td>115</td>
<td>9.7</td>
<td>29.2</td>
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<tr>
<td>120</td>
<td>7.7</td>
<td>23.2</td>
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<tr>
<td>125</td>
<td>6.2</td>
<td>18.6</td>
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<tr>
<td>130</td>
<td>5.0</td>
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<td>135</td>
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<tr>
<td>140</td>
<td>3.3</td>
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<tr>
<td>145</td>
<td>2.7</td>
<td>8.0</td>
</tr>
<tr>
<td>150</td>
<td>2.2</td>
<td>6.6</td>
</tr>
</tbody>
</table>

Specification Data From RT and Military ProASIC3 Data Sheets.

6,000 Hour Data derived predictions courtesy of Microsemi Corporation.
Initial Effects

- Engineering tests and data in literature showed an initial rapid movement in threshold voltage after configuring a device.

- Three devices configured and then margin tested once per day.

- Protocol updated: Baseline margin tests after several weeks of “settling time.”
Initial Effects: Erased

Average Erased $V_T$ After Programming

Delta Average $V_T$ (mV) vs. Time Since Programming (days)

- K2216

May 3, 2016
Initial Effects: Programmed

Average Programmed $V_T$ After Programming

Delta Average $V_T$ (mV)

Time Since Programming (days)

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Instrumentation Sensitivity

$V_T$ Measurement Independent on (In-Spec) Supply Voltages

Counts

$V_T$ (volts)

-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10

1000000 100000 10000 1000 100 10 1

100% Vcc
90% Vcc
80% Vcc
110% Vcc
Population Analysis

• Determined $V_T$ Characteristics of a Large Population of Parts
  – ~1,100 DUTs

• Analysis Criteria on Threshold Voltage ($V_T$) Histograms
  – Mean
  – Spread
  – Tails
  – Outliers
Population Analysis: Metrics

Mean

Spread

Read Voltage

Tails

Counts

-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10

V_T (volts)

Counts

-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10

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Population Analysis: Mean

Average Initial Device Threshold ($V_T$)
1,092 A3P250L Devices, April 10, 2016

Erased Std Dev: 0.18V
Programmed Std Dev: 0.37V

Erased Average

Programmed Average
Population Analysis: Spread

Spread of Device Threshold ($V_T$)
1,092 A3P250L Devices, April 10, 2016

- Erased Std Dev: 0.13V
- Programmed Dev: 0.10V

Erased Spread: Avg - Max
Program Spread: Avg - Min

Outliers
Population Analysis: Tails

Tails of Device Threshold ($V_T$)
1,092 A3P250L Devices, April 10, 2016

Erased Std Dev: 0.22V
Programmed Std Dev: 0.36V

Erased Tail: Max $V_T$
Programmed Tail: Min $V_T$

Outliers
Population Analysis: Outlier

S/N F0205, Initial Margin Test, March 10, 2016

Erased Standard Deviation = 0.21V
Outlier is 8.9 standard deviations from the mean.
DUT passes verify.
EM Susceptibility: Introduction

• **Goal:** Determine Susceptibility of Flash Cell to EM Radiation

• **DUT Configuration:**
  - 3 DUTs
  - Unpowered
  - No enclosure or other shielding
  - Simple Board: Traces for power, ground, and programming (not I/O)

• **A first test:** Tested with a NASA Mars science instrument
  - Multiple Runs with horizontal and vertical polarizations
  - Test levels based on science instrument (not fuze) requirements
# EM Susceptibility: Testing Levels

## Table 3-8: RS103 Test Levels

<table>
<thead>
<tr>
<th>Frequency Band /Range</th>
<th>Test Level V/m (dBuV/m)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 kHz to 390 MHz</td>
<td>4 V/m (132dBuV/m)</td>
<td></td>
</tr>
<tr>
<td>309 MHz to 405 MHz</td>
<td>28 V/m (148dBuV/m)</td>
<td>UHF Band, Direct Downlink</td>
</tr>
<tr>
<td>405 MHz to 500 MHz</td>
<td>4 V/m (132dBuV/m)</td>
<td></td>
</tr>
<tr>
<td>500 MHz to 3000 MHz</td>
<td>4 V/m (132dBuV/m)</td>
<td>WISDOM Payload</td>
</tr>
<tr>
<td>3000 MHz to 20,000 MHz</td>
<td>4 V/m (132dBuV/m)</td>
<td></td>
</tr>
</tbody>
</table>
EM Susceptibility Testing Facility
EM Susceptibility Results (typical)

EM Test, March 2016, S/N K2246

Counts vs. $V_T$ (volts) graph showing before and after EM results.
Neutron Susceptibility Testing

- **Sample Size:** 20 DUTs

- **Test Levels:**
  - $2 \times 10^{12}$ n/cm$^2$ (7 DUTs)
  - $2 \times 10^{13}$ n/cm$^2$ (7 DUTs)
  - $2 \times 10^{14}$ n/cm$^2$ (6 DUTs)

- **Test Conditions**
  - 1 MeV equivalent spectrum
  - DUTs unbiased
  - DUTs’ balls shorted

- **Test Facility:**
  McClellan Nuclear Research Center (near DMEA)

*MNRC Reactor in Operation*
ESD Susceptibility Testing

- **Sample Size:** 20 DUTs
- **Test Levels:**
  - Phase Lock Loop (PLL): 500V
  - Other Power and I/O: 2 kV
- **Test Equipment:** Thermo Scientific MK.1 ESD and Static Latch-up Test System
Temperature Experiment Summary

Engineering Run
* 4 devices at 150 °C for 11,592 hours + 2 control samples
* One failure at 11,592 hours; probably mechanical, part undergoing analysis
* $V_T$ shift very small

Large Population
* # of Parts Programmed: 1,091
* # of Parts Margined: 1,091
* # of Outliers\(^1\): 7 (~0.6%)
* # of Part Failures\(^2\): 1

322 Parts Soaking at 150 °C
327 Parts Soaking at 125 °C
333 Parts Soaking at 25 °C (add’l 57 being prepared)

\(^1\)All outliers were erased cells and passed Verify test.
\(^2\)K1631 would not margin or verify; likely non-flash failure, under failure analysis.
Summary, Conclusion, and Path Forward

• **Test Method and Data Analysis Tool Development**
  – Utilize Device’s Design for Test Capability
  – Write Semi-custom Data Analysis Tools
  – Produce Credible, Useful Results

• **Testing Large Populations Necessary**
  – Significant Variability Between DUTs
  – Detect Outliers (~ 0.6 % for the subject device)
  – Significant Difference in Device Retention Time

• **Investigate Tighter Threshold Voltage ($V_T$) Limits on Verify Operation**

• **Assistance Needed on EM Test Limits, Protocols, and Facilities**

• **Possible Future Large Population Test: TI Microcontroller**

• **Track Large Populations: Temperature Testing Ongoing**
  – +25 °C, +125 °C, and +150 °C
References


• “Threshold voltage distribution in MLC NAND flash memory: characterization, analysis, and modeling,” Cai, Yu; Haratsch, Erich; Mutlu, Onur; and Mai, Ken, Proceedings of the Conference on design, automation and test in europe, ISSN 1530-1591, 03/2013, DATE '13, pp. 1285 – 1290.