SpaceCube Technology Brief
Hybrid Data Processing System

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SpaceCube Overview

Heritage

- GOAL: close the gap with commercial processors while retaining reliability
- Started in 2006 at GSFC as R&D
- **38+ Xilinx device-years on orbit**
- 22 Xilinxes in space by 2016
- 8 systems in space by 2016
- Various R&D efforts on hardware acceleration

Hybrid Data Processing

- Parallel data processing:
  - FPGA + DSP + Processor(s)
- SpaceCube can move **3,000x** more data than a sequential processor per clock cycle

SpaceCube v2.0

- Currently TRL-7
- Leverages 10 years of design heritage and operation experience
- **$10M+ of NRE**
- Adopted by SSCO for all missions
- IPC 6012B Class 3/A PWB Reliability
- Modular: 9 Mission-Unique I/O cards
- **Run-Time Reconfigurable**

Xilinx Virtex-5 FPGA

SpaceCube v2.0

**SpaceCube is a Mission-Enabling Technology**
Commercial Processor Trend

“Fastest” consumer CPU in 2011
Space Processor Trend
Processor Trend Comparison

- Intel Core i7 3960X (Hex core)
- Intel Core i7 980 (Hex core)
- Intel Core i7 920 (Quad core)
- Intel Core 2 QX9770 (Quad core)
- Intel Core 2 (Quad core)
- AMD Athlon FX
- AMD Athlon XP
- Mars Rovers
- MRD
- New Horizons
- DAWN
- LRO
- SDO
- Curiosity

1,000x
Future Space Processing Requirement

Next Generation Mission Processing Requirements (Decadal Surveys)

Transistor count

1,000x Gap

SCS750
RAD750
RAD6000
RAD386
1750A
RCA 1802

1,000,000
10,000,000
100,000,000
1,000,000,000
10,000,000,000
100,000,000,000
1,000,000,000,000

SpaceCube Family Overview

### v1.0
- 2009: STS-125
- 2009: MISSE-7
- 2012: SMART (ORS)

### v1.5
- 2013: STP-H4
- 2016: STP-H5

### v2.0-EM
- 2013: STP-H4
- 2016: STP-H5

### v2.0-FLT
- 2017: RRM3
- 2018: STP-H6 (NavCube)
- 2018: NEODaC
- 2020: Restore-L
- Many NASA proposals

### v2.0 Mini
- 2016: STP-H5
- Many NASA proposals
Example SpaceCube Processing

Real-Time Image Tracking of Hubble

Fire Classification

Gigabit Instrument Interfacing

Xilinx ISS Radiation Data

Spectrometer Data Reduction

Image Compression
On-Board Image Processing

- Successfully tracked Hubble position and orientation in real-time operations
- FPGA Algorithm Acceleration was required to meet 3Hz loop requirement

<table>
<thead>
<tr>
<th>Rendezvous</th>
<th>Deploy (Docking Ring)</th>
</tr>
</thead>
<tbody>
<tr>
<td>➔ Typical space flight processors are 25-100x too slow for this application</td>
<td></td>
</tr>
</tbody>
</table>
Processor Card

- 2x Xilinx Virtex-5 (QR) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 4x 512MB DDR SDRAM
- 2x 4GB NANDFlash
- 16-channel Analog/Digital circuit for system health
- Optional 10/100 Ethernet interface
- Gigabit interfaces: 4x external, 2x on backplane
- 12x Full-Duplex dedicated differential channels
- 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Mechanical support for heat pipes and stiffener for Xilinx devices

Power Draw: 6-15W
Weight: 0.98-lbs
22 Layers, Via-in-Pad
IPC 6012B Class 3/A

2014 Global Award: Most innovative design worldwide in the Military/Aerospace sector
Processor Card Diagram

Xilinx 0 Virtex-5
- Flash
- DDR
- DDR
- SRAM

Xilinx 1 Virtex-5
- DDR
- DDR

Aeroflex UT6325 CCGA
- PROM
- A/D
- Main Osc

Main cPCI J1 Connector
- cPCI or GPIO, 60

Custom cPCI J2 Connector
- RST/GPIO, 5
- GPIO/LVDS, 52
- GTX, 2x

Service Port

Airborn 4x HS Modules
- GTX, 2x each FPGA

Airborn Nano 85-pin
- Ethernet
- LVDS/422

Airborn MDM-15
- JTAG

Airborn Nano 85-pin
- LVDS/422
- 422
Example Mission-Unique I/O Cards

- Restore-L Video/Spacecraft Interface Card
- LIDAR Digitizer, Front-End, and Laser Card
- GPS RF Front-End Interface Card
Spinoff Technologies

GPS Receiver – L1/L2C Tracking

LIDAR Instrument – Configurable Resolution
**High Level Requirements:**

- Interface with Spacecraft and Payload Busses
- Interface with vision sensors
- Host Relative Proximity Operations application
- Host Robotic Manipulation Control application

**Restore-L Dual SpaceCube Payload Control Computers**

**Restore-L will fly 21 Xilinx Virtex-5 FPGAs**

**Restore-L Capture of Landsat 7**
What About Radiation Effects??

If Spare is “Cold”, then worst case error probability: $Pe(sys) = [8x Pe(Xilinx) + 16x Pe_DDR]$
Establishing SEE Error Rates

Assessment Process

- Radiation Environment
- Establish Device WCA
- Establish System WCA
- Establish Application WCA
- ID Functional Independence
- Selective FPGA Mitigation

Labor Intensive

NASA Risk Assessment

<table>
<thead>
<tr>
<th>Likelihood</th>
<th>Safety 100% Device Utilization WCA</th>
<th>Estimated Restore WCA Upset Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Likelihood</td>
<td>100% Device Utilization WCA</td>
</tr>
<tr>
<td></td>
<td>Safety (Estimated likelihood of</td>
<td>100% Device Utilization WCA</td>
</tr>
<tr>
<td></td>
<td>Safety event occurrence)</td>
<td></td>
</tr>
<tr>
<td>5 Very High</td>
<td>( P_{SE} &gt; 10^{-1} )</td>
<td></td>
</tr>
<tr>
<td>4 High</td>
<td>( 10^{-2} &lt; P_{SE} \leq 10^{-1} )</td>
<td></td>
</tr>
<tr>
<td>3 Moderate</td>
<td>( 10^{-3} &lt; P_{SE} \leq 10^{-2} )</td>
<td></td>
</tr>
<tr>
<td>2 Low</td>
<td>( 10^{-5} &lt; P_{SE} \leq 10^{-3} )</td>
<td></td>
</tr>
<tr>
<td>1 Very Low</td>
<td>( 10^{-6} &lt; P_{SE} \leq 10^{-5} )</td>
<td></td>
</tr>
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</table>

Estimated Restore WCA Upset Rates

- Device WCA: 0.484%
- PCC WCA: 1.934%
- RPO PCC: 1.074%
- RSW PCC: 0.222%
- RPO + RSW: 1.296%

Note: Assumes BRAM Mitigation

Note: Actual utilization for RPO and RSW PCCs as of 4/18/2016

Note: Assumes RPO & RSW PCCs must be error-free for full operation
Robotic Refueling Mission SpaceCube

High Level Requirements:
- Interface with ISS and RRM3 instruments:
  - Cameras, thermal imager, motors
- Monitor/Control cryocooler and fuel transfer
- Stream video data
- Motor control of robotic tools
- Host Wireless Access Point

1553/Ethernet/Digital Card

Analog Card
NEODaC Instrument Development

- Detect and Characterize NEOs
- Working with “Partner” organization on complex detector instrument
- SpaceCube FPGAs being used to solve very challenging avionics requirements and host on-board data processing applications and compression
- Successful Detector readout with SpaceCube completed
- March 2018 Delivery

Xilinx Driver: 1.6Gbps, 1300mV, 17%

**HSCSI Link Test Results**

<table>
<thead>
<tr>
<th>Transmitter Swing (mV)</th>
<th>Transmitter % Pre-emphasis</th>
<th>Test Duration</th>
<th>Bit Error Count</th>
<th>BER (*)</th>
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<tbody>
<tr>
<td>500</td>
<td>0</td>
<td>6hr</td>
<td>32</td>
<td>9.2E-13</td>
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<tr>
<td>500</td>
<td>8</td>
<td>18hr</td>
<td>0</td>
<td>9.6E-15</td>
</tr>
<tr>
<td>800</td>
<td>0</td>
<td>4hr</td>
<td>4</td>
<td>1.7E-13</td>
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<tr>
<td>800</td>
<td>25</td>
<td>20hr</td>
<td>0</td>
<td>8.7E-15</td>
</tr>
<tr>
<td>1300</td>
<td>17</td>
<td>20hr</td>
<td>0</td>
<td>8.7E-15</td>
</tr>
<tr>
<td>1300</td>
<td>0</td>
<td>19hr</td>
<td>52</td>
<td>4.7E-13</td>
</tr>
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</table>

- Note: BER calculation assumes at least 1 error
- 58-hours of error-free transmission
SpaceCube on the ISS

ISS Flying Towards You

Image Credit: DoD Space Test Program
SpaceCube v1.0

STS-125 Shuttle Payload Bay

MISSE-7/8 ISS Payload

- 7 years of operation
- 4x Virtex-4 XC4VFX60: 0.1 SEU/FPGA/Week
- 2x on-orbit file uploads and reconfiguration
STP-H4 ISS Payload

2 years of operation. 3x Virtex-5 XC5VFX130T: 1 SEU/FPGA/Week
Successful on-orbit file upload and reconfiguration
The Space Test Program-H5 (STP-H5) external payload, a complement of 13 unique experiments from seven government agencies, is integrated and flown under the management and direction of the Department of Defense’s Space Test Program.

SpaceX Launch Scheduled November 11, 2016
Questions?