Experimentally Observed Electrical Durability of 4H-SiC JFET ICs Operating from 500 °C to 700 °C

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Abstract. Prolonged 500 °C to 700 °C electrical testing data from 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) are combined with post-testing microscopic studies in order to gain more comprehensive understanding of the durability limits of the present version of NASA Glenn’s extreme temperature microelectronics technology. The results of this study support the hypothesis that \(T \geq 500 \, ^\circ \text{C}\) durability-limiting IC failure initiates with thermal-stress-related crack formation where dielectric passivation layers overcoat micron-scale vertical features including patterned metal traces.

Previously, we reported multi-level interconnect 4H-SiC JFET ICs operating for 1000’s of hours at 500 °C \([1,2]\) and briefly to 700 °C \([2,3]\).

Below we present additional data from packaged integrated circuit oven-testing at 500 °C and 700 °C in room-air atmosphere.

500 °C: All circuits now tested to failure, which occurs prior to 7000 hours.

700 °C: NOR logic gate (left) and ring oscillators (right) \([3]\).

Microscopic studies of multiple failed ICs evidence a common mechanism of IC failure (first proposed in \([2]\), further supported below):

1. Thermal-stress causes cracks to form in the dielectric, often above topology induced by edges of underlying metal interconnect features.
2. Cracks enable atmospheric oxygen to reach and locally oxidize (optically discoloring) underlying TaSi\(_2\) metal interconnect.
3. As local TaSi\(_2\) oxidation proceeds, interconnect local resistance increases leading to circuit degradation and failure.

Conclusions:

1. Durability of present-generation 4H-SiC JFET IC at 500 °C is between 1500 hours to 7000 hours.

2. Crack formation/propagation in dielectric film limits \(T \geq 500 \, ^\circ \text{C}\) IC operating lifetime.

References:


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